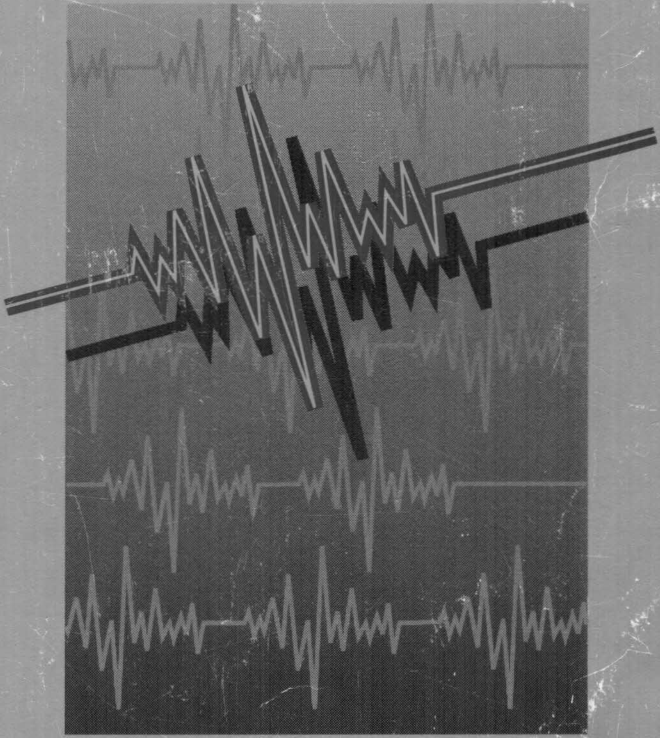
MICROELECTRONICS
ANALOG
COMMUNICATIONS
HANDBOOK



MITEL
SEMICONDUCTOR

MICROELECTRONICS **ANALOG** COMMUNICATIONS HANDBOOK

MITEL®

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Issue 8

MITEL®

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GENERAL INFORMATION

MITEL®

MITEL®

Mitel Semiconductor

Mitel Semiconductor is an international supplier of mixed analog and digital telecommunication and data communication components. Since the founding of Mitel Semiconductor in 1976, the cornerstone of Mitel's success has been the innovative design of analog circuits such as tone-to-pulse converters, DTMF receivers and crosspoint switches.

Today, Mitel remains the leader in DTMF technology with products ranging from filters and decoders to completely integrated single chip DTMF receivers and transceivers. We have also developed a serial bus interface called the ST-BUS specifically for digital telecommunications and data communication applications. The ST-BUS is a bus architecture which simplifies the system design by providing a common set of functional parameters which are used synonymously on all ST-BUS circuits.

Mitel Semiconductor is dedicated to providing a system solution to all communication applications. This is justified by our vertical integration of products which consists of our Telecom ICs and hybrid family as well as a full line of board and software products.

To support our total systems solution concept, Mitel Semiconductor strives to contribute through every phase of the project implementation. This ranges from early consultation on technical feasibility to providing tools for product conception as well as after-sales service support.

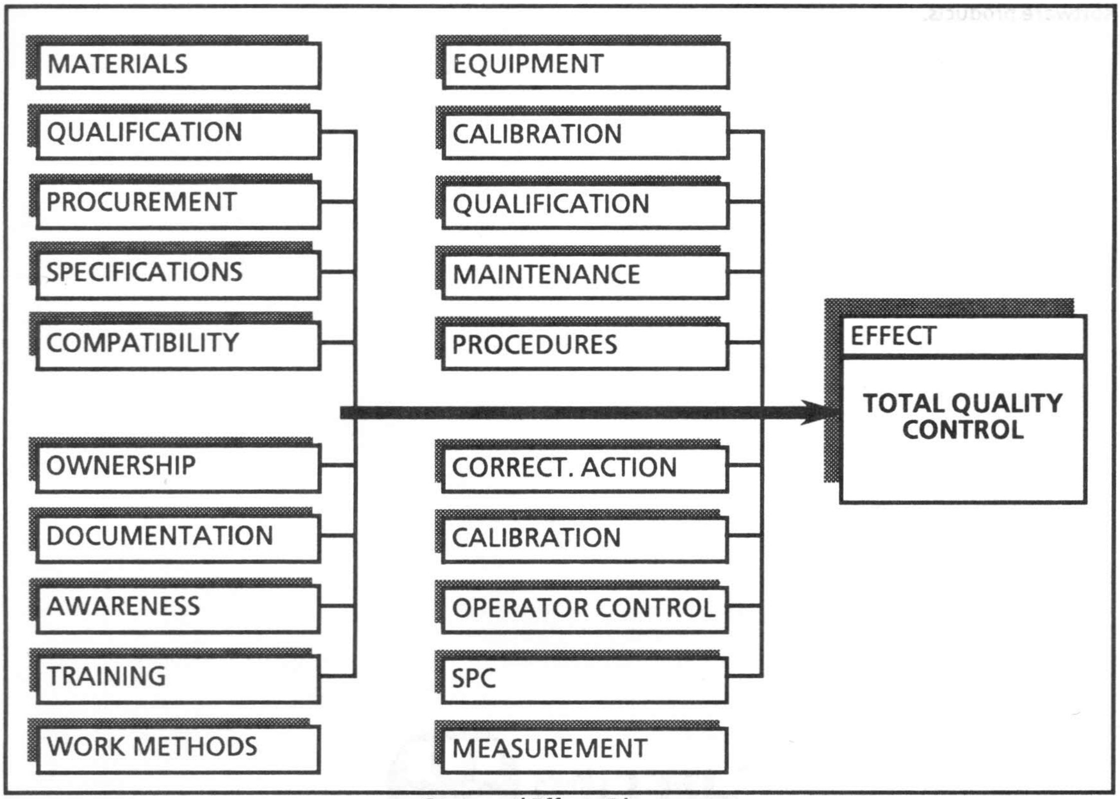
Mitel Semiconductor has helped to set several ISDN standards and in the process has become recognized as the predominant supplier of complete ISDN solutions. Our constant innovation in new product development, teamed with superior applications support gives you the Mitel advantage. Also, Mitel Semiconductor has made a substantial investment in the quality assurance process, with the result that all our customers receive a reliable product that meets or exceeds specifications every time.

Quality Assurance and Reliability

As we prepare to enter the 1990's, it is increasingly apparent that traditional Quality Control activities are not sufficient to protect both the customer's and Mitel Semiconductor's best interests. To supplement the next generation of Mitel devices, a Quality system that is capable of withstanding the rigors of ever evolving customer needs, customer-supplier relationships and contractual agreements must be established. It is no longer sufficient to subject product to quality control gates and hope that probability theory will prevail and defective product detected and removed prior to shipment to the customer. Increasingly lower defect rates are not only common within the industry, they are demanded by cost conscious consumers who recognize the attendant cost of supporting a vendor who cannot or will not control his process and reduce or eliminate defects. With this in mind, Mitel Semiconductor has initiated programs that when fully implemented, will provide the customer with a level of protection not easily achieved with traditional methods.

Leading the way in the quest for higher quality is the adoption of the Internation Standards Organization (ISO) 9000 or the American National Standards Institute (ANSI)/American Society for Quality Control (ASQC) Q90 series of Quality Systems. The principal objective of these systems is the achievement and sustaining of the customer's needs. With approval already granted to ISO 9001 (also known as British Standard (BS) 5750 in the United Kingdom) for the thick film hybrid facility and target dates of late 1990 for the integrated circuit facilities, Mitel Semiconductor is proceeding to establishing the foundation of a more efficient and effective quality management system.

In addition to the management system, progressive actions such as statistical process control (SPC) and design-of-experiments (focusing on Taguchi methods) will also yield significant return on investment, as the emphasis migrates from reaction or screening to a system of prevention. The implementation of a system of prevention will then allow for the ownership of quality to be transferred to the production floor, with defect rates no longer being controlled through Quality Control acceptance sampling.



Cause and Effects Diagram

The role of the Quality Assurance department is beginning to evolve from a policing authority to that of an audit or confirming position, serving to monitor the continued compliance to the processes and systems installed. The cause-and-effect diagram illustrated on the previous page simplifies the new tasks involved in Quality Assurance, identifying the departures from conventional techniques and the comprehensiveness of a total quality control system. From basics such as operator training and awareness, to proactive steps such as ensuring material compatibility and preventive maintenance, all areas are critical in ensuring that the desired effect is continually achieved.

In addition to these process oriented controls, effective development methodologies designed to establish conformance to requirements from the early stages in the product evolution cycle, comprehensive ESD programs and employee training in total quality control concepts (based upon the Philip Crosby quality system) also contribute to the integrity of the Mitel product that the customer receives.

At Mitel, it is recognized that all of these actions are required to continually supply customers with quality products and services. In addition, evolving customer requirements such as just-in-time and dock-to-stock programs leave absolutely no room for error on the part of the supplier. The product must be correct and defect free when received, to avoid production downtime, missed commitments and lost billings.

To illustrate the quality system installed at Mitel Semiconductor, and its results, two publications have been made available to customers. The first is a brochure entitled 'Delivering the Commitment'. It details the quality managements system, and outlines all manufacturing flows - including wafer processing, IC assembly and test, and hybrid manufacturing. The second manual is the 'Reliability Data Book', which is published annually and it contains valuable information such as data from accelerated stress testing on products detailed within this data book and detailed electrical and mechanical stress test data derived from the reliability monitor program. Encompassing steady state life, temperature humidity bias, and high accelerated stress testing (HAST), as well as mechanical testing such as temperature cycling, thermal shock, and vibration, most questions relating to the reliability of Mitel product can be found in this publication. To obtain a copy simply call the nearest Sales representative and identify the publication required. In addition, your name will be added to the mailing list to ensure that subsequent Quality News releases are sent to you.

At Mitel "Delivering the Commitment" is the stated quality goal, and only through the focus identified above will this goal be constantly achieved into the 1990's and beyond.

MITEL SEMICONDUCTOR

During the last decade, Mitel has participated in virtually all aspects of the semiconductor industry: as an innovative designer of telecommunications components and digital devices, as a pioneer of the ISO-CMOS process, and as a participant in the merchant components market. Increasingly, companies need to obtain custom and semi-custom devices to survive in today's highly competitive market. Mitel offers the following range of services and facilities to design engineers for co-operative production of custom and semi-custom devices.

Design

The Mitel wafer foundry accepts customer designs in the form of a database tape, Pattern Generation (PG) tape, or a set of photo-masks.

Mitel Semiconductor supplies design rules and electrical parameters to customers who have the resources to produce their own design tooling.

Full design services are available through design houses. Complete information about this service is available upon request.

Wafer Foundry

This state-of-the-art facility comprises:

- A 9,500 square foot wafer fab area consisting of class 100 clean room modules.
- A 5,000 square foot process development area.

The foundry currently processes silicon gate, P-well CMOS wafers in 5, 4, 3 and 2 micron geometries, and is compatible with a number of other major foundries. Double layer polysilicon is available on all processes, and there are a number of processes that can support double level metalizations.

A 9 micron metal gate CMOS process is offered for high voltage applications.

Fabrication equipment includes medium and high current implanters, plasma etching equipment, sputterers, projection alignment and direct step-on wafer. The foundry maintains tight parametric control and consistently achieves high yields.

Mask Making

In order to achieve optimum yields, and simplify the interface to the foundry, many customers find it convenient to have the Mitel photomask shop prepare the photomasks for their production requirements. The Mitel photomask shop uses optical pattern generation techniques to create high-quality projection master plates from GDS-1 or GDS-2 database tapes or Mann 3000, Mann 3600 and Emask 2000 PG tapes.

Device Testing

Mitel has available the following equipment for wafer probe and final testing of devices:

- LTX with DX89 or 90 and full DSP capability
- Fairchild Sentinel and Sentry VII
- Megatest Q2/62

Prototype Packaging

Mitel Semiconductor offers rapid turn-around on prototype packaging and supplies a complete choice of hermetic packages; Cerdip, Side-brazed DIP and Leadless Chip Carrier.

Mitel qualified subcontractors perform plastic packaging for prototyping or high volume assembly.

Customer Service

Mitel Semiconductor views customer service as being an important aspect of our wafer foundry business. The throughput commitment that Mitel measures itself against is a five week turnaround in wafer fabrication. Should photomask making be required, or wafer probing, an additional week would be required for each step.

Beyond this, the customer service group in Bromont, Quebec prides itself on the availability of timely information about the position and forecasted due-out date of foundry wafers. Whether by telephone or electronic mail, customers are kept well informed about the progress of their wafers as they move through the fabrication process.

CMOS Process Options

Several process options are available to customers at Mitel depending upon their needs. The process options listed in the following tables are given for guidance only. Many of the parameters can be adjusted to suit customer requirements. For full process specifications, contact a Mitel Sales Office or representative.

Gate Size: 5 micron, High Threshold

Parameter		N-Channel	P-Channel
Threshold Voltage	(volts @ 0μA)	0.6 - 1.2	0.6 - 1.2
Field Threshold	(Volts)	>18	>18
Breakdown Voltage BV_{dss}	(Volts)	>18	>18
K'	(μA/Volt^2)	26.0	10.0
Body Effect Coefficient	(Volt$^{\frac{1}{2}}$)	1.10	0.55
Effective Channel Length	(μm)	3.0	3.4
Gate Oxide Thickness	(Å)	800	800
Sheet Resistivity	(Ohms/square)	18 - 38	40 - 90
Polysilicon I Gate Resistivity	(Ohms/square)	14 - 26	14 - 26
Polysilicon II Resistivity	(Ohms/square)	30 - 80	30 - 80
Poly I to Poly II Capacitance	(10-4 pF/μm^2)	6.0	
Metal Width/Spacing	(μm)	5 / 5	
Second Layer Metal Option		None	
Process Compatibility		AMI	

Gate Size: 5 micron, Low Threshold

Parameter		N-Channel	P-Channel
Threshold Voltage	(volts @ 0μA)	0.4 - 0.9	0.4 - 0.9
Field Threshold	(Volts)	>18	>18
Breakdown Voltage BV_{dss}	(Volts)	>18	>18
K'	(μA/Volt^2)	26.0	10.0
Body Effect Coefficient	(Volt$^{\frac{1}{2}}$)	1.10	0.55
Effective Channel Length	(μm)	1.8	2.8
Gate Oxide Thickness	(Å)	800	800
Sheet Resistivity	(Ohms/square)	6 - 14	70 - 110
Polysilicon I Gate Resistivity	(Ohms/square)	14 - 26	14 - 26
Polysilicon II Resistivity	(Ohms/square)	30 - 80	30 - 80
Poly I to Poly II Capacitance	(10-4 pF/μm^2)	4.8	
Metal Width/Spacing	(μm)	5 / 5	
Second Layer Metal Option		None	
Process Compatibility		GTE, Plessey	

CMOS Process Options

Gate Size: 4 micron

Parameter		N-Channel	P-Channel
Threshold Voltage	(volts @ 0μA)	0.4 - 0.9	0.4 - 0.9
Field Threshold	(Volts)	>12	>12
Breakdown Voltage BV_{dss}	(Volts)	>15	>15
K'	(μA/Volt²)	32.0	13.0
Body Effect Coefficient	(Volt$^{\frac{1}{2}}$)	0.90	0.45
Effective Channel Length	(μm)	1.6	2.6
Gate Oxide Thickness	(Å)	640	640
Sheet Resistivity	(Ohms/square)	6 - 14	70 - 110
Polysilicon I Gate Resistivity	(Ohms/square)	14 - 26	14 - 26
Polysilicon II Resistivity	(Ohms/square)	30 - 80	30 - 80
Poly I to Poly II Capacitance	(10-4 pF/μm²)	4.8	
Metal Width/Spacing	(μm)	4 / 4	
Second Layer Metal Option		None	
Process Compatibility		GTE, Plessey	

Gate Size: 3 Micron

Parameter		N-Channel	P-Channel
Threshold Voltage	(volts @ 0μA)	0.6 - 1.0	0.6 - 1.0
Field Threshold	(Volts)	>12	>12
Breakdown Voltage BV_{dss}	(Volts)	>10	>10
K'	(μA/Volt²)	43.5	16.0
Body Effect Coefficient	(Volt$^{\frac{1}{2}}$)	0.43	0.53
Effective Channel Length	(μm)	2.4	2.2
Gate Oxide Thickness	(Å)	480	480
Sheet Resistivity	(Ohms/square)	20 - 35	80 - 120
Polysilicon I Gate Resistivity	(Ohms/square)	15 - 30	15 - 30
Polysilicon II Resistivity	(Ohms/square)	75 - 125	75 - 125
Poly I to Poly II Capacitance	(10-4 pF/μm²)	4.8	
Metal Width/Spacing	(μm)	3 / 3	
Second Layer Metal Option		Yes	
Process Compatibility		GTE, IMP	

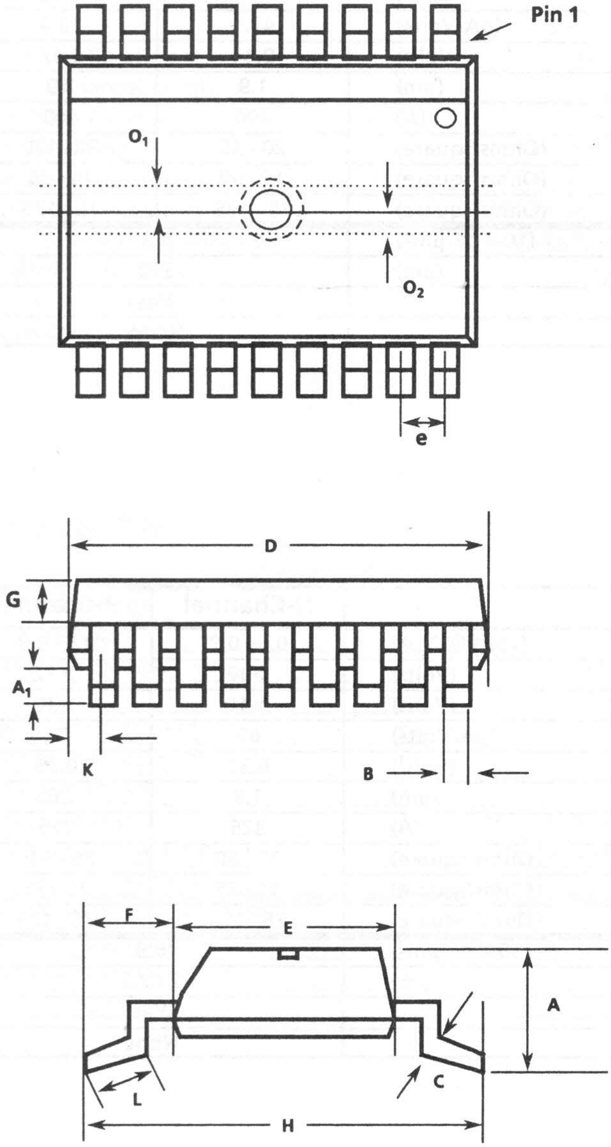
Gate Size: 2.5 Micron

Parameter		N-Channel	P-Channel
Threshold Voltage	(volts @ 0μA)	0.6 - 1.0	0.6 - 1.0
Field Threshold	(Volts)	>12	>12
Breakdown Voltage BV_{dss}	(Volts)	>10	>10
K'	(μA/Volt²)	47.5	12.4
Body Effect Coefficient	(Volt½)	0.44	0.47
Effective Channel Length	(μm)	1.9	1.9
Gate Oxide Thickness	(Å)	400	400
Sheet Resistivity	(Ohms/square)	20 - 35	80 - 120
Polysilicon I Gate Resistivity	(Ohms/square)	15 - 30	15 - 30
Polysilicon II Resistivity	(Ohms/square)	75 - 125	75 - 125
Poly I to Poly II Capacitance	(10-4 pF/μm²)	5.3	
Metal Width/Spacing	(μm)	3 /3	
Second Layer Metal Option		Yes	
Process Compatibility		None	

Gate Size: 2 micron

Parameter		N-Channel	P-Channel
Threshold Voltage	(volts @ 0μA)	0.5 - 0.9	0.5 - 0.9
Field Threshold	(Volts)	>12	>12
Breakdown Voltage BV_{dss}	(Volts)	>10	>10
K'	(μA/Volt²)	65	22
Body Effect Coefficient	(Volt½)	0.31	0.26
Effective Channel Length	(μm)	1.8	1.65
Gate Oxide Thickness	(Å)	325	325
Sheet Resistivity	(Ohms/square)	30 - 50	85 - 115
Polysilicon I Gate Resistivity	(Ohms/square)	15 - 25	15 - 25
Polysilicon II Resistivity	(Ohms/square)	75 - 125	75 - 125
Poly I to Poly II Capacitance	(10-4 pF/μm²)	6.9	
Metal Width/Spacing	(μm)	2 / 2.5	
Second Layer Metal Option		Yes	
Process Compatibility		None	

PACKAGING OUTLINES



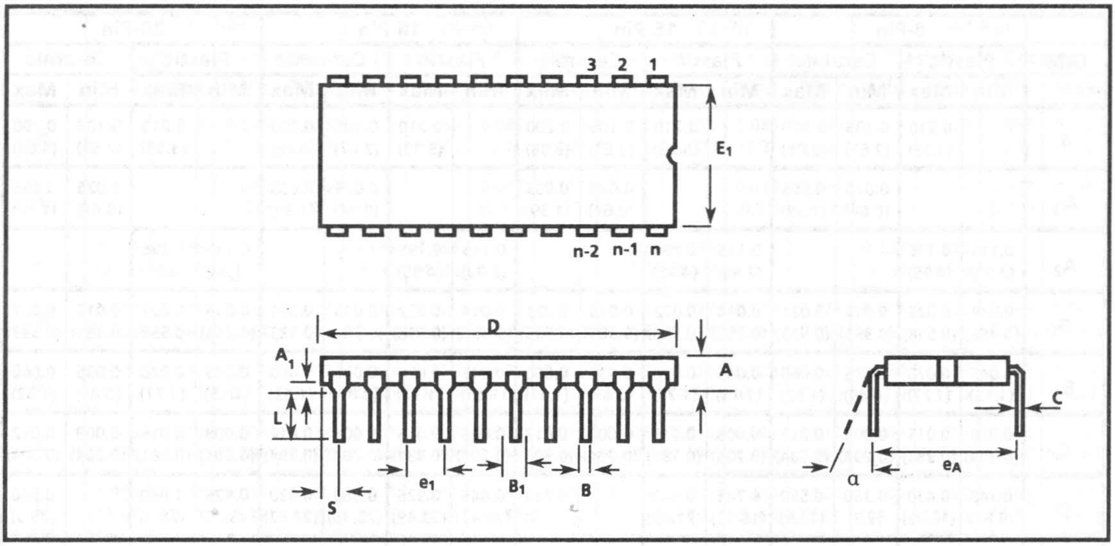
DIM	18-Pin SOIC		20-Pin SOIC	
	Min	Max	Min	Max
A	0.093 (2.35)	0.104 (2.65)	0.093 (2.35)	0.104 (2.65)
A_1	0.004 (0.10)	0.012 (0.30)	0.004 (0.10)	0.012 (0.30)
B	0.014 (0.351)	0.019 (0.488)	0.014 (0.351)	0.019 (0.488)
C	0.009 (0.231)	0.013 (0.318)	0.009 (0.231)	0.013 (0.318)
D	0.447 (11.35)	0.469 (11.90)	0.496 (12.60)	0.518 (13.00)
E	0.291 (7.40)	0.305 (7.75)	0.291 (7.40)	0.305 (7.75)
e	0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
F	0.044 (1.125)	0.064 (1.625)	0.044 (1.125)	0.064 (1.625)
G	0.040 (1.016)	0.050 (1.270)	0.040 (1.016)	0.050 (1.270)
H	0.394 (10.00)	0.419 (10.65)	0.394 (10.00)	0.419 (10.65)
K	0.035 (0.889)	0.045 (1.143)	0.035 (0.889)	0.045 (1.143)
L	0.016 (0.40)	0.050 (1.27)	0.016 (0.40)	0.050 (1.27)
O_1	-	0.005 (0.13)	-	0.005 (0.13)
O_2	-	0.005 (0.13)	-	0.005 (0.13)

NOTE: ( ) millimeters

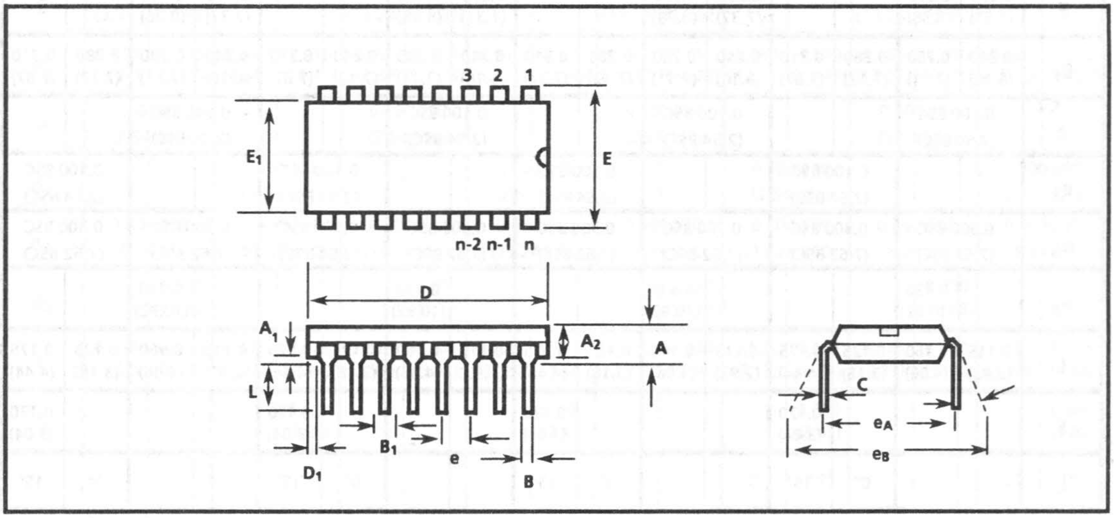
NOTES:

1) A & B Maximum dimensions include allowable mold flash.
2) O_1 & O_2 are SYMMETRY dimensions.

Lead SOIC Package (S Suffix)



Ceramic Dual-In-Line Packages (CDIP) - C Suffix



Plastic Dual-In-Line Packages (PDIP) - E Suffix

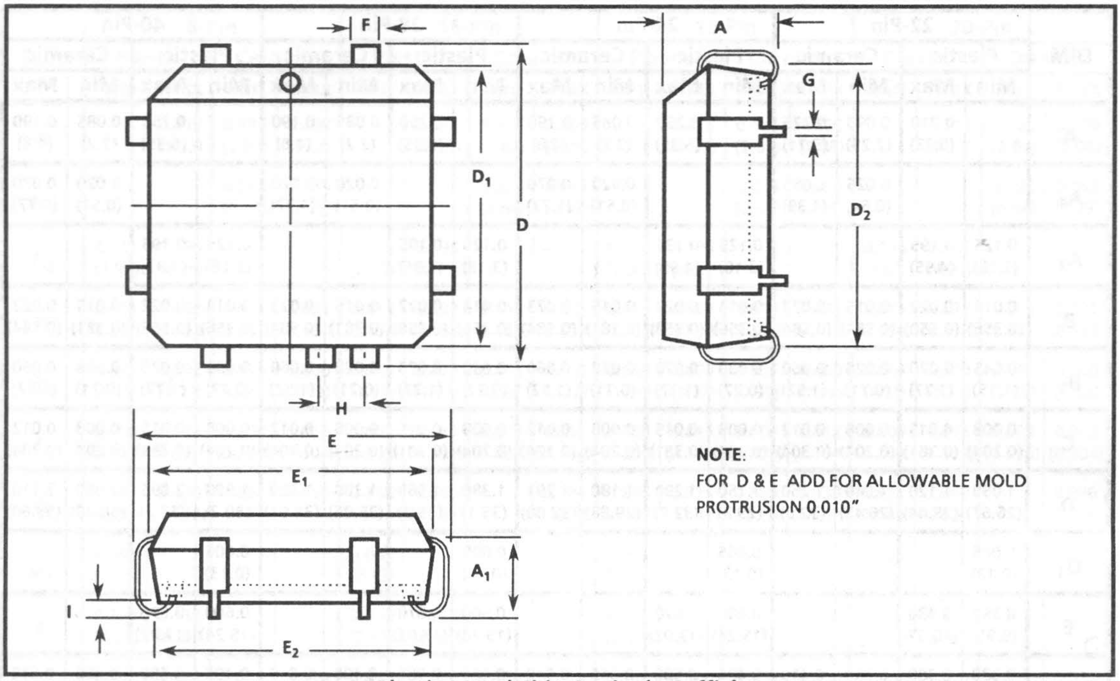
Package Outlines

DIM	8-Pin				16-Pin				18-Pin				20-Pin			
	Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)		0.210 (5.33)	0.105 (2.67)	0.200 (5.08)
A_1			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)			0.025 (0.64)	0.055 (1.39)
A_2	0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)			0.115 (2.93)	0.195 (4.95)		
B	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.021 (0.533)
B_1	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)	0.045 (1.15)	0.070 (1.77)	0.035 (0.89)	0.060 (1.52)
C	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)
D	0.348 (8.84)	0.430 (10.92)	0.380 (9.7)	0.550 (13.9)	0.745 (18.93)	0.840 (21.33)		0.784 (19.9)	0.845 (21.47)	0.925 (23.49)	0.880 (22.36)	0.930 (23.62)	0.925 (23.49)	1.060 (26.9)		0.996 (25.3)
D_1	0.005 (0.13)				0.005 (0.13)				0.005 (0.13)				0.005 (0.13)			
E	0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)			0.290 (7.37)	0.330 (8.38)		
E_1	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)	0.240 (6.10)	0.280 (7.11)	0.280 (7.12)	0.310 (7.87)
e	0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)			
e_1			0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)	
e_A	0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (2.54 BSC)		0.300 BSC (7.62 BSC)		0.300 BSC (7.62 BSC)	
e_B		0.430 (10.92)				0.430 (10.92)				0.430 (10.92)				0.430 (10.92)		
L	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)
S				0.120 (3.04)				0.120 (3.04)				0.120 (3.04)				0.120 (3.04)
α			0°	15°			0°	15°			0°	15°			0°	15°

NOTE: ( ) Millimeters

DIM	22-Pin				24-Pin				28-Pin				40-Pin			
	Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic		Plastic		Ceramic	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A		0.210 (5.33)	0.090 (2.29)	0.225 (5.71)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)		0.250 (6.35)	0.085 (2.2)	0.190 (4.8)
A_1			0.025 (0.64)	0.055 (1.39)			0.020 (0.51)	0.070 (1.77)			0.020 (0.51)	0.070 (1.77)			0.020 (0.51)	0.070 (1.77)
A_2	0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)			0.125 (3.18)	0.195 (4.95)		
B	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)	0.014 (0.356)	0.022 (0.558)	0.015 (0.381)	0.023 (0.584)
B_1	0.045 (1.15)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)	0.030 (0.77)	0.070 (1.77)	0.028 (0.71)	0.060 (1.52)
C	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)	0.008 (0.204)	0.015 (0.381)	0.008 (0.204)	0.012 (0.304)
D	1.050 (26.67)	1.120 (28.44)	1.040 (26.42)	1.260 (32.0)	1.150 (29.3)	1.290 (32.7)	1.180 (29.88)	1.291 (32.80)	1.380 (35.1)	1.565 (39.7)	1.380 (35.06)	1.520 (38.61)	1.980 (50.3)	2.095 (53.2)	1.980 (50.30)	2.110 (53.60)
D_1	0.005 (0.13)				0.005 (0.13)				0.005 (0.13)				0.005 (0.13)			
E	0.390 (9.91)	0.430 (10.92)			0.600 (15.24)	0.670 (17.02)			0.600 (15.24)	0.670 (17.02)			0.600 (15.24)	0.670 (17.02)		
E_1	0.330 (8.39)	0.380 (9.65)	0.350 (8.89)	0.410 (10.41)	0.485 (12.32)	0.580 (14.73)	0.516 (13.11)	0.610 (15.49)	0.485 (12.32)	0.580 (14.73)	0.480 (12.19)	0.610 (15.49)	0.485 (12.32)	0.580 (14.73)	0.480 (12.19)	0.618 (15.70)
e	0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)			
e_1			0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)				0.100 BSC (2.54 BSC)	
e_A	0.400 BSC (10.16 BSC)		0.400 BSC (10 .16 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)		0.600 BSC (15.24 BSC)	
e_B		0.500 (12.70)				0.700 (17.78)				0.700 (17.78)				0.700 (17.78)		
L	0.115 (2.93)	0.160 (4.06)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)	0.115 (2.93)	0.200 (5.08)	0.125 (3.18)	0.175 (4.44)
S				0.120 (3.04)				0.100 (2.54)				0.800 (2.05)				0.800 (2.05)
α			0°	15°			0°	15°			0°	15°			0°	15°

NOTE: ( ) Millimeters



Plastic J-Lead Chip Carrier (P-Suffix)

DIM	20-Pin PLCC		28-Pin PLCC		44-Pin PLCC		68-Pin PLCC		84-Pin PLCC	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.180 (4.57)	0.165 (4.20)	0.200 (5.08)	0.165 (4.20)	0.200 (5.08)
A_1	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.120 (3.04)	0.090 (2.29)	0.130 (3.30)	0.090 (2.29)	0.130 (3.30)
B			0.020 TP (0.511 TP)							
B_1										
B_2										
D/E	0.385 (9.78)	0.395 (10.03)	0.485 (12.32)	0.495 (12.57)	0.685 (17.40)	0.695 (17.65)	0.985 (25.02)	0.995 (25.27)	0.185 (30.10)	1.195 (30.35)
D_1/E_1	0.350 (8.890)	0.356 (9.042)	0.450 (11.430)	0.456 (11.582)	0.650 (16.510)	0.656 (16.662)	0.950 (24.130)	0.958 (24.333)	1.150 (29.210)	1.158 (29.413)
D_2/E_2	0.290 (7.37)	0.330 (8.38)	0.390 (9.91)	0.430 (10.92)	0.590 (14.99)	0.630 (16.00)	0.890 (22.61)	0.930 (23.62)	1.090 (27.69)	1.130 (28.70)
D_4/E_4										
e			0.050 BSC (1.27 BSC)							
F	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)	0.026 (0.661)	0.032 (0.812)
G	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)	0.013 (0.331)	0.021 (0.533)
H	0.050 BSC (1.27 BSC)				0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)		0.050 BSC (1.27 BSC)	
h			0.040 BSC (1.02 BSC)							
h_1										
I	0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)		0.020 (0.51)	
L										
L_1										
R_1										

NOTE: ( ) Millimeters

Tube Quantities

PIN COUNT	DEVICE QUANTITY BY PACKAGE TYPE					
	PLASTIC DIP	PLCC	SOIC	CERDIP	LCC	SIDE BRAZE
8	50	-	-	-	-	-
16	25	-	-	24	-	-
18	21	-	41	20	-	-
20	18	-	37	19	-	-
22	17	-	-	17	-	-
24	15	-	-	15	47	-
28	13	38	-	13	42	12
40	9	-	-	9	-	9
44	-	27	-	-	29	-
68	-	19	-	-	-	-
84	-	16	-	-	-	-

Standard IC Tube Quantity

Note: Standard IC shipping tube length is 50 cm ± 0.2 cm (19.75 in ± 0.08 in)

Ordering Information

Part Number Identification

Mitel Semiconductor products are identified by a prefix defining the product family, a device type designation number, a specification suffix, and a package suffix. The specification suffix defines variants of a particular device-type and its significance is described in the data sheet of the device concerned. The package suffix, which defines the package type, refers to drawings in the databook section "Package Outlines". The first page of each data sheet carries a section named "Ordering Information". This shows the full part number for each of the variants and package styles available for the device, and should be consulted to determine the correct part number for ordering purposes. A breakdown of a typical part number is shown below for reference.

Advance and Preliminary Data

Some data sheets carry the designation "Advance" or "Preliminary". Advance information represents the design objective for a device type in development and may be revised without notice before the device reaches production. Preliminary information is intended for design guidance purposes and refers to a device type in early production where device characterization is ongoing and information is still subject to change without notice. Current information on the status of Advance or Preliminary programs may be obtained from Mitel Sales Offices, Representatives, or Distributors.

Example:

MT 8804 A E ← **Package Suffix**

Family Prefix (MT)

- **MD** - Digital
- **MH** - Hybrid
- **MT** - Telecom
- **CM** - Module
- **MB** - Board
- **MS** - Software

Device Type (8804)

Specification Suffix (A)

Package Suffix (E)

- **C** -Ceramic Dual-in-line (Cerdip)
- **D** -Ceramic Dual-in-line (Side-braze)
- **E** -Plastic Dual-in-line
- **H** -Die in tray-pack
- **P** -Plastic J-lead chip carrier
- **W** -Probed die on wafer
- **Y** -Ceramic leadless chip carrier
- **S** - Small Outline Integrated Circuit

SMD Packages, Moisture Control and Solder Reflow

1.0 Introduction

The increasing use of surface mount devices (SMDs) such as plastic leaded chip carriers (PLCCs) and small outline integrated circuits (SOICs) in place of traditional through-hole soldered components has highlighted new reliability concerns.

The exposure of SMD packages to solder reflow assembly processes has revealed the following problems:

1. Moisture induced package cracking (also known as the "popcorn" effect)

2. Die and/or leadframe delamination leading to contamination traps or corrosion.

With advances in leadframe material construction (copper replacing Alloy-42 for improved thermal matching between leadframe and plastic); leadframe adhesion promoters (to improve plastic-to-leadframe bonding); leadframe design improvements (leadlock holes and die attach pad downsetting to create a single monolith instead of a top and bottom sandwich with the die and leadframe in between) and improved die top-coatings such as silicon nitride and spin-on-glass (SOG) delaminations, contamination, and corrosion problems are being kept in check.

However, because of the hygroscopic nature of plastic packaging materials, moisture induced package cracking continues to be a potential and costly problem, especially when the body and the leads of the SMD are exposed to wave or reflow soldering conditions. (If hand soldering or socketed circuit assembly is used then no potential moisture induced package cracking problems exist.)

An industry-wide long term solution to the moisture induced package cracking problem does not yet exist. Short term solutions include:

1. Identifying SMD package types and pin counts at highest risk.

2. Measuring absorbed moisture level thresholds for SMDs.

3. Performing a dehydration bake before soldering SMDs.

This bulletin describes the work Mitel Semiconductor has performed to identify high risk package types and pin counts and to determine the moisture thresholds for those SMD packages. Also included are details on how to perform a dehydration bake before soldering.

2.0 Moisture Sorption Characteristics

Moisture is absorbed from the environment by the plastic SMD and diffuses into the package according to Ficks diffusion law. Because there is a moisture diffusion gradient, the concentration and location of the moisture in the package is not known exactly; but the total amount of absorbed moisture can be calculated using:

(wet weight - initial weight) / initial weight x 100 = % weight absorbed.

The moisture desorption level obtained from dehydration baking can be similarly calculated using:

(initial weight - baked weight)/initial weight x 100 = % weight desorbed.

Moisture induced package cracking is affected by the:

1. Moisture absorption characteristics of the SMD.

2. SMD package cracking threshold level.

3. Temperature and humidity levels of the SMD environment.

4. Solder reflow process conditions.

The amount of moisture absorbed by the package is the dominating factor and can be measured and controlled to a limiting degree using dehydration bake by the user. The package cracking susceptibility level is a function of VLSI design and packaging technologies and can be measured by the user to provide comparison data for mixed SMD solder reflowing.

A. <u>Moisture Absorption by the SMD:</u>

Figure 1 shows data collected from the technical literature (1-5) and data collected for Mitel Semiconductor SMDs. Moisture absorption levels greater than 0.16-0.22% (by weight) are considered susceptible to package cracking during reflow soldering.

B. <u>SMD package cracking threshold level:</u>

Figure 2 combines die size and package base thickness to produce a "SAFE REGION" and a "CRACKING REGION" described by R. Lin (1,2). Mitel Semiconductor SMD data has been added to this graph in Figure 3. This data is useful in determining if a particular SMD is relatively more susceptible to cracking when compared to another

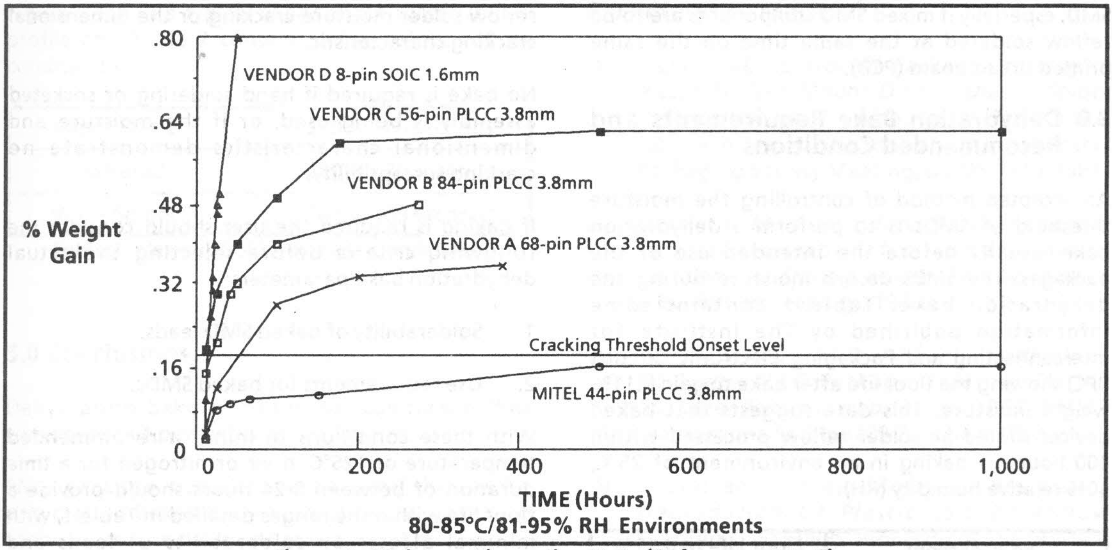


Figure 1. Moisture Absorption Data (References 1 to 5)

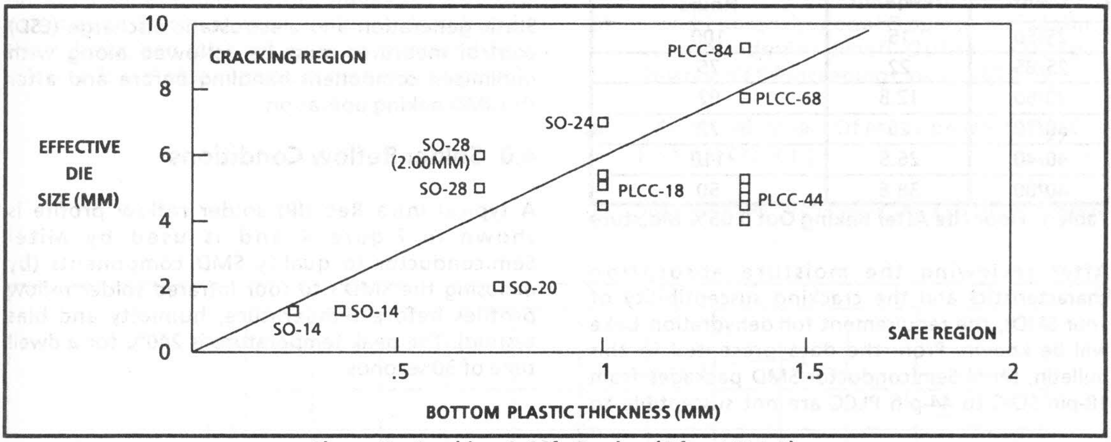


Figure 2. Cracking & Safe Region (After LIN 1,2)

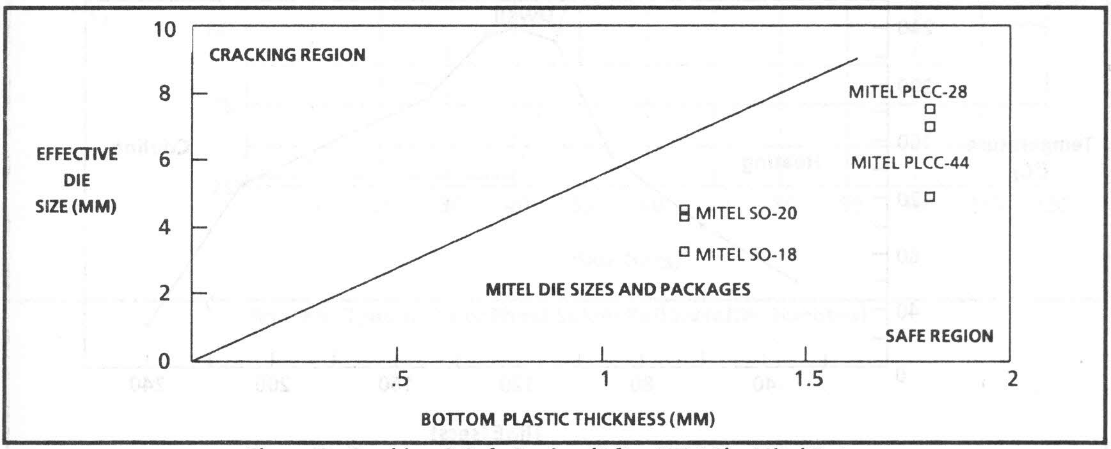


Figure 3. Cracking & Safe Region (After LIN 1,2) Mitel Data

SMD, especially if mixed SMD components are to be reflow soldered at the same time on the same printed circuit board (PCB).

3.0 Dehydration Bake Requirements and Recommended Conditions

An accepted method of controlling the moisture threshold of SMDs is to perform a dehydration bake, usually before the intended use of the packages. The SMDs desorb moisture during the dehydration bake. Table 1 contains some information published by The Institute for Interconnecting and Packaging Electronic Circuits (IPC) showing the floor life after bake to gain 0.11% weight moisture. This data suggests that baked devices should be solder reflow processed within 100 hours of baking in an environment of 25°C, 50% relative humidity (RH).

Environment		Floor Life to 0.11%
°C%RH	Dewpoint	Hours
25/50	15	100
25/85	22	75
30/60	12.8	92
30/70	25	72
40/40	26.5	110
40/80	38.6	50

Table 1: Floor Life After Baking Out 0.05% Moisture

After reviewing the moisture absorption characteristics and the cracking susceptibility of your SMDs, the requirement for dehydration bake will be known. From the data presented in this bulletin, Mitel Semiconductor SMD packages from 18-pin SOIC to 44-pin PLCC are not susceptible to reflow solder moisture cracking or the dimensional cracking characteristic.

No bake is required if hand soldering or socketed assembly is being used, or if the moisture and dimensional characteristics demonstrate no cracking susceptibility.

If baking is required the user should consider the following criteria before selecting the actual dehydration bake parameters:

1. Solderability of baked SMD leads.
2. Use requirements for baked SMDs.

With these conditions in mind, a recommended temperature of 125°C in air or nitrogen for a time duration of between 8-24 hours should provide a floor life within the ranges detailed in Table 1, with minimal affects on solderability of leads and provide adequate floor life.

Static generation and electrostatic discharge (ESD) control measures must be followed along with minimized component handling before and after the SMD baking operation.

4.0 Solder Reflow Conditions

A typical Infra Red (IR) solder reflow profile is shown in Figure 4 and is used by Mitel Semiconductor to qualify SMD components (by exposing the SMD's to four infrared solder reflow profiles before temperature, humidity and bias testing). The peak temperature is 240°C for a dwell time of 30 seconds.

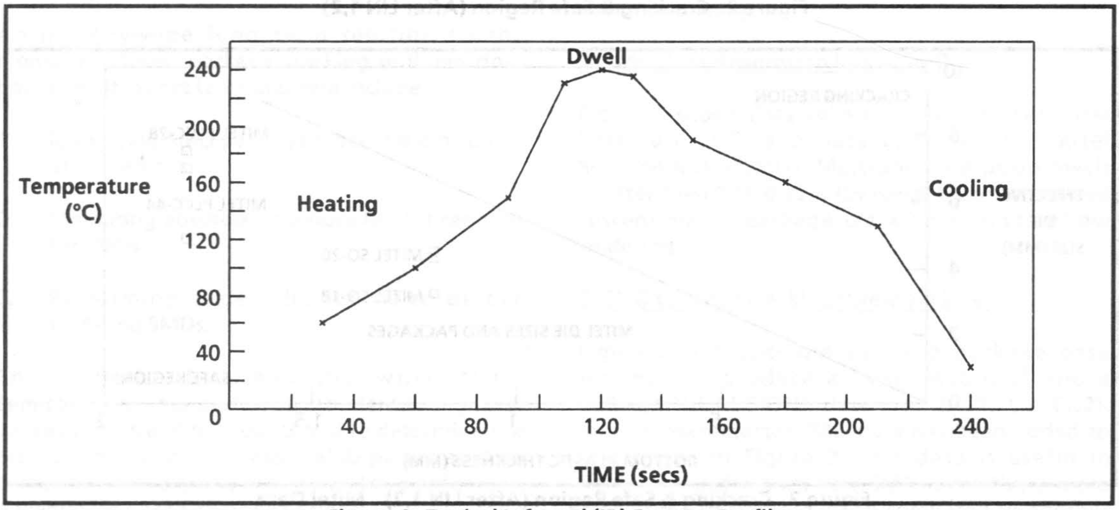


Figure 4. Typical Infrared (IR) Furnace Profile

Figure 5 shows a typical vapor phase solder reflow profile and Table 2 contains other solder reflow conditions.

Vapor Phase	220°C, 60 seconds
Infrared	240°C, 30 seconds
Wave Solder	260°C, 60 seconds

Table 2: Various Solder Reflow Conditions

5.0 Conclusions

Dehydration bake of Mitel Semiconductor SMD packages of 44 pins or less is not required.

SMD package sizes above 44 pins should be dehydration baked before solder reflow according to the procedure described above.

Mitel Semiconductor SMD packages can be dehydration baked at the conditions described in this bulletin, and the packages can withstand four solder reflow profile conditions detailed in Figure 4.

6.0 Reference Material

(1) R.Lin et al, *Control Of Package Cracking In Plastic Surface Mount Devices During Solder Reflow Process,* Proceedings of 7th Annual Conference Of International Electric Packaging Society Meeting, pp995-1010, 1987.

(2) R.Lin et al, *Moisture Induced Package Cracking In Plastic Encapsulated Surface Mount Components During Solder Reflow Process,* IEEE/IRPS Proceedings, 1988.

(3) Terry O.Steiner and David Suhl, *Investigations Of Large PLCC Package Cracking During Surface Mount Exposure,* IEEE/CHMT Transactions 10-2, pp209-216, June 1987.

(4) I.Fukuzawa et al, *Moisture Resistance Degradation Of Plastic LSIs By Reflow Soldering,* IEEE/IRPS Proceedings, pp192-197, 1985.

(5) Satoshi Ito et al, *Special Properties Of Molding Compounds For Small Outline Packaged Devices,* IEEE Proceedings, pp360-363, 1986.

(6) IPC-SM-786 Impact Of Moisture On Plastic IC Package Cracking.

(7) Signetics SMD Reliability Data Update - Section 4.

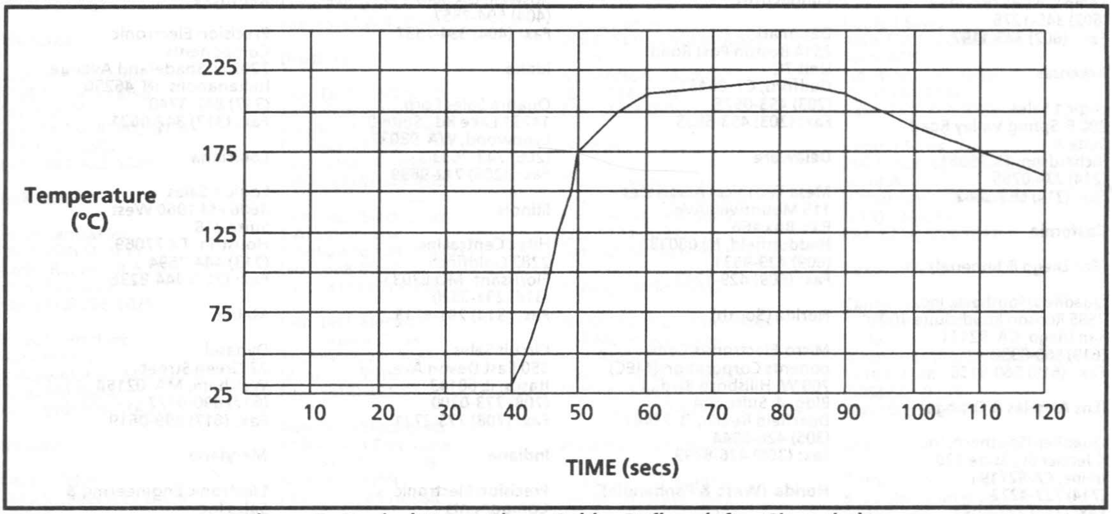


Figure 5. Typical Vapor Phase Solder Reflow (after Signetics)

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The Lyons Corporation
248 North State Street
Westerville, OH 43081
(614) 895-1447
Fax: (513) 278-3609

The Lyons Corporation
4615 W. Streetsboro Road
Richfield, OH 44286
(216) 659-9224
Fax: (216) 659-9227

Oklahoma

Logic 1 Sales
200 E. Spring Valley Road
Suite A
Richardson, TX 75081
(214) 234-0765
Fax: (214) 669-3042

Oregon

Quadra Sales Corp.
14231 Lake Rd., Suite B
Lynnwood, WA 98037
(206) 743-2633
Fax: (206) 742-9899

Pennsylvania (East)

Mesa Technical Associates
115 Mountwell Ave.
P.O. Box 466
Haddonfield, NJ 08033
(609) 429-9531
Fax: (609) 429-1242

Pennsylvania (West)

The Lyons Corporation
248 North State Street
Westerville, OH 43081
(614) 895-1447
Fax: (513) 278-3609

The Lyons Corporation
4615 W. Streetsboro Road
Richfield, OH 44286
(216) 659-9224

Rhode Island

Dynasel
22 Green Street
Waltham, MA 02154
(617) 890-6777

South Carolina

Godwin Associates
1100 Logger Court
Suite B102
Raleigh, NC 27609
(919) 878-8000
Fax: (919) 878-3923

Godwin Associates
3127 Eastway Dr., Suite 205
Charlotte, NC 28205
(704) 549-8500
Fax: (704) 532-2322

South Dakota

Tecteam Sales Inc.
3050 Metro Dr., Ste 301
Minneapolis, MN 55425
(612) 854-6616

Tennessee

Southern Component Sales, Inc.
307 Clinton Ave. E, Ste 413
Huntsville, AL 35801
(205) 533-6500
Fax: (205) 533-6578

Texas

Logic 1 Sales
11149 Research Blvd.
Austin, TX 78759
(512) 345-2952
Fax: (512) 346-5309

Logic 1 Sales
4606 FM 1960 West
Suite 418
Houston, TX 77069
(713) 444-7594
Fax: (713) 444-8236

Logic 1 Sales
200 E. Spring Valley Road
Suite A
Richardson, TX 75081
(214) 234-0765
Fax: (214) 669-3042

Texas (West)

Cantec Sales, Inc.
5736 Osuna Rd. N.E.
Suite 11
Alburquerque, New Mexico
87109-2588
(505) 889-9165
Fax: (505) 889-9198

Utah

Gemini Electronics
8120 Sheridan Blvd.
Suite C-206
Arvada, CO 80003-6104
(303) 428-5600
Fax: (303) 428-5689

North American Representatives (cont'd.)

Vermont

Dynasel
22 Green Street
Waltham, MA 02154
(617) 890-6777
Fax: (617) 899-0619

Virginia

Electronic Engineering & Sales Inc.
235 Prince George St.
Annapolis, MD 21401
(301) 269-4234
Fax: (301) 269-6476

Washington

Quadra Sales Corp.
14231 Lake Rd., Suite B
Lynnwood, WA 98037
206-743-2633
Fax: (206) 742-9899

West Virginia

The Lyons Corporation
248 North State Street
Westerville, OH 43081
(614) 895-1447
Fax: (513) 278-3609

Wisconsin

Tecteam Sales Inc.
3050 Metro Dr.
Suite 301
Minneapolis, MN 55425
(612) 854-6616
Fax: (612) 854-8031

Circuit Sales
650 East Devon Ave.
Itasca, IL 60143
(708) 773-0200
Fax: (708) 773-2721

Wyoming

Gemini Electronics
8120 Sheridan Blvd.
Suite C-206
Arvada, CO 80003-6104
(303) 428-5600
Fax: (303) 428-5689

CANADA

Alberta

Deskin Sales
3504 78th Ave.
Edmonton, AL T6B 2X9
(403) 466-2106
Fax: (403) 468-3019
TWX: (610) 831-1660

Deskin Sales
Suite 502
609-14th Ave. N.W.
Calgary, AL T2N 2A1
(403) 270-4440
Fax: (403) 283-2491

British Columbia

Deskin Sales
8650 Cambie St.
Vancouver, BC V6P 6M6
(604) 324-8343
Fax: (604) 324-6965
TWX: (610) 922-5036

Manitoba

Deskin Sales
P.O.Box 173
Transcona, MAN R2C 2Z9
(0) Zenith 06009
(403) 466-2106
Fax: (204) 224-2084
TWX: (610) 821-7394

Ontario

Deskin Sales
155 Clayton Drive
Markham, ONT L3R 5T9
(416) 475-1412
Telex: 06-966559
Fax: (416) 474-9105
TWX: (610) 492-5113

Deskin Sales
6 Antares Dr., Suite 204
Nepean, ONT K2E 8A9
(613) 228-1201
TWX: (610) 421-3793
Fax: (613) 228-1499

Quebec

Deskin Sales
5656 Thimens Blvd.
Ville St. Laurent, PQ H4R 2K9
(514) 331-2860
Telex: 05-824838
TWX: (610) 421-37 93
Fax: (514) 331-8692

North American Distributors

UNITED STATES

Alabama

Jaco/QC, Inc.
6035 Atlantic Blvd., Suite J
Norcross, GA 30071
(404) 449-9508
Fax: (404) 449-0275

Arizona

Anthem Electronics
1555 W. 10th Place, Suite 101
Tempe, AZ 85281
(602) 966-6600
Fax: (602) 966-4826

Sterling Electronics Inc.
(Billing Address)
P.O. Drawer 20867
Phoenix, AZ 85036
(602) 437-5565
Fax: (602) 437-5588

Sterling Electronics Inc.
(Shipping Address)
3312 East Broadway Rd.
Phoenix, AZ 85040

Time Electronics
1301 West Geneva Drive
Tempe, AZ 85282
(602) 967-2000
Fax: (602) 967-5923

Arkansas

Jaco/QC Inc.
4251 Kellway Circle
Addison, TX 75264
(214) 733-4300

Time Electronics
330 Sovereign Court
St. Louis, MO 63011-4491
(314) 391-6444

Time Electronics
1876 Firman
Richardson, TX 75081
(214) 644-4644
Fax: (214) 644-6668

California

Anthem Electronics
9131 Oakdale Ave.
Chatsworth, CA 91311
818-700-1000
Fax: (818) 775-1302

Anthem Electronics
1 Oldfield Drive
East Irvine, CA 92718-9208
(714) 768-4444
Fax: (714) 380-4747

Anthem Electronics
1040 E. Brokaw Road
San Jose, CA 95131
(408) 453-1200
Fax: (408) 452-2281

Anthem Electronics
9369 Carroll Park Drive
San Diego, CA 92121
(619) 453-4871
Fax: (619) 546-7893

Anthem Electronics
580 Menlo Drive, Suite 8
Rocklin, CA 95677
(916) 624-9744

Almo Electronics
2107 N. First St., Suite 690
San Jose, CA 95110
(408) 436-8822
Fax: (408) 436-8928
TWX: (910) 328-6161

Almo Electronics
3017 South Daimler St.
Santa Ana, CA 92705-5812
(714) 757-0444
Fax: (714) 757-0410

Almo Electronics
5137 Clareton Drive, Ste. 200
Agoura Hills, CA 91301
(818) 991-3984
Fax: (818) 706-0549

Semi-Dice
10961 Bloomfield Drive
Los Alamitos, CA 90720
(213) 594-4631
TWX: (910) 341-7710

Time Electronics
370 South Crenshaw Blvd., Suite E-104
Torrence, CA 90503-1727
(213) 320-0880
Fax: (213) 320-6372

Time Electronics
1339 Moffett Park Dr.
Sunnyvale, CA 94086
(408) 734-9888
Fax: (408) 734-1719

Time Electronics
30343 Canwood St.
Suite 210
Agoura Hills, CA 91301
(818) 707-2890
Fax: (818) 707-3657

Counties in California

(Los Angeles & Kern)

Time Electronics
9751 Independence Street
Chatsworth, CA 91311
(818) 998-7200
Fax: (818) 998-0143

Jaco Electronics
2260 Townsgate Rd.
Westlake Village, CA 91361
(805) 495-9998
Fax: (805) 494-3864

(San Diego & Imperial)

Time Electronics
8525 Arjons Drive, Suite A
San Diego, CA 92126
(619) 586-1331
Fax: (619) 271-7011

Jaco Electronics
1541 Parkway Loop "D"
Tustin, CA 92680
(714) 258-9003
Fax: (714) 258-1909

(Orange)

Time Electronics
3002 Dow Ave., Suite 102
Tustin, CA 92680
(714) 669-0100
Fax: (714) 544-2526

Jaco Electronics
1541 Parkway Loop "D"
Tustin, CA 92680
(714) 258-9003
Fax: (714) 258-1909

North American Distributors (cont'd.)

Colorado

Anthem Electronics
373 Inverness Drive, South
Englewood, CO 80112
(303) 790-4500
Fax: (303) 790-4532

Time Electronics
7399 South Tucson Way
Englewood, CO 80112
(303) 799-8851
Fax: (303) 799-0012

Connecticut

Jaco Electronics
384 Pratt Street
Meriden, CT 06450
(203) 235-1422
Fax: (203) 634-4884

Delaware

Mid-Atlantic Electronics
Interstate Industrial Park
Kor-Center East H-1
Bellmawr, NJ 08031
(609) 931-5305
Fax: (609) 931-4928

District of Columbia

Time Electronics
9051 Red Branch Road
Columbia, MD 21045
(301) 964-3090
Fax: (301) 964-9274

Jaco Electronics
10270 Old Columbia Rd.
Columbia, MD 21046
(301) 995-6620
Fax: (301) 995-6032

Florida

Jaco Electronics
1060 Holland Dr., Suite 3K
Boca Raton, FL 33487
(407) 241-7943
Fax: (407) 241-7950

Time Electronics
4203 Vineland Rd. K-7
Orlando, FL 32811
(407) 841-6565
Fax: (407) 648-0814

Georgia

Jaco/QC, Inc.
6035 Atlantic Blvd, Suite J
Norcross, GA 30071
(404) 449-9508
Fax: (404) 449-0275

Idaho

Anthem Electronics
19017-120th Ave. N.E.
Suite 102
Bothell, WA 98011
(206) 483-1700
Fax: (206) 486-0571

Time Electronics
8601 Willows Road, N.E.
Redmond, WA 98052
(206) 882-1600
Fax: (206) 883-1158

Illinois

Classic Components
3336 Commercial
Northbrook, IL 60062
(708) 272-9650
TWX: (910) 686-4783

Time Electronics
2000 Algonquin Rd.
Schaumburg, IL 60173
(708) 303-3000
Fax: (708) 303-3030

Illinois (South)

Time Electronics
330 Sovereign Court
St. Louis, MO 63011
(314) 391-6444

Indiana

Bell Industries
5230 West 79th St.
Indianapolis, IN 46268
(317) 875-8200

Bell Industries
3606 E. Maumee
Fort Wayne, IN 46801
(219) 423-3422

Iowa

Sterling Electronics
5000 West 78th Street
Minneapolis, MN 55435
(612) 831-2666
Twx: (910) 576-3135

Kansas

Time Electronics
330 Sovereign Court
St. Louis, MO 63011
(314) 391-6444

Sterling Electronics
9535 Alden St.
Lenexa, Kansas 66215
(913) 492-5406

Kentucky

Bell Industries
5230 West 79th St.
Indianapolis, IN 46268
(317) 875-8200

Bell Industries
3606 E. Maumee
Fort Wayne, IN 46801
(219) 423-3422

Louisiana

Jaco/QC, Inc.
1005 Industrial Blvd
Sugarland, TX 77478
(713) 240-2255

Time Electronics
1876 Firman
Richardson, TX 75081
(214) 644-4644
Fax: (214) 644-6668

Maine

Jaco Electronics
1053 East St.
Tewksbury, MA 01876
(508) 640-0010
Fax: (508) 640-0755

Time Electronics
10A Centennial Drive
Peabody, MA 01960
(508) 532-6200
Fax: (508) 596-7989

Maryland

Time Electronics
9051 Red Branch Road
Columbia, MD 21045
(301) 964-3090
Fax: (301) 964-9274

Jaco Electronics
10270 Old Columbia Road
Columbia, MD 21046
(301) 995-6620
Fax: (301) 995-6032

Massachusetts

Jaco Electronics
1053 East St.
Tewksbury, MA 01876
(508) 640-0010
Fax: (508) 640-0755

Time Electronics
10A Centennial Drive
Peabody, MA 01960
(508) 532-6200
Fax: (508) 596-7989

Michigan

Time Electronics
945 N. Edgewood Dr. Suite G
Wooddale, IL 60191
(708) 350-0610

Bell Industries
3981 Varsity Drive
Ann Arbor, MI 48106
(313) 971-9093

Minnesota

Sterling Electronics
5000 West 78th Street
Minneapolis, MN 55435
(612) 831-2666
Twx: (910) 576-3135

Time Electronics
945 N. Edgewood Drive
Suite G
Wooddale, IL 60191
(708) 350-0610

Mississippi

Jaco/QC, Inc.
6035 Atlantic Blvd., Suite J
Norcross, GA 30071
(404) 449-9508
Fax: (404) 449-0275

Missouri

Time Electronics
330 Sovereign Court
St. Louis, MO 63011-4491
(314) 391-6444

Montana

Time Electronics
7399 South Tucson Way
Englewood, CO 80112
(303) 799-8851
Fax: (303) 799-0012

Nevada

Anthem Electronics
1555 W. 10th Place, Suite 101
Tempe, AZ 85281
(602) 966-6600
Fax: (602) 966-4826

Sterling Electronics Inc.
3312 East Broadway Road
Phoenix, AZ 85282
(602) 268-2121
Fax: (602) 437-5588

Nevada (North)

Time Electronics
1339 Moffet Park Drive
Sunnyvale, CA 94086
(408) 734-9888
Fax: (408) 734-1719

New Hampshire

Jaco Electronics
1053 East St.
Tewksbury, MA 01876
(508) 640-0010
Fax: (508) 640-0755

Time Electronics
10A Centennial Drive
Peabody, MA 01960
(508) 532-6200
Fax: (508) 596-7989

New Jersey

Mid-Atlantic Electronics
Interstate Industrial Park
Kor-Center East H-1
Bellmawr, NJ 08031
(609) 931-5305
Fax: (609) 931-4928

Jaco Electronics
110 Green Rail Ave.
Wayne, NJ 07470
(201) 904-9510
Fax: (201) 904-9521

Time Electronics
70 Marcus Blvd
Hauppauge, NY 11788
(516) 273-0100
Fax: (516) 273-0136

New Mexico

Time Electronics
1301 West Geneva Drive
Tempe, AZ 85282
(602) 967-2000
Fax: (602) 967-5923

North American Distributors (cont'd.)

New York

Time Electronics
70 Marcus Blvd.
Hauppauge, NY 11788
(516) 273-0100
Fax: (516) 273-0136

ACI Electronics
200 Newtown Road
Plainview, NY 11803
(516) 293-6630
TWX: 510-224-6550
Fax: (516) 293-5192

Jaco Electronics
145 Oser Avenue
Hauppauge, NY 11788
(516) 273-5500
Fax: (516) 273-5528

Upstate New York

Time Electronics
7010 Fly Rd.
East Syracuse, NY 13057
(315) 432-0355
Fax: (315) 432-8147

North Carolina

Jaco/QC, Inc.
3029-107 Stonybook Drive
Raleigh, NC 27604
(919) 876-7767
Fax: (919) 876-6964

Time Electronics
9800-L Southern Pine Blvd.
Charlotte, NC 28210
(704) 522-7600
Fax: (704) 527-3860

North Dakota

Sterling Electronics
5000 West 78th Street
Minneapolis, MN 55435
(612) 831-2666
TWX: (910) 576-3135

Time Electronics
945 N. Edgewood Dr.
Suite 6
Wooddale, IL 60191
(312) 350-0610

Ohio

Bell Industries
446 Windsor Park Drive
Dayton, OH 45459
(513) 435-8660

Bell Industries
3606 E. Maumee
Fort Wayne, IN 46801
(219) 423-3422

Time Electronics
945 N. Edgewood Drive
Suite G
Wooddale, IL 60191
(312) 350-0610

Advacom Inc.
5620 West Road
McKean, PA 16426
1-800-678-0512

Oklahoma

Jaco, QC, Inc.
3158 S. 108th East Ave.
Suite 274
Tulsa, OK 74146
(918) 664-8812

Time Electronics
330 Sovereign Court
St. Louis, MO 63011-4491
(314) 391-6444

Time Electronics
1876 Firman
Richardson, TX 75081
(214) 644-4644
Fax: (214) 644-6668

Oregon

Anthem Electronics
9090 S.W. Gemini Dr.
Beaverton, OR 97005
(503) 643-1114
Fax : (503) 626-7928

Time Electronics
15688 S.W. 72nd Ave.,
Portland, OR 97224-7743
(503) 684-3780
Fax: (503) 684-5523

Pennsylvania (East)

Mid-Atlantic Electronics
Interstate Industrial Park
Kor-Center East H-1
Bellmawr, NJ 08031
(609) 931-5305

Pennsylvania (West)

Advacom Inc.
5620 West Road
McKean, PA 16426
1-800-678-0512

Advacom Inc.
5613R William Penn Hwy.
Export, PA 15632
(412) 733-5400

Rhode Island

Jaco Electronics
1053 East St.
Tewksbury, MA 01876
(508) 640-0010
Fax: (508) 640-0755

Time Electronics
10A Centennial Drive
Peabody, MA 01960
(508) 532-6200
Fax: (508) 596-7989

South Carolina

Jaco/QC, Inc.
3029-107 Stonybrook Dr.
Raleigh, NC 27604
(919) 876-7767
Fax: (919) 876-6964

Time Electronics
9800-L Southern Pine Blvd.
Charlotte, NC 28210
(704) 522-7600

South Dakota

Sterling Electronics
5000 West 78th Street
Minneapolis, MN 55435
(612) 831-2666
TWX: (910) 576-3135

Time Electronics
7667 Cahill Rd.
Edina, MN 55435
(612) 835-1250

Tennessee

Jaco/QC, Inc.
6035 Atlantic Blvd., Suite J
Norcross, GA 30071
(404) 449-9508
Fax: (404) 449-0275

Texas

Jaco/QC, Inc.
4251 Kellway Circle
Addison, TX 75264
(214) 733-4300

Jaco/QC, Inc.
2120M West Braker Lane
Austin, TX 78758
(512) 835-0220

Jaco/QC, Inc.
1005 Industrial Blvd.
Sugarland, TX 77478
(713) 240-2255

Time Electronics
1876 Firman
Richardson, TX 75081
(214) 644-4644
Fax: (214) 644-6668

Utah

Anthem Electronics
1279 W. 2200 South, Suite A
Salt Lake City, UT 84119
(801) 973-8909
Fax: (801) 973-8555

Time Electronics
2446 Progress Drive
West Valley, UT 84119
(801) 973-8181

Vermont

Time Electronics
10A Centennial Drive
Peabody, MA 01960
(508) 532-6200
Fax: (508) 596-7989

Jaco Electronics
1053 East St.
Tewksbury, MA 01876
(508) 640-0010
Fax: (508) 640-0755

Virginia

Jaco Electronics
10270 Old Columbia Rd.
Columbia, MD 21046
(301) 995-6620
Fax: (301) 995-6032

Time Electronics
9051 Red Branch Road
Columbia, MD 21045
(301) 964-3090
Fax: (301) 964-9274

Washington

Anthem Electronics
19017-120th Ave. N.E.
Suite 102
Bothell, WA 98011
(206) 483-1700
Fax: (206) 486-0571

Time Electronics
8601 Willows Road, N.E.
Redmond, WA 98052
(206) 882-1600
Fax: (206) 883-1158

Wisconsin

Classic Components
2925 S. 160th Street
New Berlin, WI 53151
(414) 786-5300

Wyoming

Time Electronics
7399 South Tucson Way
Englewood, CO 80112
(303) 799-8851
Fax: (303) 799-0012

North American Distributors (cont'd.)

CANADA

Alberta

Deskin Sales
3504 78th Avenue
Edmonton, AL T6B 2X9
(403) 466-2106
TWX: (610) 831-1660
Fax: (403) 468-3019

Deskin Sales
609-14th Ave. N.W.
Suite 502
Calgary, Alberta T2N 2A1
(403) 270-4440
Fax: (403) 283-2491

British Columbia

Deskin Sales
8650 Cambie Street
Vancouver, B.C. V6P 6M6
(604) 324-8343
TWX: (610)922-5036
Fax: (604) 324-6965

Manitoba

Deskin Sales
P.O. Box 173
Transcona, MAN. R2C 2Z9
(0) Zenith 06009
(403) 466-2106
TWX: (610) 821-7394
Fax: (204) 224-2084

Ontario

Deskin Sales
155 Clayton Drive
Markham, ONT.
L3R 5T9
(416) 475-1412
Telex: 06-966559
TWX: (610) 492-5113
Fax: (416) 474-9105

Deskin Sales
6 Antares Dr., Suite 204
Nepean, Ontario
K2E 8A9
(613) 228-1201
TWX: (610) 421-3793
Fax: (613) 228-1499

Quebec

Deskin Sales
5656 Thimens Blvd.
Ville St. Laurent, P.Q.
H4R 2K9
(514) 331-2860
TWX: (610) 421-3793
Telex: 05-824838
Fax: (514) 331-8692

International Distributors/Representatives

Argentina

YEL S.R.L.
Cangallo 1454, Piso 8 of.41
(1037) Buenos Aires,
Argentina
Phone:1-440-1532
Telex: 18605
Fax: 1-440-1533

Australia

George Brown & Co. Pty. Ltd.
(also known as George
Brown Group)
Locked Bag 29,
P.O. Rydalmere NSW 2116
Australia
Shipping Address:
Unit 1, 38 South Street
Rydalmere NSW 2116
Phone: 61 (2) 638-1999
Fax: 61 (2) 638-1798
Telex: AA 121732

Brasil

Hastec Assessoramento
Tecnicoe Representacoes
LTDA
R. Ferreira Do Alentejo 90
04728 - Sao Paulo - SP- Brasil
Phone: (11) 522-1799
Telex: (11) 60890 HAVN BR
Fax: (11) 247-9524

China

Chinam Associates Ltd.
Block C-1, 12th Floor
Hong Kong Industrial Centre
491 Castle Peak Road
Kowloon, Hong Kong
Phone: 3 7441186
Telex: 37644 SPSHK HX
Fax: 3-7850582
Cable: SPEEDYHKG

Hong Kong

Draco International Ltd.
16/F, First Pacific Bank
Centre
51-57 Gloucester Rd.
Wanchai, Hong Kong
Phone: 852 866 9913
Fax: 852 861 3588
Telex: 80539 DRACO HX

India

Balcorp (India) Pvt. Ltd.
921 Maker Chambers V
Nariman Point
Bombay 40002, India
Phone: 23-03-19
Fax: to Montreal Office
(514) 939-0777
Attn: Baljit Chadha
Telex: 81-112009 BIPL-IN

Indonesia

P.T. Centronix
36, Matraman Raya
Jakarta 13150
Indonesia
Phone: 8581187
Telex: 48216 CENT IA
Fax: 880 11 6221

Israel

Gallium Electronics
5 Ussishkin Street
P.O.B. 1379
Ramat-Hasharon 47100,
Israel
Phone: 972 3 5402242
Fax: 972 3 5402425

Japan

Tokyo Electron Limited
Semiconductor Sales Dept.
EC-2 Division,
P.O. Box 7006 Shinjuku
Monolith,
3-1 Nishi-Shinjuku 2-Chome
Shinjuku-Ku, Tokyo 163
Japan
Phone: +81-3-340-8257
Fax: +81-3-340-8402
Telex: J24291 LABTEL

Korea

Ellen & Company Inc.
1602-4, Shucho-1Dong
Shucho-Ku
Seoul 137-071, Korea
Phone: 822-587-5724
Fax: 011-822-585-1519

Sung-Ill Trading Co.
Room 814, Jae-Ill Bldg.
44-35 Yeouido-Dong
Seoul, Korea
Phone: 02-782-4905-4906
Fax: 02-785-3879

New Zealand

George Brown & Co. Pty. Ltd.
(also known as George
Brown Group)
Locked Bag 29,
P.O. Rydalmere NSW 2116
Australia
Phone: 61 (2) 638-1999
Fax: 61 (2) 638-1798
Telex: AA 121732

Pakistan

Makkays High-Tech Systems
Kulsum Plaza
42 Blue Area
Islamabad, Pakistan
Phone: (051) 828831
Fax: (051) 820888

Singapore

DOS Electronis Pte Ltd.
Block 6001,
Bedok Reservoir Rd.
Bedok Industrial Park C
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ANALOG SWITCHES

2

MITEL®

CMOS **MT8804A**

8 × 4 Analog Switch Array

9161-002-124-NA ISSUE 2 October 1989

Features

- Microprocessor compatible control inputs
- On chip control memory and address decoding
- Row addressing
- Master reset
- 32 crosspoint switches in 8 × 4 array
- 5.0V to 15.0V operation
- Low crosstalk between switches
- Low on resistance: 90Ω (typ.) at 13V
- Matched switch characteristics
- Switches frequencies up to 40MHz

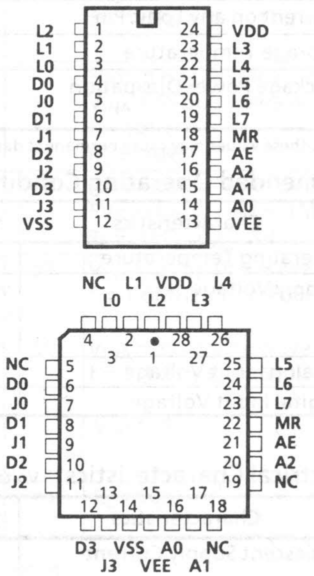
Applications

- PABX and key sytems
- Data acquisition systems
- Test equipment/instrumentation
- Analog/digital multiplexers

Description

The MT8804A is a CMOS/LSI 8×4 Analog Switch Array incorporating control memory (32 bits), decoder and digital logic level converters. This circuit has digitally controlled analog switches having very low "ON" resistance and very low "OFF" leakage current. Switches will operate with analog signals at frequencies to 40 MHz and up to 15.0Vp-p. A "HIGH" on the Master Reset input switches all channels "OFF" and clears the memory. This device is ideal for crosspoint switching applications.

Pin Connections



Ordering Information −40° to 85°C

MT8804AC	24 Pin CERDIP
MT8804AE	24 Pin PLASTIC DIP
MT8804AP	28 Pin PLCC

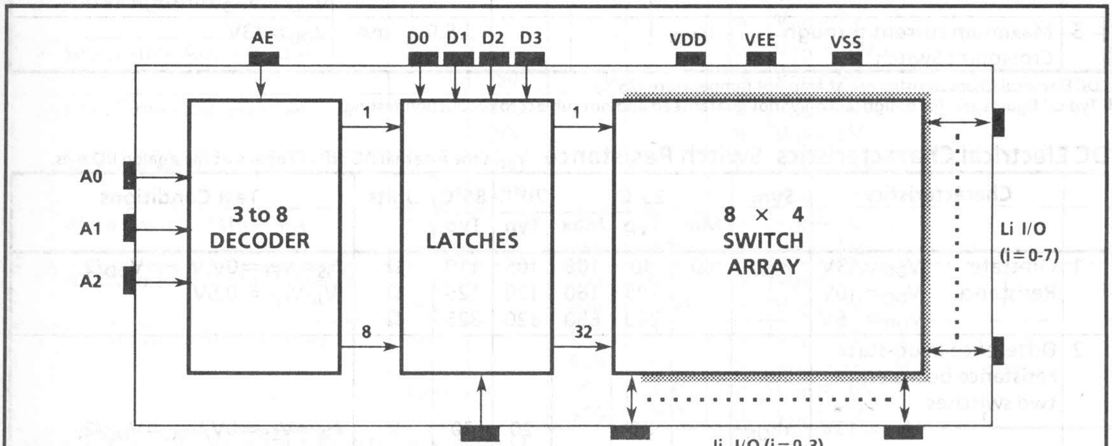


Figure 1- Functional Block Diagram

Absolute Maximum Ratings* - Voltages are with respect to V_{EE} unless otherwise stated.

	Parameter		Symbol	Min	Max	Units
1	Supply Voltage		V_{DD}-V_{SS} V_{DD}-V_{EE} V_{SS}-V_{EE}	-0.3 -0.3 -0.3	16 16 16	V V V
2	Analog Input Voltage		V_{INA}	V_{EE}-0.3	V_{DD}+0.3	V
3	Digital Input Voltage		V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
4	Current on any Logic Pin		I		10	mA
5	Storage Temperature		T_S	-65	+150	°C
6	Package Power Dissipation	PLASTIC DIP CERDIP	P_D P_D		0.6 1.2	W W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{EE} unless otherwise stated.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T_O	−40	25	85	°C	
2	Supply Voltage	V_{DD}-V_{SS} V_{DD}-V_{EE} V_{SS}-V_{EE}	5 5 0	5 10 5	15 15 10	V V V	
3	Analog Input Voltage	V_{INA}	V_{EE}		V_{DD}	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics† - Voltages are with respect to $V_{EE}=V_{SS}=0V$.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DD}		1	100	μA	$V_{DD}=15V$. All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}
2	Off-state Leakage Current (Any line to any junctor)	I_{OFF}		±0.1	±500	nA	$V_{DD}=13V$, Switch is 'Off' $\lvert V_{Ji}-V_{Lj}\rvert = V_{DD}-V_{EE}$
3	Input Logic "0" level	V_{IL}			3.0 1.5	V V	$V_{DD}=10V$ $V_{DD}=5V$ $V_{INA}=V_{DD}$ through 1kΩ
4	Input Logic "1" level	V_{IH}	7.0 3.5			V V	$V_{DD}=10V$ $V_{DD}=5V$ $V_{INA}=V_{DD}$ through 1kΩ
5	Maximum current through Crosspoint Switch	I_{MAX}			±8.0	mA	$V_{DD}=13V$

† DC Electrical Characteristics are at ambient temperature (25°C).
‡ Typical figures are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics- Switch Resistance - V_{DC} is the external DC offset applied at the analog I/O pins.

	Characteristics		Sym	25°C			70°C	85°C	Units	Test Conditions
				Min	Typ	Max	Typ	Typ		
1	On-state Resistance	$V_{DD}=13V$ $V_{DD}=10V$ $V_{DD}=5V$	R_{ON}	60	90 105 290	108 160 650	105 120 320	110 125 325	Ω Ω Ω	$V_{SS}=V_{EE}=0V, V_{DC}=V_{DD}/2$, $\lvert V_{Ji}-V_{Lj}\rvert = 0.6V$
2	Difference in on-state resistance between two switches	$V_{DD}=13V$ $V_{DD}=10V$	ΔR_{ON}		20 30		20 30	20 30	Ω Ω	$V_{SS}=V_{EE}=0V, V_{DC}=V_{DD}/2$, $\lvert V_{Ji}-V_{Lj}\rvert = 0.6V$

2

AC Electrical Characteristics† - Crosspoint Performance

-V_{DC} is the external DC offset applied at the analog I/O pins. Voltages are with respect to $V_{DD}=10V$, $V_{SS}=V_{EE}=0V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch Line Capacitance	C_{IS}		5		pF	
2	Switch Junctor Capacitance	C_{OS}		20		pF	
3	Feedthrough Capacitance	C_I		0.2		pF	
4	Frequency Response Channel "ON" $20LOG(V_{OUT}/V_{INA})=-3dB$	F_{3dB}		40		MHz	Switch is "ON"; $V_{DC}=5V$, $V_{INA}=5Vpp$ sinewave $f=1kHz$; $R_L=1k\Omega$
5	Total Harmonic Distortion $V_{DD}=15V/V_{DC}=7.5V$ $V_{DD}=10V/V_{DC}=5V$ $V_{DD}=5V/V_{DC}=2.5V$	THD		 0.1 0.2 1.0		 % % %	Switch is "ON"; $V_{EE}=V_{SS}=0V$ $V_{INA}=5Vpp$ sinewave $f=1kHz$; $R_L=10k\Omega$
6	Feedthrough Channel "OFF" Feed. $=20LOG(V_{OUT}/V_{INA})$	FDT		−50		dB	All Switches "OFF"; $V_{INA}=5Vpp$ sine wave $f=1MHz$; $R_L=1k\Omega$. $V_{DC}=5V$
7	Crosstalk between any two channels for switches Li−Ji and Lj−Jj. Li − Ji is "ON" Lj − Jj is "OFF" $Xtalk=20LOG(V_{Jj}/V_{Li})$.	X_{talk}		−40 −90		dB dB	$V_{INA}=2Vpp$ sine wave $f=1.0MHz$; $R_L=600\Omega$. $V_{INA}=2Vpp$ sine wave $f=3.4kHz$; $R_L=600\Omega$. $V_{DC}=5V$
8	Propagation delay through switch	t_{PS}		10		ns	$C_L=50pF$

† AC Electrical Characteristics are at ambient temperature (25°C).
‡ Typical figures are for design aid only; not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Control and I/O Timings

- Voltages are with respect to $V_{SS}=V_{EE}=0V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Digital Input Capacitance	C_{DI}		5		pF	$V_{DD}=10V$
2	Setup Time D0-D3 to AE	t_{DS}	150 200			ns ns	$V_{DD}=10V$ $V_{DD}=5V$
3	Hold Time D0-D3 to AE	t_{DH}	120 300			ns ns	$V_{DD}=10V$ $V_{DD}=5V$
4	Setup Time Address to AE	t_{AS}	0 50			ns ns	$V_{DD}=10V$ $V_{DD}=5V$
5	Hold Time Address to AE	t_{AH}	120 300			ns ns	$V_{DD}=10V$ $V_{DD}=5V$
6	AE Pulse Width	t_{AEW}	100 250			ns ns	$V_{DD}=10V$ $V_{DD}=5V$
7	AE to Switch Status Delay	t_{PAE}		200 650	300 900	ns ns	$V_{DD}=10V$ ① $V_{DD}=5V$ ①
8	DATA to Switch Status Delay	t_{PLH} t_{PHL}		250 650	400 1000	ns ns	$V_{DD}=10V$ ① $V_{DD}=5V$ ①
9	MR to Switch Status Delay	t_{MR} t_{MRR}		250 500 200 500	400 600 350 750	ns ns ns ns	$V_{DD}=10V$ ② $V_{DD}=5V$ ② $V_{DD}=10V$ ② $V_{DD}=5V$ ②

† AC Electrical Characteristics are at ambient temperature (25°C).
‡ Typical figures are for design aid only; not guaranteed and not subject to production testing.
① $R_L=10k\Omega$, $C_L=50pF$
② $R_L=1k\Omega$, $C_L=50pF$
Digital Input rise time (tr) and fall time (tf) = 5ns.

MEMORY RESET **MR**	ADDRESS ENABLE **AE**	ADDRESS			ADDRESSED LINE	INPUT DATA TO CONTROL MEMORY				JUNCTORS CONNECTED TO ADDRESSED LINE			
		A2	A1	A0		D3	D2	D1	D0	J3	J2	J1	J0
1	X	X	X	X	ALL	X	X	X	X	All Switches "OFF"			
0	0	X	X	X	NONE	X	X	X	X	No Change of State			
0	1	0	0	0	L0	0	0	0	0	●	●	●	●
0	1	0	0	0	L0	0	0	0	1	●	●	●	+
0	1	0	0	0	L0	0	0	1	0	●	●	+	●
0	1	0	0	0	L0	0	0	1	1	●	●	+	+
0	1	0	0	0	L0	0	1	0	0	●	+	●	●
0	1	0	0	0	L0	0	1	0	1	●	+	●	+
0	1	0	0	0	L0	0	1	1	0	●	+	+	●
0	1	0	0	0	L0	0	1	1	1	●	+	+	+
0	1	0	0	0	L0	1	0	0	0	+	●	●	●
0	1	0	0	0	L0	1	0	0	1	+	●	●	+
0	1	0	0	0	L0	1	0	1	0	+	●	+	●
0	1	0	0	0	L0	1	0	1	1	+	●	+	+
0	1	0	0	0	L0	1	1	0	0	+	+	●	●
0	1	0	0	0	L0	1	1	0	1	+	+	●	+
0	1	0	0	0	L0	1	1	1	0	+	+	+	●
0	1	0	0	0	L0	1	1	1	1	+	+	+	+
0	1	0	0	1	L1	0	0	0	0	●	●	●	●
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	0	0	1	L1	1	1	1	1	+	+	+	+
0	1	0	1	0	L2	0	0	0	0	●	●	●	●
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	0	1	0	L2	1	1	1	1	+	+	+	+
0	1	0	1	1	L3	0	0	0	0	●	●	●	●
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	0	1	1	L3	1	1	1	1	+	+	+	+
0	1	1	0	0	L4	0	0	0	0	●	●	●	●
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	1	0	0	L4	1	1	1	1	+	+	+	+
0	1	1	0	1	L5	0	0	0	0	●	●	●	●
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	1	0	1	L5	1	1	1	1	+	+	+	+
0	1	1	1	0	L6	0	0	0	0	●	●	●	●
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	1	1	0	L6	1	1	1	1	+	+	+	+
0	1	1	1	1	L7	0	0	0	0	●	●	●	●
↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
0	1	1	1	1	L7	1	1	1	1	+	+	+	+

Table 1 - Address Decode Truth Table

NOTES:
- 0 - Low Logic Level
- 1 - High Logic Level
- X - Don't Care Condition
- + - Indicates Connection Between Junctor and Addressed Line
- ● - Indicates No Connection Between Junctor and Addressed Line

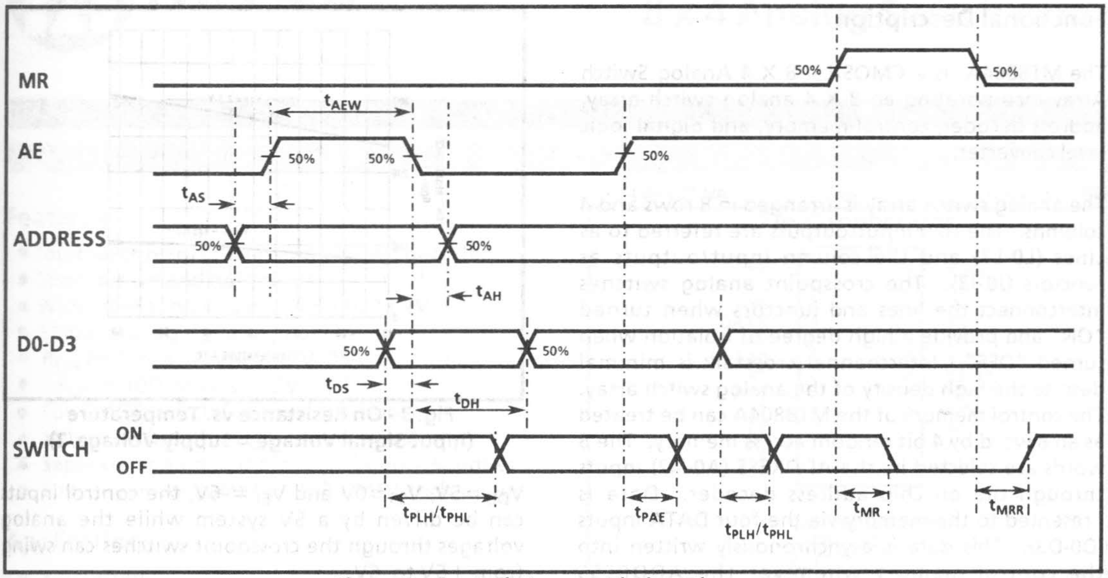


Figure 2 - Control Memory Timing Diagram

Pin Description

Pin #*	Name	Description
1-3	L2-L0	**L2-L0 Analog Lines (Inputs/Outputs):** these are connected to the L2-L0 columns of the switch array.
4	D0	**D0 Data (Input):** Active High.
5	J0	**J0 Analog Junctor (Input/Output):** this is connected to the J0 row of the switch array.
6	DI	**DI Data (Input).** Active High.
7	J1	**J1 Analog Junctor (Input/Output):** this is connected to the J1 row of the switch array.
8	D2	**D2 Data (Input):** Active High.
9	J2	**J2 Analog Junctor (Input/Output):** this is connected to the J2 row of the switch array.
10	D3	**D3 Data (Input):** Active High.
11	J3	**J3 Analog Junctor (Input/Output):** this is connected to the J3 row of the switch array.
12	V_{SS}	**Digital Ground Reference.**
13	V_{EE}	**Negative Power Supply.**
14-16	A0-A2	**A0-A2 Address Lines (Inputs).**
17	AE	**Address Enable/Strobe (Input):** enables function selected by address and data. Address must be stable before AE goes high and D0-D3 must be stable on the falling edge of the AE. Active High.
18	MR	**Master RESET (Input):** this is used to turn off all switches. Active High.
19-23	L7-L3	**L7-L3 Analog Lines (Inputs/Outputs):** these are connected to the L7-L3 columns of the switch array.
24	V_{DD}	**Positive Power Supply.**

* Plastic DIP and CERDIP only

Functional Description

The MT8804A is a CMOS/LSI 8 X 4 Analog Switch Array incorporating an 8 X 4 analog switch array, address decoder, control memory, and digital logic level converter.

The analog switch array is arranged in 8 rows and 4 columns. The row input/outputs are referred to as Lines (L0-L7) and the column input/outputs as Junctors (J0-J3). The crosspoint analog switches interconnect the lines and junctors when turned "ON" and provide a high degree of isolation when turned "OFF". Interchannel crosstalk is minimal despite the high density of the analog switch array. The control memory of the MT8804A can be treated as an 8 word by 4 bit random access memory. The 8 words are selected by the ADDRESS (A0-A2) inputs through the on chip address decoder. Data is presented to the memory via the four DATA inputs (D0-D3). This data is asynchronously written into the control memory whenever the ADDRESS ENABLE (AE) input is HIGH. A HIGH level written into a memory cell turns the corresponding crosspoint switch "ON" while a LOW level causes the crosspoint to turn "OFF".

Only the crosspoint switches corresponding to the addressed memory word are affected when data is written into the memory. The remaining switches retain their previous states. By establishing appropriate patterns in the control memory, any combination of lines and junctors may be interconnected. A HIGH level on the MASTER RESET (MR) input returns all memory locations to a LOW level and turns all crosspoint switches "OFF" effectively isolating the lines from the junctors. The digital logic level converters allow the digital input levels to differ from limits of the analog levels switched through the array. For example, with $V_{DD}=5V$, $V_{SS}=0V$ and $V_{EE}=-6V$, the control inputs can be driven by a 5V system while the analog voltages through the crosspoint switches can swing from +5V to -6V.

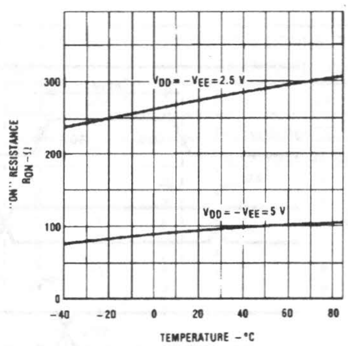


Fig. 3 - On Resistance vs. Temperature (Input Signal Voltage = Supply Voltage/2)

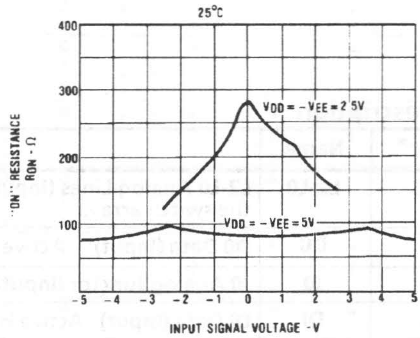


Fig. 4 - On Resistance vs. Input Signal Voltage

8 x 8 Analog/Digital Switch

Two MT8804's configured as shown, implement an 8 x 8 analog/digital switch. The switch capacity can be expanded to an M x N array of inputs/outputs. Expansion in the M dimension is as shown with the MT8804A lines (L0-L7) commoned. Expansion in the N dimension is accomplished by replicating the circuit shown and connecting the MT8804A junctors (J0-J3) in common. The address and data control inputs of the MT8804A's can be connected in common for any size and switch provided that the address enable (AE) inputs are driven individually. A particular signal path is connected by setting up the appropriate signals or the address and data lines and taking the corresponding address enable input high. The master reset (MR), when taken high, disconnects all signal paths.

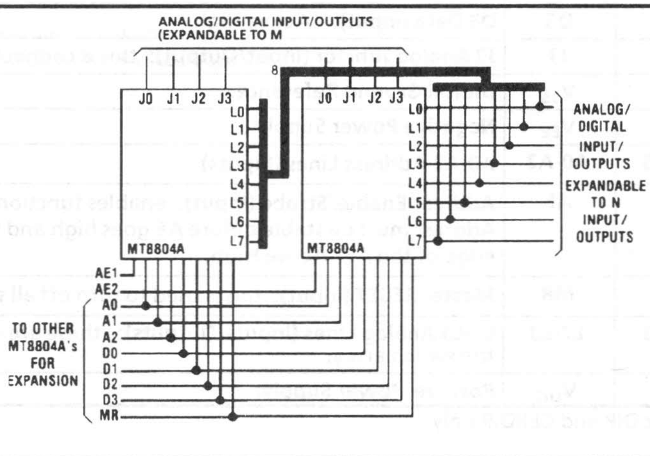


Fig. 5 - 8 x 8 Analog/Digital Switch

MITEL®

ISO-CMOS MT8806
8 x 4 Analog Switch Array

9161-002-097-NA ISSUE 2 November 1988

Features

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage: 4.5V to 13.2V
- 12Vpp analog signal capability
- R_{ON} 65Ω max. @ V_{DD}=12V, 25°C
- $\Delta R_{ON} \leq 10\Omega$ @ V_{DD}=12V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Separate analog and digital reference supplies
- Low power consumption ISO-CMOS technology

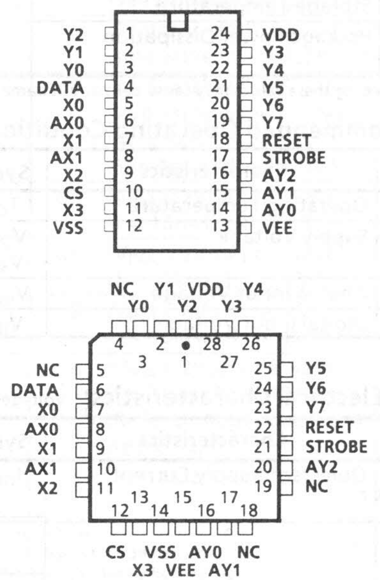
Applications

- Key systems
- PBX systems
- Mobile radio
- Test equipment /instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Description

The Mitel MT8806 is fabricated in MITEL's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8×4 array of crosspoint switches along with a 5 to 32 line decoder and latch circuits. Any one of the 32 switches can be addressed by selecting the appropriate five address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. V_{SS} is the ground reference of the digital inputs. The range of the analog signal is from V_{DD} to V_{EE}. Chip Select (CS) allows the crosspoint array to be cascaded for matrix expansion.

Pin Connections



Ordering Information −40° to 85°C

MT8806AC	24 Pin CERDIP
MT8806AE	24 Pin PLASTIC DIP
MT8806AP	28 Pin PLCC

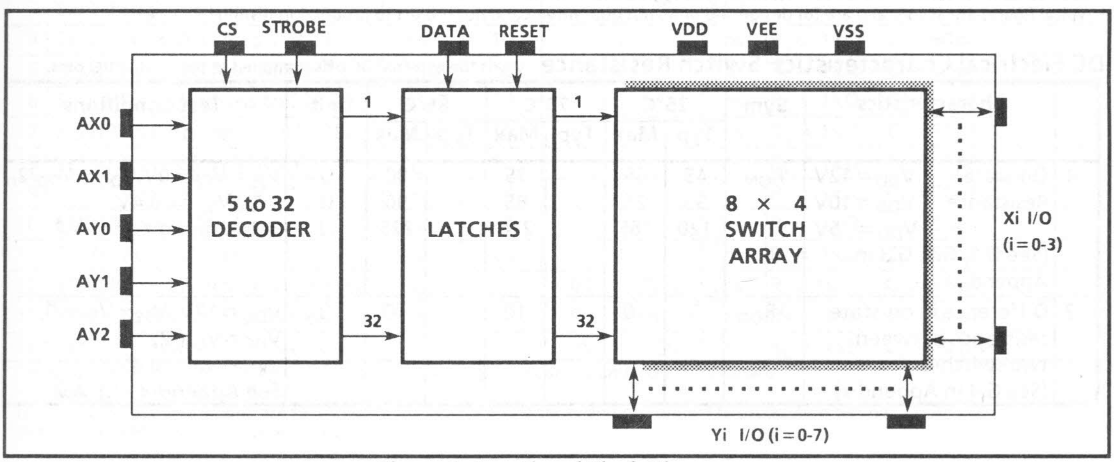


Figure 1- Functional Block Diagram

Absolute Maximum Ratings* - Voltages are with respect to V_{EE} unless otherwise stated.

	Parameter		Symbol	Min	Max	Units
1	Supply Voltage		V_{DD} V_{SS}	−0.3 −0.3	15.0 $V_{DD}+0.3$	V V
2	Analog Input Voltage		V_{INA}	−0.3	$V_{DD}+0.3$	V
3	Digital Input Voltage		V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
4	Current on any I/O Pin		I		±15	mA
5	Storage Temperature		T_S	−65	+150	°C
6	Package Power Dissipation	PLASTIC DIP CERDIP	P_D P_D		0.6 1.0	W W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{EE} unless otherwise stated.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T_O	−40	25	85	°C	
2	Supply Voltage	V_{DD} V_{SS}	4.5 V_{EE}		13.2 $V_{DD}-4.5$	V V	
3	Analog Input Voltage	V_{INA}	V_{EE}		V_{DD}	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics† - Voltages are with respect to $V_{EE}=V_{SS}=0V$, $V_{DD}=12V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DD}		1	100	µA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}
				0.4	1.5	mA	All digital inputs at $V_{IN}=2.4+V_{SS}$; $V_{SS}=7.0V$
				5	15	mA	All digital inputs at $V_{IN}=3.4V$
2	Off-state Leakage Current (See G.9 in Appendix)	I_{OFF}		±1	±500	nA	$\lvert V_{Xi}-V_{Yj}\rvert = V_{DD}-V_{EE}$ See Appendix, Fig. A.1
3	Input Logic "0" level	V_{IL}			$0.8+V_{SS}$	V	$V_{SS}=7.5V$; $V_{EE}=0V$
4	Input Logic "1" level	V_{IH}	$2.0+V_{SS}$			V	$V_{SS}=6.5V$; $V_{EE}=0V$
5	Input Logic "1" level	V_{IH}	3.3			V	
6	Input Leakage (digital pins)	I_{LEAK}		0.1	10	µA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}

† DC Electrical Characteristics are over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics- Switch Resistance - V_{DC} is the external DC offset applied at the analog I/O pins.

	Characteristics	Sym	25°C		70°C		85°C		Units	Test Conditions
			Typ	Max	Typ	Max	Typ	Max		
1	On-state Resistance $V_{DD}=12V$ $V_{DD}=10V$ $V_{DD}=5V$ (See G.1, G.2, G.3 in Appendix)	R_{ON}	45 55 120	65 75 185		75 85 215		80 90 225	Ω Ω Ω	$V_{SS}=V_{EE}=0V$, $V_{DC}=V_{DD}/2$, $\lvert V_{Xi}-V_{Yj}\rvert = 0.4V$ See Appendix, Fig. A.2
2	Difference in on-state resistance between two switches (See G.4 in Appendix)	ΔR_{ON}	5	10		10		10	Ω	$V_{DD}=12V$, $V_{SS}=V_{EE}=0$, $V_{DC}=V_{DD}/2$, $\lvert V_{Xi}-V_{Yj}\rvert = 0.4V$ See Appendix, Fig. A.2

AC Electrical Characteristics† - Crosspoint Performance

-Voltages are with respect to $V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-7V$, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f=1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f=1 MHz
3	Frequency Response Channel "ON" $20LOG(V_{OUT}/V_{Xi})=-3dB$	F_{3dB}		45		MHz	Switch is "ON"; $V_{INA}=2Vpp$ sine wave; $R_L=1k\Omega$ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; $V_{INA}=2Vpp$ sine wave f= 1kHz; $R_L=1k\Omega$
5	Feedthrough Channel "OFF" Feed.= $20LOG(V_{OUT}/V_{Xi})$ (See G.8 in Appendix)	FDT		−95		dB	All Switches "OFF"; $V_{INA}=$ 2Vpp sine wave f= 1kHz; $R_L=1k\Omega$. See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi−Yi and Xj−Yj. $Xtalk=20LOG(V_{Yj}/V_{Xi})$. (See G.7 in Appendix).	X_{talk}		−45		dB	$V_{INA}=2Vpp$ sine wave f= 10MHz; $R_L=75\Omega$.
				−90		dB	$V_{INA}=2Vpp$ sine wave f= 10kHz; $R_L=600\Omega$.
				−85		dB	$V_{INA}=2Vpp$ sine wave f= 10kHz; $R_L=1k\Omega$.
				−80		dB	$V_{INA}=2Vpp$ sine wave f= 1kHz; $R_L=10k\Omega$. Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t_{PS}			30	ns	$R_L=1k\Omega$; $C_L=50pF$

† Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5dB better.

AC Electrical Characteristics† - Control and I/O Timings

- Voltages are with respect to $V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-7V$, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Control Input crosstalk to switch (for CS, DATA, STROBE, Address)	CX_{talk}		30		mVpp	$V_{IN}=3V$ square wave; $R_{IN}=1k\Omega$, $R_L=10k\Omega$. See Appendix, Fig. A.6
2	Digital Input Capacitance	C_{DI}		10		pF	f=1MHz
3	Switching Frequency	F_O			20	MHz	
4	Setup Time DATA to STROBE	t_{DS}	10			ns	$R_L=1k\Omega$, $C_L=50pF$ ①
5	Hold Time DATA to STROBE	t_{DH}	10			ns	$R_L=1k\Omega$, $C_L=50pF$ ①
6	Setup Time Address to STROBE	t_{AS}	10			ns	$R_L=1k\Omega$, $C_L=50pF$ ①
7	Hold Time Address to STROBE	t_{AH}	10			ns	$R_L=1k\Omega$, $C_L=50pF$ ①
8	Setup Time CS to STROBE	t_{CSS}	10			ns	$R_L=1k\Omega$, $C_L=50pF$ ①
9	Hold Time CS to STROBE	t_{CSH}	10			ns	$R_L=1k\Omega$, $C_L=50pF$ ①
10	STROBE Pulse Width	t_{SPW}	20			ns	$R_L=1k\Omega$, $C_L=50pF$ ①
11	RESET Pulse Width	t_{RPW}	40			ns	$R_L=1k\Omega$, $C_L=50pF$ ①
12	STROBE to Switch Status Delay	t_S		40	100	ns	$R_L=1k\Omega$, $C_L=50pF$ ①
13	DATA to Switch Status Delay	t_D		50	100	ns	$R_L=1k\Omega$, $C_L=50pF$ ①
14	RESET to Switch Status Delay	t_R		35	100	ns	$R_L=1k\Omega$, $C_L=50pF$ ①

† Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
Digital Input rise time (tr) and fall time (tf) = 5ns.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
① Refer to Appendix, Fig. A.7 for test circuit.

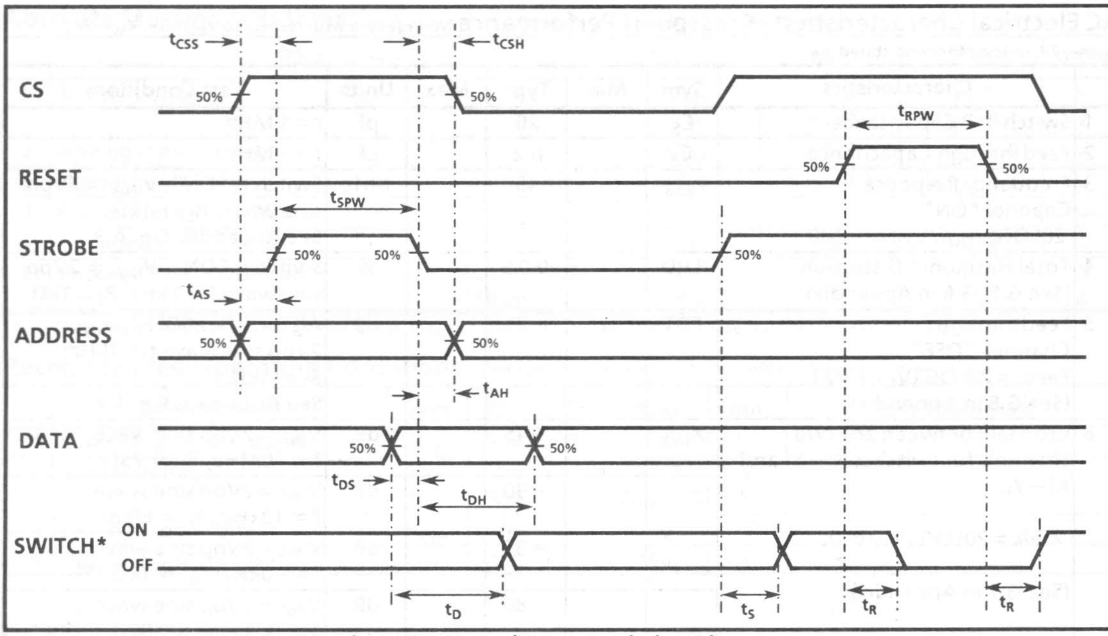


Figure 2 - Control Memory Timing Diagram

*See Appendix, Fig. A.7 for switching waveform

AX0	AX1	AY0	AY1	AY2	Connection
0	0	0	0	0	X0-Y0
0	0	1	0	0	X0-Y1
0	0	0	1	0	X0-Y2
0	0	1	1	0	X0-Y3
0	0	0	0	1	X0-Y4
0	0	1	0	1	X0-Y5
0	0	0	1	1	X0-Y6
0	0	1	1	1	X0-Y7
1 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 1	X1-Y0 ↓ ↓ X1-Y7
0 ↓ 0	1 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	X2-Y0 ↓ ↓ X2-Y7
1 ↓ 1	1 ↓ 1	0 ↓ 1	0 ↓ 1	0 ↓ 1	X3-Y0 ↓ ↓ X3-Y7

Table 1 - Address Decode Truth Table

Pin Description

Pin #*	Name	Description
1-3	Y2-Y0	**Y2-Y0 Analog (Inputs/Outputs):** these are connected to the Y2-Y0 columns of the switch array.
4	DATA	**DATA (Input)**: a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
5	X0	**X0 Analog (Input/Output):** this is connected to the X0 row of the switch array.
6	AX0	**X0 Address Line (Input).**
7	X1	**X1 Analog (Input/Output):** this is connected to the X1 row of the switch array.
8	AX1	**X1 Address Line (Input).**
9	X2	**X2 Analog (Input/Output):** this is connected to the X2 row of the switch array.
10	CS	**Chip Select (Input)**: this is used to select the device. Active High.
11	X3	**X3 Analog (Input/Output):** this is connected to the X3 row of the switch array.
12	VSS	**Digital Ground Reference.**
13	VEE	**Negative Power Supply.**
14-16	AY0-AY2	**Y0 -Y2 Address Lines (Inputs).**
17	STROBE	**STROBE (Input)**: enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High.
18	RESET	**Master RESET (Input):** this is used to turn off all switches regardless of the condition of CS. Active High.
19-23	Y7-Y3	**Y7-Y3 Analog (Inputs/Outputs):** these are connected to the Y7-Y3 columns of the switch array.
24	VDD	**Positive Power Supply.**

* Plastic DIP and CERDIP only

Functional Description

The MT8806 is an analog switch matrix with an array size of 8×4. The switch array is arranged such that there are 8 columns by 4 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 32 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0 & AX1). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever both the CS (Chip Select) and the STROBE inputs are high and is latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input will asynchronously return all memory locations to logical "0" turning off all crosspoint switches regardless of whether CS is high or low. Two voltage reference pins (V_{SS} and V_{EE}) are provided for the MT8806 to enable switching of negative analog signals. The range for digital signals is from V_{DD} to V_{SS} while the range for analog signals is from V_{DD} to V_{EE}. V_{SS} and V_{EE} pins can be tied together if a single voltage reference is needed.

Address Decode

The five address inputs along with the STROBE and CS (Chip Select) inputs are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low and CS must go high while the address and data are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

NOTES:

MITEL®

ISO-CMOS MT8808
8 x 8 Analog Switch Array

9161-002-098-NA ISSUE 2 November 1988

Features

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage: 4.5V to 13.2V
- 12Vpp analog signal capability
- R_{ON} 65Ω max. @ V_{DD} = 12V, 25°C
- $\Delta R_{ON} \leq 10\Omega$ @ V_{DD} = 12V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Separate analog and digital reference supplies
- Low power consumption ISO-CMOS technology

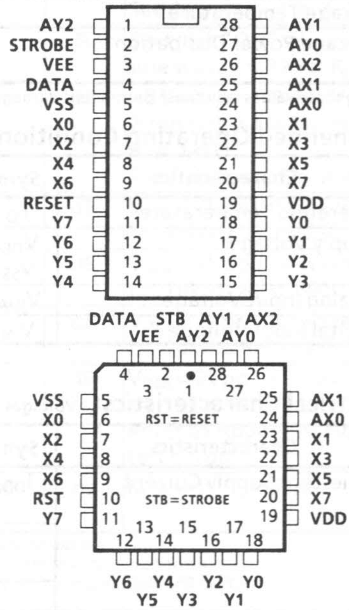
Applications

- Key systems
- PBX systems
- Mobile radio
- Test equipment /instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Description

The Mitel MT8808 is fabricated in MITEL's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8×8 array of crosspoint switches along with a 6 to 64 line decoder and latch circuits. Any one of the 64 switches can be addressed by selecting the appropriate six address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. V_{SS} is the ground reference of the digital inputs. The range of the analog signal is from V_{DD} to V_{EE}.

Pin Connections



Ordering Information −40° to 85°C

MT8808AC 28 Pin CERDIP
MT8808AE 28 Pin PLASTIC DIP
MT8808AP 28 Pin PLCC

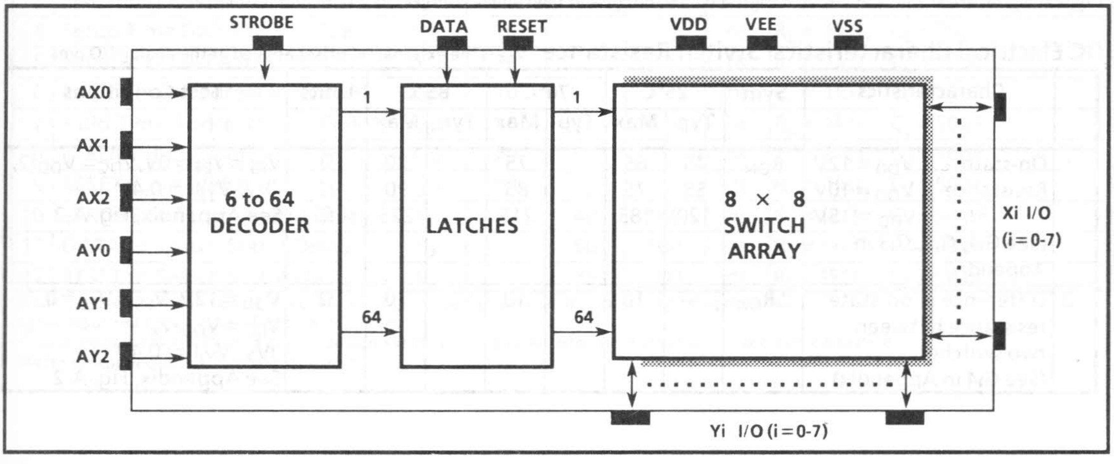


Figure 1- Functional Block Diagram

Absolute Maximum Ratings* - Voltages are with respect to V_{EE} unless otherwise stated.

	Parameter		Symbol	Min	Max	Units
1	Supply Voltage		V_{DD} V_{SS}	−0.3 −0.3	15.0 $V_{DD}+0.3$	V V
2	Analog Input Voltage		V_{INA}	−0.3	$V_{DD}+0.3$	V
3	Digital Input Voltage		V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
4	Current on any I/O Pin		I		±15	mA
5	Storage Temperature		T_S	−65	+150	°C
6	Package Power Dissipation	PLASTIC DIP CERDIP	P_D P_D		0.6 1.0	W W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{EE} unless otherwise stated.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T_O	−40	25	85	°C	
2	Supply Voltage	V_{DD} V_{SS}	4.5 V_{EE}		13.2 $V_{DD}-4.5$	V V	
3	Analog Input Voltage	V_{INA}	V_{EE}		V_{DD}	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics† - Voltages are with respect to $V_{EE}=V_{SS}=0V$, $V_{DD}=12V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DD}		1	100	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}
				0.4	1.5	mA	All digital inputs at $V_{IN}=2.4+V_{SS}$; $V_{SS}=7.0V$
				5	15	mA	All digital inputs at $V_{IN}=3.4V$
2	Off-state Leakage Current (See G.9 in Appendix)	I_{OFF}		±1	±500	nA	$\lvert V_{Xi}-V_{Yj}\rvert = V_{DD}-V_{EE}$ See Appendix, Fig. A.1
3	Input Logic "0" level	V_{IL}			$0.8+V_{SS}$	V	$V_{SS}=7.5V$; $V_{EE}=0V$
4	Input Logic "1" level	V_{IH}	$2.0+V_{SS}$			V	$V_{SS}=6.5V$; $V_{EE}=0V$
5	Input Logic "1" level	V_{IH}	3.3			V	
6	Input Leakage (digital pins)	I_{LEAK}		0.1	10	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}

† DC Electrical Characteristics are over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics- Switch Resistance - V_{DC} is the external DC offset applied at the analog I/O pins.

	Characteristics	Sym	25°C		70°C		85°C		Units	Test Conditions
			Typ	Max	Typ	Max	Typ	Max		
1	On-state Resistance $V_{DD}=12V$ $V_{DD}=10V$ $V_{DD}=5V$ (See G.1, G.2, G.3 in Appendix)	R_{ON}	45 55 120	65 75 185		75 85 215		80 90 225	Ω Ω Ω	$V_{SS}=V_{EE}=0V$, $V_{DC}=V_{DD}/2$, $\lvert V_{Xi}-V_{Yj}\rvert = 0.4V$ See Appendix, Fig. A.2
2	Difference in on-state resistance between two switches (See G.4 in Appendix)	ΔR_{ON}	5	10		10		10	Ω	$V_{DD}=12V$, $V_{SS}=V_{EE}=0$, $V_{DC}=V_{DD}/2$, $\lvert V_{Xi}-V_{Yj}\rvert = 0.4V$ See Appendix, Fig. A.2

AC Electrical Characteristics† - Crosspoint Performance

-Voltages are with respect to $V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-7V$, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f=1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f=1 MHz
3	Frequency Response Channel "ON" $20LOG(V_{OUT}/V_{Xi})=-3dB$	F_{3dB}		45		MHz	Switch is "ON"; V_{INA} = 2Vpp sine wave; R_L = 1kΩ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; V_{INA} = 2Vpp sine wave f= 1kHz; R_L=1kΩ
5	Feedthrough Channel "OFF" Feed.=$20LOG(V_{OUT}/V_{Xi})$ (See G.8 in Appendix)	FDT		−95		dB	All Switches "OFF"; V_{INA}= 2Vpp sine wave f= 1kHz; R_L= 1kΩ. See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi−Yi and Xj−Yj. Xtalk=$20LOG(V_{Yj}/V_{Xi})$. (See G.7 in Appendix).	X_{talk}		−45		dB	V_{INA}=2Vpp sine wave f= 10MHz; R_L = 75Ω.
				−90		dB	V_{INA}=2Vpp sine wave f= 10kHz; R_L = 600Ω.
				−85		dB	V_{INA}=2Vpp sine wave f= 10kHz; R_L = 1kΩ.
				−80		dB	V_{INA}=2Vpp sine wave f= 1kHz; R_L = 10kΩ. Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t_{PS}			30	ns	R_L= 1kΩ; C_L=50pF

† Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5dB better.

AC Electrical Characteristics† - Control and I/O Timings

- Voltages are with respect to $V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-7V$, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Control Input crosstalk to switch (for DATA, STROBE, Address)	CX_{talk}		30		mVpp	V_{IN}=3V squarewave; R_{IN}=1kΩ, R_L=10kΩ. See Appendix, Fig. A.6
2	Digital Input Capacitance	C_{DI}		10		pF	f=1MHz
3	Switching Frequency	F_O			20	MHz	
4	Setup Time DATA to STROBE	t_{DS}	10			ns	R_L= 1kΩ, C_L=50pF ①
5	Hold Time DATA to STROBE	t_{DH}	10			ns	R_L= 1kΩ, C_L=50pF ①
6	Setup Time Address to STROBE	t_{AS}	10			ns	R_L= 1kΩ, C_L=50pF ①
7	Hold Time Address to STROBE	t_{AH}	10			ns	R_L= 1kΩ, C_L=50pF ①
8	STROBE Pulse Width	t_{SPW}	20			ns	R_L= 1kΩ, C_L=50pF ①
9	RESET Pulse Width	t_{RPW}	40			ns	R_L= 1kΩ, C_L=50pF ①
10	STROBE to Switch Status Delay	t_S		40	100	ns	R_L=1kΩ, C_L=50 pF ①
11	DATA to Switch Status Delay	t_D		50	100	ns	R_L=1kΩ, C_L=50 pF ①
12	RESET to Switch Status Delay	t_R		35	100	ns	R_L=1kΩ, C_L=50 pF ①

† Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
Digital Input rise time (tr) and fall time (tf) = 5ns.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
① Refer to Appendix, Fig. A.7 for test circuit.

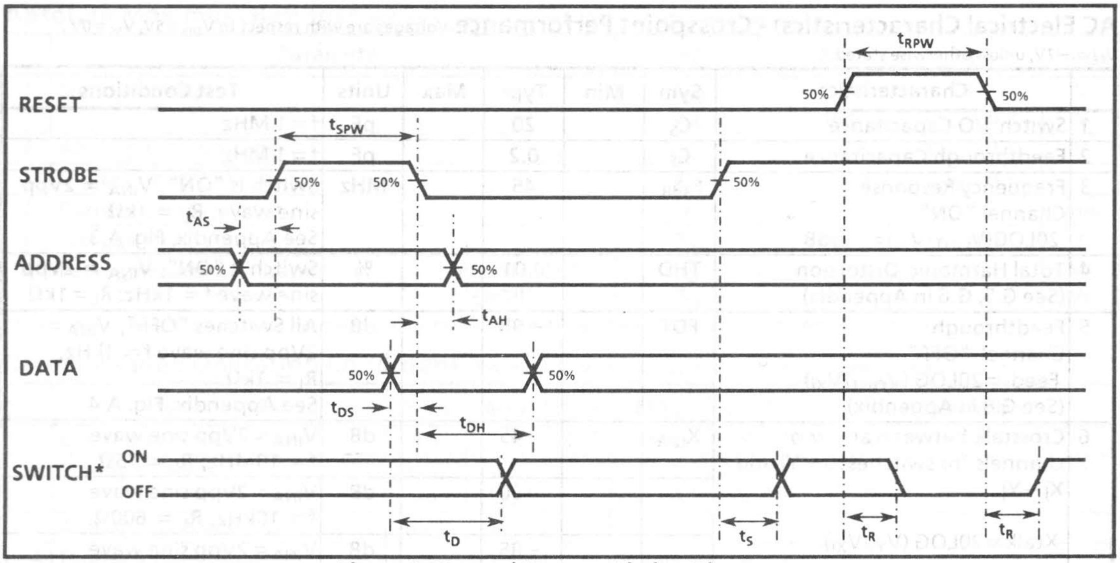


Figure 2 - Control Memory Timing Diagram

*See Appendix, Fig. A.7 for switching waveform

AY2	AY1	AY0	AX2	AX1	AX0	Connection	AY2	AY1	AY0	AX2	AX1	AX0	Connection
0	0	0	0	0	0	X0 Y0	1	0	0	0	0	0	X0 Y4
0	0	0	0	0	1	X1 Y0	1	0	0	0	0	1	X1 Y4
0	0	0	0	1	0	X2 Y0	1	0	0	0	1	0	X2 Y4
0	0	0	0	1	1	X3 Y0	1	0	0	0	1	1	X3 Y4
0	0	0	1	0	0	X4 Y0	1	0	0	1	0	0	X4 Y4
0	0	0	1	0	1	X5 Y0	1	0	0	1	0	1	X5 Y4
0	0	0	1	1	0	X6 Y0	1	0	0	1	1	0	X6 Y4
0	0	0	1	1	1	X7 Y0	1	0	0	1	1	1	X7 Y4
0	0	1	0	0	0	X0 Y1	1	0	1	0	0	0	X0 Y5
0	0	1	0	0	1	X1 Y1	1	0	1	0	0	1	X1 Y5
0	0	1	0	1	0	X2 Y1	1	0	1	0	1	0	X2 Y5
0	0	1	0	1	1	X3 Y1	1	0	1	0	1	1	X3 Y5
0	0	1	1	0	0	X4 Y1	1	0	1	1	0	0	X4 Y5
0	0	1	1	0	1	X5 Y1	1	0	1	1	0	1	X5 Y5
0	0	1	1	1	0	X6 Y1	1	0	1	1	1	0	X6 Y5
0	0	1	1	1	1	X7 Y1	1	0	1	1	1	1	X7 Y5
0	1	0	0	0	0	X0 Y2	1	1	0	0	0	0	X0 Y6
0	1	0	0	0	1	X1 Y2	1	1	0	0	0	1	X1 Y6
0	1	0	0	1	0	X2 Y2	1	1	0	0	1	0	X2 Y6
0	1	0	0	1	1	X3 Y2	1	1	0	0	1	1	X3 Y6
0	1	0	1	0	0	X4 Y2	1	1	0	1	0	0	X4 Y6
0	1	0	1	0	1	X5 Y2	1	1	0	1	0	1	X5 Y6
0	1	0	1	1	0	X6 Y2	1	1	0	1	1	0	X6 Y6
0	1	0	1	1	1	X7 Y2	1	1	0	1	1	1	X7 Y6
0	1	1	0	0	0	X0 Y3	1	1	1	0	0	0	X0 Y7
0	1	1	0	0	1	X1 Y3	1	1	1	0	0	1	X1 Y7
0	1	1	0	1	0	X2 Y3	1	1	1	0	1	0	X2 Y7
0	1	1	0	1	1	X3 Y3	1	1	1	0	1	1	X3 Y7
0	1	1	1	0	0	X4 Y3	1	1	1	1	0	0	X4 Y7
0	1	1	1	0	1	X5 Y3	1	1	1	1	0	1	X5 Y7
0	1	1	1	1	0	X6 Y3	1	1	1	1	1	0	X6 Y7
0	1	1	1	1	1	X7 Y3	1	1	1	1	1	1	X7 Y7

Table 1 - Address Decode Truth Table

Pin Description

Pin #	Name	Description
1	AY2	**AY2 Address Line (Input).**
2	STROBE	**STROBE (Input)**: enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High.
3	VEE	**Negative Power Supply.**
4	DATA	**DATA (Input)**: a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
5	VSS	**Digital Ground Reference .**
6-9	X0, X2, X4, X6	**X0, X2, X4 and X6 Analog (Inputs/Outputs):** these are connected to the X0, X2, X4 and X6 rows of the switch array.
10	RESET	**Master RESET (Input):** this is used to turn off all switches. Active High.
11-18	Y7 - Y0	**Y7 - Y0 Analog (Inputs/Outputs):** these are connected to the Y0 - Y7 columns of the switch array.
19	VDD	**Positive Power Supply.**
20-23	X7, X5, X3, X1	**X7, X5, X3 and X1 Analog (Inputs/Outputs):** these are connected to the X7, X5, X3 and X1 rows of the switch array.
24-26	AX0-AX2	**AX0 - AX2 Address Lines (Inputs).**
27,28	AY0, AY1	**AY0 and AY1 Address Lines (Inputs).**

Functional Description

The MT8808 is an analog switch matrix with an array size of 8×8. The switch array is arranged such that there are 8 columns by 8 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 64 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX2). Data is presented to the memory on the DATA input. Data is asynchro-nously written into memory whenever the STROBE input is high and is latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input will asynchronously return all memory locations to logical "0" turning off all crosspoint switches. Two voltage reference pins (V_{SS} and V_{EE}) are provided for the MT8808 to enable switching of negative analog signals. The range for digital signals is from V_{DD} to V_{SS} while the range for analog signals is from V_{DD} to V_{EE}. V_{SS} and V_{EE} pins can be tied together if a single voltage reference is needed.

Address Decode

The six address inputs along with the STROBE are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low while the address and data are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

NOTES:

MITEL®

ISO-CMOS **MT8809**

8 x 8 Analog Switch Array

9161-002-099-NA   ISSUE 2   November 1988

Features

- Internal control latches and address decoder
- Short setup and hold times
- Wide operating voltage: 4.5V to 13.2V
- 12Vpp analog signal capability
- R_{ON} 65Ω max. @ V_{DD} = 12V, 25°C
- $\Delta R_{ON} \leq 10\Omega$ @ V_{DD} = 12V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Low power consumption ISO-CMOS technology
- Internal pull-up resistor for $\overline{\text{RESET}}$ pin

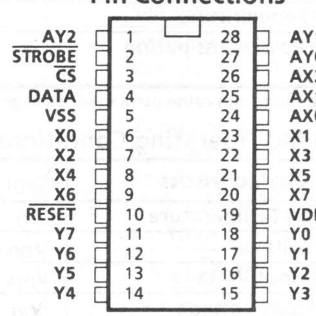
Applications

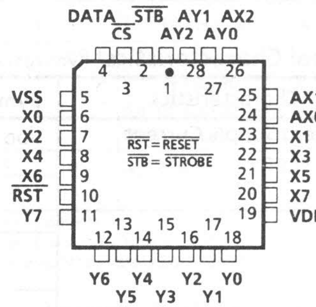
- Key systems
- PBX systems
- Mobile radio
- Test equipment /instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Description

The Mitel MT8809 is fabricated in MITEL's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8×8 array of crosspoint switches along with a 6 to 64 line decoder and latch circuits. Any one of the 64 switches can be addressed by selecting the appropriate six address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. Chip Select ($\overline{\text{CS}}$) allows the crosspoint array to be cascaded for matrix expansion.

Pin Connections





Ordering Information -40° to 85°C

MT8809AC	28 Pin CERDIP
MT8809AE	28 Pin PLASTIC DIP
MT8809AP	28 Pin PLCC

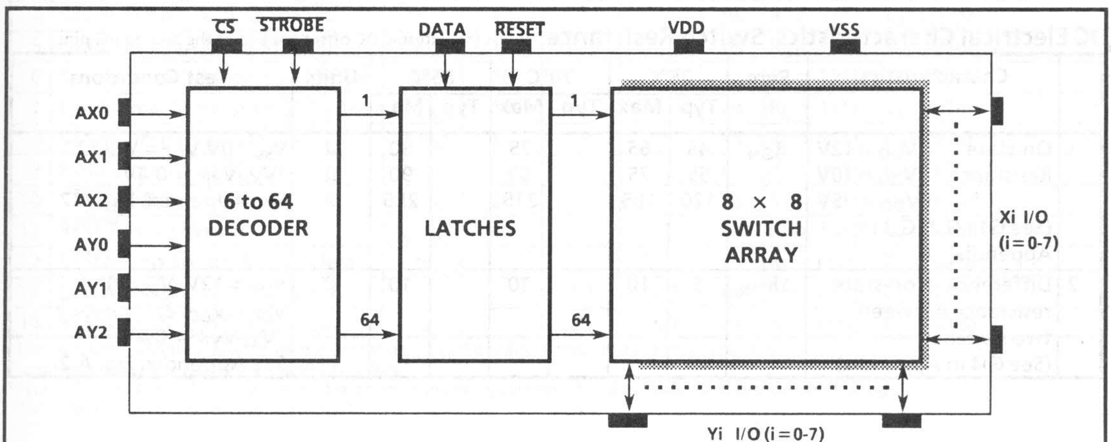


Figure 1- Functional Block Diagram

Absolute Maximum Ratings* - Voltages are with respect to V_{SS} unless otherwise stated.

	Parameter		Symbol	Min	Max	Units
1	Supply Voltage		V_{DD} V_{SS}	−0.3 −0.3	15.0 $V_{DD}+0.3$	V V
2	Analog Input Voltage		V_{INA}	−0.3	$V_{DD}+0.3$	V
3	Digital Input Voltage		V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
4	Current on any I/O Pin		I		±15	mA
5	Storage Temperature		T_S	−65	+150	°C
6	Package Power Dissipation	PLASTIC DIP CERDIP	P_D P_D		0.6 1.0	W W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{SS} unless otherwise stated.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T_O	−40	25	85	°C	
2	Supply Voltage	V_{DD}	4.5		13.2	V	
3	Analog Input Voltage	V_{INA}	V_{SS}		V_{DD}	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics† - Voltages are with respect to $V_{SS}=0V$, $V_{DD}=12V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DD}		1	100	μA	All digital inputs at $V_{IN}=V_{SS}$ V_{DD} except $\overline{RESET}=V_{DD}$.
				120	400	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD} except $\overline{RESET}=V_{SS}$.
				0.5	1.6	mA	All digital inputs at $V_{IN}=2.4V$, $V_{DD}=5.0V$
				5	15	mA	All digital inputs at $V_{IN}=3.4V$
2	Off-state Leakage Current (See G.9 in Appendix)	I_{OFF}		±1	±500	nA	$\lvert V_{Xi}-V_{Yj}\rvert = V_{DD}-V_{SS}$ See Appendix, Fig. A.1
3	Input Logic "0" level	V_{IL}			0.8	V	
4	Input Logic "1" level	V_{IH}	3.0			V	
5	Input Leakage (digital pins)	I_{LEAK}		0.1	10	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}; $\overline{RESET}=V_{DD}$

† DC Electrical Characteristics are over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics- Switch Resistance - V_{DC} is the external DC offset applied at the analog I/O pins.

	Characteristics		Sym	25°C		70°C		85°C		Units	Test Conditions
				Typ	Max	Typ	Max	Typ	Max		
1	On-state Resistance (See G1, G.2, G.3 in Appendix)	$V_{DD}=12V$ $V_{DD}=10V$ $V_{DD}=5V$	R_{ON}	45 55 120	65 75 185		75 85 215		80 90 225	Ω Ω Ω	$V_{SS}=0V, V_{DC}=V_{DD}/2$, $\lvert V_{Xi}-V_{Yj}\rvert = 0.4V$ See Appendix, Fig. A.2
2	Difference in on-state resistance between two switches (See G.4 in Appendix)		ΔR_{ON}	5	10		10		10	Ω	$V_{DD}=12V$, $V_{SS}=0$, $V_{DC}=V_{DD}/2$, $\lvert V_{Xi}-V_{Yj}\rvert = 0.4V$ See Appendix, Fig. A.2

AC Electrical Characteristics† - Crosspoint Performance- V_{DC} is the external DC offset at the analog I/O pins.

Voltages are with respect to V_{DD} = 5V, V_{DC} = 0V, V_{SS} = −7V, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f=1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f=1 MHz
3	Frequency Response Channel "ON" 20LOG(V_{OUT}/V_{Xi}) = −3dB	F_{3dB}		45		MHz	Switch is "ON"; V_{INA} = 2Vpp sine wave; R_L = 1kΩ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; V_{INA} = 2Vpp sine wave f= 1kHz; R_L=1kΩ
5	Feedthrough Channel "OFF" Feed.=20LOG (V_{OUT}/V_{Xi}) (See G.8 in Appendix)	FDT		−95		dB	All Switches "OFF"; V_{INA}= 2Vpp sine wave f= 1kHz; R_L= 1kΩ. See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi−Yi and Xj−Yj. Xtalk=20LOG (V_{Yj}/V_{Xi}). (See G.7 in Appendix).	X_{talk}		−45		dB	V_{INA}=2Vpp sine wave f= 10MHz; R_L = 75Ω.
				−90		dB	V_{INA}=2Vpp sine wave f= 10kHz; R_L = 600Ω.
				−85		dB	V_{INA}=2Vpp sine wave f= 10kHz; R_L = 1kΩ.
				−80		dB	V_{INA}=2Vpp sine wave f= 1kHz; R_L = 10kΩ. Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t_{PS}			30	ns	R_L=1kΩ; C_L=50pF

† Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5dB better.

AC Electrical Characteristics† - Control and I/O Timings- V_{DC} is the external DC offset applied at the analog I/O pins.

Voltages are with respect to V_{DD} = 5V, V_{DC} = 0V, V_{SS} = −7V unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Control Input crosstalk to switch (for $\overline{CS}$, DATA, $\overline{STROBE}$, Address)	CX_{talk}		30		mVpp	V_{IN}=3V + V_{DC} squarewave; R_{IN}= 1kΩ, R_L = 1kΩ. See Appendix, Fig. A.6
2	Digital Input Capacitance	C_{DI}		10		pF	f=1MHz
3	Switching Frequency	F_O			20	MHz	
4	Setup Time DATA to $\overline{STROBE}$	t_{DS}	10			ns	R_L= 1kΩ, C_L=50pF ①
5	Hold Time DATA to $\overline{STROBE}$	t_{DH}	10			ns	R_L= 1kΩ, C_L=50pF ①
6	Setup Time Address to $\overline{STROBE}$	t_{AS}	10			ns	R_L= 1kΩ, C_L=50pF ①
7	Hold Time Address to $\overline{STROBE}$	t_{AH}	10			ns	R_L= 1kΩ, C_L=50pF ①
8	Setup Time $\overline{CS}$ to $\overline{STROBE}$	t_{CSS}	10			ns	R_L= 1kΩ, C_L=50pF ①
9	Hold Time $\overline{CS}$ to $\overline{STROBE}$	t_{CSH}	10			ns	R_L= 1kΩ, C_L=50pF ①
10	$\overline{STROBE}$ Pulse Width	t_{SPW}	20			ns	R_L= 1kΩ, C_L=50pF ①
11	$\overline{RESET}$ Pulse Width	t_{RPW}	40			ns	R_L= 1kΩ, C_L=50pF ①
12	$\overline{STROBE}$ to Switch Status Delay	t_S		40	100	ns	R_L=1kΩ, C_L=50 pF ①
13	DATA to Switch Status Delay	t_D		50	100	ns	R_L=1kΩ, C_L=50 pF ①
14	$\overline{RESET}$ to Switch Status Delay	t_R		35	100	ns	R_L=1kΩ, C_L=50 pF ①

† Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
Digital Input rise time (tr) and fall time (tf) = 5ns.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
① Refer to Appendix, Fig. A.7 for test circuit.

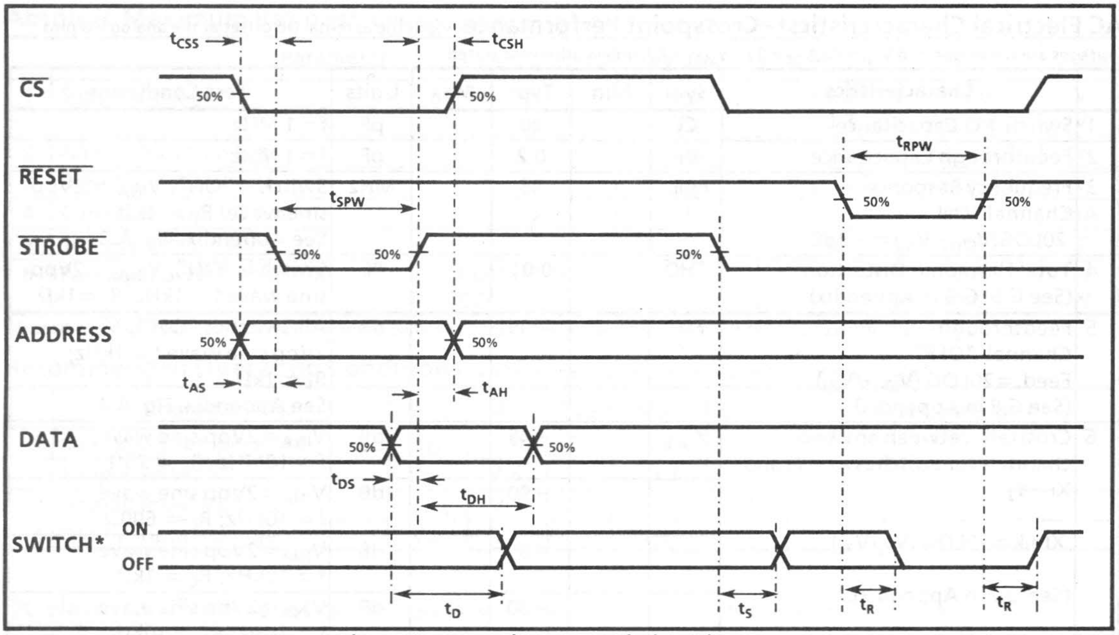


Figure 2 - Control Memory Timing Diagram

*See Appendix, Fig. A.7 for switching waveform

AY2	AY1	AY0	AX2	AX1	AX0	Connection	AY2	AY1	AY0	AX2	AX1	AX0	Connection
0	0	0	0	0	0	X0 Y0	1	0	0	0	0	0	X0 Y4
0	0	0	0	0	1	X1 Y0	1	0	0	0	0	1	X1 Y4
0	0	0	0	1	0	X2 Y0	1	0	0	0	1	0	X2 Y4
0	0	0	0	1	1	X3 Y0	1	0	0	0	1	1	X3 Y4
0	0	0	1	0	0	X4 Y0	1	0	0	1	0	0	X4 Y4
0	0	0	1	0	1	X5 Y0	1	0	0	1	0	1	X5 Y4
0	0	0	1	1	0	X6 Y0	1	0	0	1	1	0	X6 Y4
0	0	0	1	1	1	X7 Y0	1	0	0	1	1	1	X7 Y4
0	0	1	0	0	0	X0 Y1	1	0	1	0	0	0	X0 Y5
0	0	1	0	0	1	X1 Y1	1	0	1	0	0	1	X1 Y5
0	0	1	0	1	0	X2 Y1	1	0	1	0	1	0	X2 Y5
0	0	1	0	1	1	X3 Y1	1	0	1	0	1	1	X3 Y5
0	0	1	1	0	0	X4 Y1	1	0	1	1	0	0	X4 Y5
0	0	1	1	0	1	X5 Y1	1	0	1	1	0	1	X5 Y5
0	0	1	1	1	0	X6 Y1	1	0	1	1	1	0	X6 Y5
0	0	1	1	1	1	X7 Y1	1	0	1	1	1	1	X7 Y5
0	1	0	0	0	0	X0 Y2	1	1	0	0	0	0	X0 Y6
0	1	0	0	0	1	X1 Y2	1	1	0	0	0	1	X1 Y6
0	1	0	0	1	0	X2 Y2	1	1	0	0	1	0	X2 Y6
0	1	0	0	1	1	X3 Y2	1	1	0	0	1	1	X3 Y6
0	1	0	1	0	0	X4 Y2	1	1	0	1	0	0	X4 Y6
0	1	0	1	0	1	X5 Y2	1	1	0	1	0	1	X5 Y6
0	1	0	1	1	0	X6 Y2	1	1	0	1	1	0	X6 Y6
0	1	0	1	1	1	X7 Y2	1	1	0	1	1	1	X7 Y6
0	1	1	0	0	0	X0 Y3	1	1	1	0	0	0	X0 Y7
0	1	1	0	0	1	X1 Y3	1	1	1	0	0	1	X1 Y7
0	1	1	0	1	0	X2 Y3	1	1	1	0	1	0	X2 Y7
0	1	1	0	1	1	X3 Y3	1	1	1	0	1	1	X3 Y7
0	1	1	1	0	0	X4 Y3	1	1	1	1	0	0	X4 Y7
0	1	1	1	0	1	X5 Y3	1	1	1	1	0	1	X5 Y7
0	1	1	1	1	0	X6 Y3	1	1	1	1	1	0	X6 Y7
0	1	1	1	1	1	X7 Y3	1	1	1	1	1	1	X7 Y7

Table 1 - Address Decode Truth Table

Pin Description

Pin #	Name	Description
1	AY2	**AY2 Address Line (Input).**
2	$\overline{\text{STROBE}}$	**STROBE (Input):** enables function selected by address and data. Address must be stable before $\overline{\text{STROBE}}$ goes low and DATA must be stable on the rising edge of $\overline{\text{STROBE}}$. Active Low.
3	$\overline{\text{CS}}$	**Chip Select (Input):** this is used to select the device. Active Low.
4	DATA	**DATA (Input):** a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
5	VSS	**Ground Reference.**
6-9	X0, X2, X4, X6	**X0, X2, X4 and X6 Analog (Inputs/Outputs):** these are connected to the X0, X2, X4 and X6 rows of the switch array.
10	$\overline{\text{RESET}}$	**Master RESET (Input):** this is used to turn off all switches regardless of the condition of $\overline{\text{CS}}$. A 100kΩ internal pull-up resistor is also provided. This can be used in conjunction with a 0.1µF capacitor (connected to the $\overline{\text{RESET}}$ pin) to perform power-on reset of the device. Active Low.
11-18	Y7 - Y0	**Y7 - Y0 Analog (Inputs/Outputs):** these are connected to the Y0 - Y7 columns of the switch array.
19	VDD	**Positive Power Supply .**
20-23	X7, X5, X3, X1	**X7, X5, X3 and X1 Analog (Inputs/Outputs):** these are connected to the X7, X5, X3 and X1 rows of the switch array.
24-26	AX0-AX2	**AX0 - AX2 Address Lines (Inputs).**
27, 28	AY0, AY1	**AY0 and AY1 Address Lines (Inputs).**

Functional Description

The MT8809 is an analog switch matrix with an array size of 8×8. The switch array is arranged such that there are 8 columns by 8 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 64 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX2). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever both the $\overline{\text{CS}}$ (Chip Select) and $\overline{\text{STROBE}}$ inputs are low and are latched on the rising edge of $\overline{\text{STROBE}}$. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "0" on the $\overline{\text{RESET}}$ input will asynchronously return all memory locations to logical "0" turning off all crosspoint switches regardless of whether $\overline{\text{CS}}$ is high or low.

Address Decode

The six address inputs along with the $\overline{\text{STROBE}}$ and $\overline{\text{CS}}$ (Chip Select) are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, $\overline{\text{RESET}}$ must be high and $\overline{\text{CS}}$ must go low while the address and data are set up. Then the $\overline{\text{STROBE}}$ input is set low and then high causing the data to be latched. The data can be changed while $\overline{\text{STROBE}}$ is low, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the rising edge of $\overline{\text{STROBE}}$ in order for correct data to be written to the latch.

NOTES:

ISO-CMOS MT8812
8 x 12 Analog Switch Array

9161-002-059-NA ISSUE 5 November 1988

Features

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage: 4.5V to 14.5V
- 14Vpp analog signal capability
- R_{ON} 65Ω max. @ V_{DD}=14V, 25°C
- $\Delta R_{ON} \leq 10\Omega$ @ V_{DD}=14V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Low power consumption ISO-CMOS technology

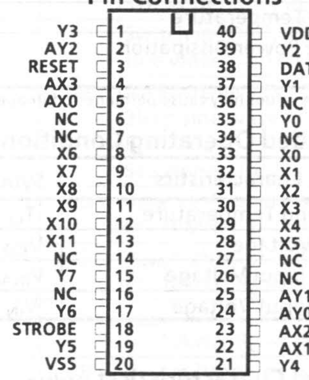
Applications

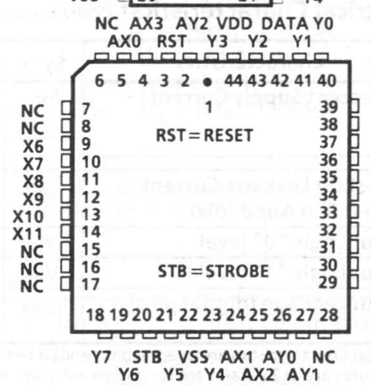
- PBX systems
- Mobile radio
- Test equipment /instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Description

The Mitel MT8812 is fabricated in MITEL's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8×12 array of crosspoint switches along with a 7 to 96 line decoder and latch circuits. Any one of the 96 switches can be addressed by selecting the appropriate seven input bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input.

Pin Connections





Ordering Information 0° to 70°C

MT8812AC	40 Pin CERDIP
MT8812AE	40 Pin PLASTIC DIP
MT8812AP	44 Pin PLCC

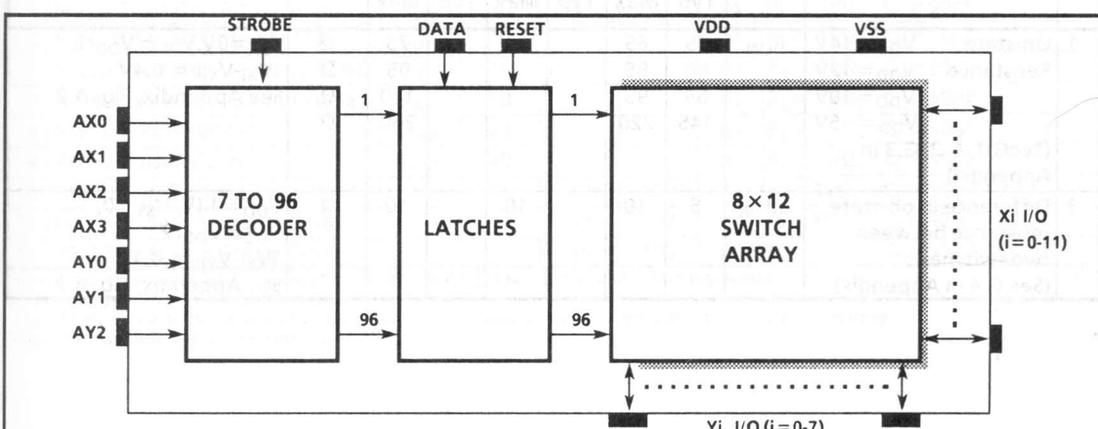


Figure 1- Functional Block Diagram

Absolute Maximum Ratings* - Voltages are with respect to V_{SS} unless otherwise stated.

	Parameter		Symbol	Min	Max	Units
1	Supply Voltage		V_{DD} V_{SS}	−0.3 −0.3	16.0 $V_{DD}+0.3$	V V
2	Analog Input Voltage		V_{INA}	−0.3	$V_{DD}+0.3$	V
3	Digital Input Voltage		V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
4	Current on any I/O Pin		I		±15	mA
5	Storage Temperature		T_S	−65	+150	°C
6	Package Power Dissipation	PLASTIC DIP CERDIP	P_D P_D		0.6 1.0	W W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{SS} unless otherwise stated

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T_O	0	25	70	°C	
2	Supply Voltage	V_{DD}	4.5		14.5	V	
3	Analog Input Voltage	V_{INA}	V_{SS}		V_{DD}	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics† - Voltages are with respect to $V_{SS}=0V$ and $V_{DD}=14V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DD}		1	100	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}
				7	15	mA	All digital inputs at $V_{IN}=2.4V$
2	Off-state Leakage Current (See G.9 in Appendix)	I_{OFF}		±1	±500	nA	$\lvert V_{Xi}-V_{Yj}\rvert=V_{DD}-V_{SS}$ See Appendix, Fig. A.1
3	Input Logic "0" level	V_{IL}			0.8	V	
4	Input Logic "1" level	V_{IH}	2.4			V	
5	Input Leakage (digital pins)	I_{LEAK}		0.1	10	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Switch Resistance - V_{DC} is the external DC offset applied at the analog I/O pins.

	Characteristics	Sym	25°C		60°C		70°C		Units	Test Conditions
			Typ	Max	Typ	Max	Typ	Max		
1	On-state Resistance $V_{DD}=14V$	R_{ON}	45	65				75	Ω	$V_{SS}=0V, V_{DC}=V_{DD}/2$, $\lvert V_{Xi}-V_{Yj}\rvert=0.4V$ See Appendix, Fig. A.2
	$V_{DD}=12V$		60	85				95	Ω	
	$V_{DD}=10V$		65	95				110	Ω	
	$V_{DD}=5V$ (See G.1, G.2, G.3 in Appendix)		145	220				260	Ω	
2	Difference in on-state resistance between two switches (See G.4 in Appendix)	ΔR_{ON}	5	10		10		10	Ω	$V_{DD}=14V, V_{SS}=0$, $V_{DC}=V_{DD}/2$, $\lvert V_{Xi}-V_{Yj}\rvert=0.4V$ See Appendix, Fig. A.2

AC Electrical Characteristics† - Crosspoint Performance
- V_{DC} is the external DC offset applied at the analog I/O pins. Voltages are with respect $V_{DD}=7V$, $V_{DC}=0V$, $V_{SS}=-7V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f=1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f=1 MHz
3	Frequency Response Channel "ON" $20LOG(V_{OUT}/V_{Xi})=-3dB$	F_{3dB}		45		MHz	Switch is "ON"; V_{INA} = 2Vpp sine wave; R_L = 1kΩ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; V_{INA} = 2Vpp sine wave f= 1kHz; R_L=1kΩ
5	Feedthrough Channel "OFF" Feed.=20LOG (V_{OUT}/V_{Xi}) (See G.8 in Appendix)	FDT		−95		dB	All Switches "OFF"; V_{INA}= 2Vpp sine wave f= 1kHz; R_L= 1kΩ. See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi−Yi and Xj−Yj. Xtalk=20LOG (V_{Yj}/V_{Xi}). (See G.7 in Appendix).	X_{talk}		−45		dB	V_{INA}=2Vpp sine wave f= 10MHz; R_L = 75Ω.
				−90		dB	V_{INA}=2Vpp sine wave f= 10kHz; R_L = 600Ω.
				−85		dB	V_{INA}=2Vpp sine wave f= 10kHz; R_L = 1kΩ.
				−80		dB	V_{INA}=2Vpp sine wave f= 1kHz; R_L = 10kΩ. Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t_{PS}			30	ns	R_L=1kΩ; C_L=50pF

† Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5dB better.

AC Electrical Characteristics† - Control and I/O Timings
- V_{DC} is the external DC offset applied at the analog I/O pins. Voltages are with respect $V_{DD}=7V$, $V_{DC}=0V$, $V_{SS}=-7V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Control Input crosstalk to switch (for DATA, STROBE, Address)	CX_{talk}		30		mVpp	$V_{IN}=3V+V_{DC}$ squarewave; R_{IN}=1kΩ, R_L=10kΩ. See Appendix, Fig. A.6
2	Digital Input Capacitance	C_{DI}		10		pF	f=1MHz
3	Switching Frequency	F_O			20	MHz	
4	Setup Time DATA to STROBE	t_{DS}	10			ns	R_L= 1kΩ, C_L=50pF ①
5	Hold Time DATA to STROBE	t_{DH}	10			ns	R_L= 1kΩ, C_L=50pF ①
6	Setup Time Address to STROBE	t_{AS}	10			ns	R_L= 1kΩ, C_L=50pF ①
7	Hold Time Address to STROBE	t_{AH}	10			ns	R_L= 1kΩ, C_L=50pF ①
8	STROBE Pulse Width	t_{SPW}	20			ns	R_L= 1kΩ, C_L=50pF ①
9	RESET Pulse Width	t_{RPW}	40			ns	R_L= 1kΩ, C_L=50pF ①
10	STROBE to Switch Status Delay	t_S		40	100	ns	R_L=1kΩ, C_L=50 pF ①
11	DATA to Switch Status Delay	t_D		50	100	ns	R_L=1kΩ, C_L=50 pF ①
12	RESET to Switch Status Delay	t_R		35	100	ns	R_L=1kΩ, C_L=50 pF ①

† Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
Digital Input rise time (tr) and fall time (tf) = 5ns.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
① Refer to Appendix, Fig. A.7 for test circuit.

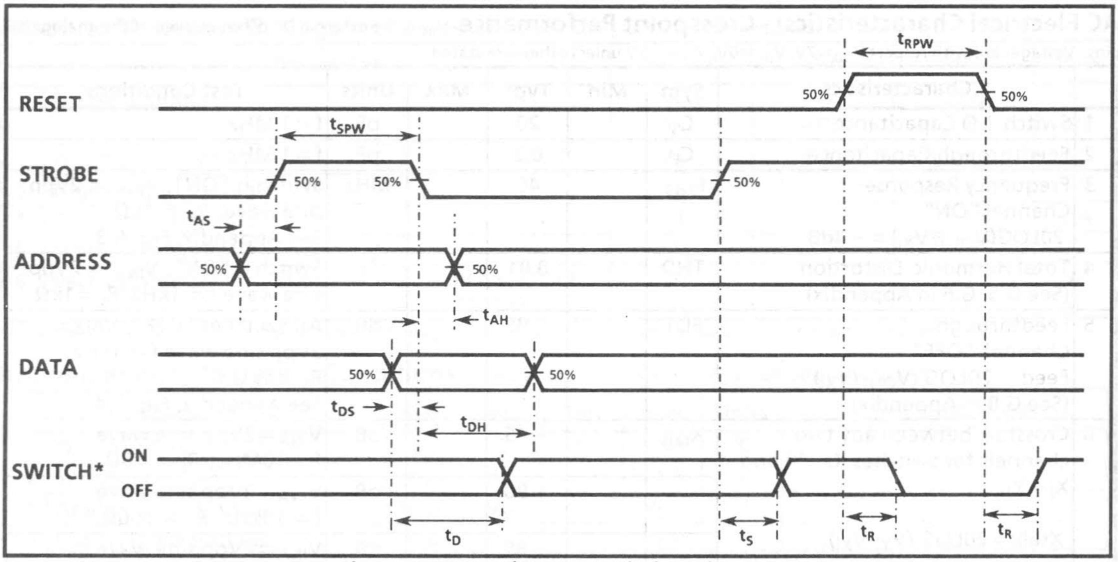


Figure 2 - Control Memory Timing Diagram

*See Appendix, Fig. A.7 for switching waveform

AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection
0	0	0	0	0	0	0	X0-Y0
1	0	0	0	0	0	0	X1-Y0
0	1	0	0	0	0	0	X2-Y0
1	1	0	0	0	0	0	X3-Y0
0	0	1	0	0	0	0	X4-Y0
1	0	1	0	0	0	0	X5-Y0
0	1	1	0	0	0	0	No Connection[①]
1	1	1	0	0	0	0	No Connection[①]
0	0	0	1	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
0	1	0	1	0	0	0	X8-Y0
1	1	0	1	0	0	0	X9-Y0
0	0	1	1	0	0	0	X10-Y0
1	0	1	1	0	0	0	X11-Y0
0	1	1	1	0	0	0	No Connection[①]
1	1	1	1	0	0	0	No Connection[①]
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	0 ↓ 0	X0-Y1 ↓ X11-Y1
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	0 ↓ 0	X0-Y2 ↓ X11-Y2
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	0 ↓ 0	X0-Y3 ↓ X11-Y3
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	0 ↓ 0	1 ↓ 1	X0-Y4 ↓ X11-Y4
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	1 ↓ 1	X0-Y5 ↓ X11-Y5
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	1 ↓ 1	X0-Y6 ↓ X11-Y6
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	1 ↓ 1	X0-Y7 ↓ X11-Y7

Table 1 - Address Decode Truth Table

①This address has no effect on device status.

Pin Description

Pin #*	Name	Description
1	Y3	**Y3 Analog (Input/Output):** this is connected to the Y3 column of the switch array.
2	AY2	**Y2 Address Line (Input).**
3	RESET	**Master RESET (Input):** this is used to turn off all switches. Active High.
4,5	AX3,AX0	**X3 and X0 Address Lines (Inputs).**
6,7	NC	**No Connection.**
8-13	X6-X11	**X6-X11 Analog (Inputs/Outputs):** these are connected to the X6-X11 rows of the switch array.
14	NC	**No Connection.**
15	Y7	**Y7 Analog (Input/Output):** this is connected to the Y7 column of the switch array.
16	NC	**No Connection.**
17	Y6	**Y6 Analog (Input/Output):** this is connected to the Y6 column of the switch array.
18	STROBE	**STROBE (Input):** enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High.
19	Y5	**Y5 Analog (Input/Output):** this is connected to the Y5 column of the switch array.
20	VSS	**Ground Reference.**
21	Y4	**Y4 Analog (Input/Output):** this is connected to the Y4 column of the switch array.
22, 23	AX1,AX2	**X1 and X2 Address Lines (Inputs).**
24, 25	AY0,AY1	**Y0 and Y1 Address Lines (Inputs).**
26, 27	NC	**No Connection.**
28 - 33	X5-X0	**X5-X0 Analog (Inputs/Outputs):** these are connected to the X5-X0 rows of the switch array.
34	NC	**No Connection.**
35	Y0	**Y0 Analog (Input/Output):** this is connected to the Y0 column of the switch array.
36	NC	**No Connection.**
37	Y1	**Y1 Analog (Input/Output):** this is connected to the Y1 column of the switch array.
38	DATA	**DATA (Input):** a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
39	Y2	**Y2 Analog (Input/Output):** this is connected to the Y2 column of the switch array.
40	VDD	**Positive Power Supply.**

* Plastic DIP and CERDIP only.

Functional Description

The MT8812 is an analog switch matrix with an array size of 8×12. The switch array is arranged such that there are 8 columns by 12 rows. The columns are referred to as the Y input/output lines and the rows are the X input/output lines. The crosspoint analog switch array will interconnect any X line with any Y line when turned on and provide a high degree of isolation when turned off. The control memory consists of a 96 bit write only RAM in which the bits are selected by the address input lines (AY0-AY2, AX0-AX3). Data is presented to the memory on the DATA input line. Data is asynchronously written into memory whenever the STROBE input is high and is latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y lines can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input line will asynchronously return all memory locations to logical "0" turning off all crosspoint switches.

Address Decode

The seven address lines along with the STROBE input are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low while the address and data lines are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn on and off in accordance with the data. Data must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

MITEL

ISO-CMOS MT093
8 x 12 Analog Switch Array

9161-002-131-NA ISSUE 1 January 1990

Features

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage: 4.5V to 14.5V
- 3.5Vpp analog signal capability
- R_{ON} 65Ω max. @ V_{DD}=14V, 25°C
- $\Delta R_{ON} \leq 10\Omega$ @ V_{DD}=14V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Low power consumption ISO-CMOS technology

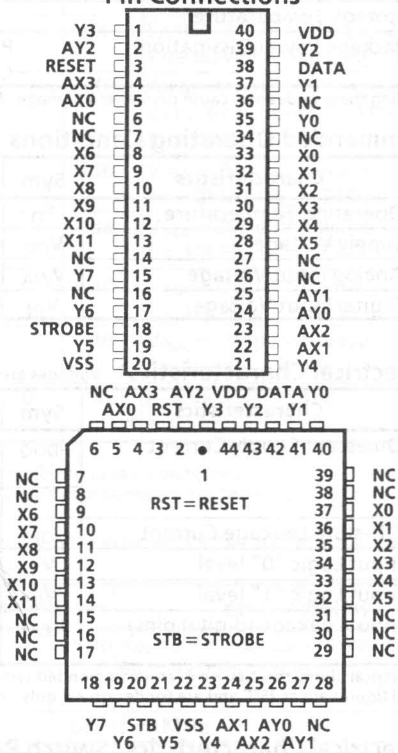
Applications

- PBX systems
- Mobile radio
- Test equipment /instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Description

The Mitel MT093 is fabricated in MITEL's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8×12 array of crosspoint switches along with a 7 to 96 line decoder and latch circuits. Any one of the 96 switches can be addressed by selecting the appropriate seven input bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input.

Pin Connections



Ordering Information 0° to 70°C

MT093AC	40 Pin CERDIP
MT093AE	40 Pin PLASTIC DIP
MT093AP	44 Pin PLCC

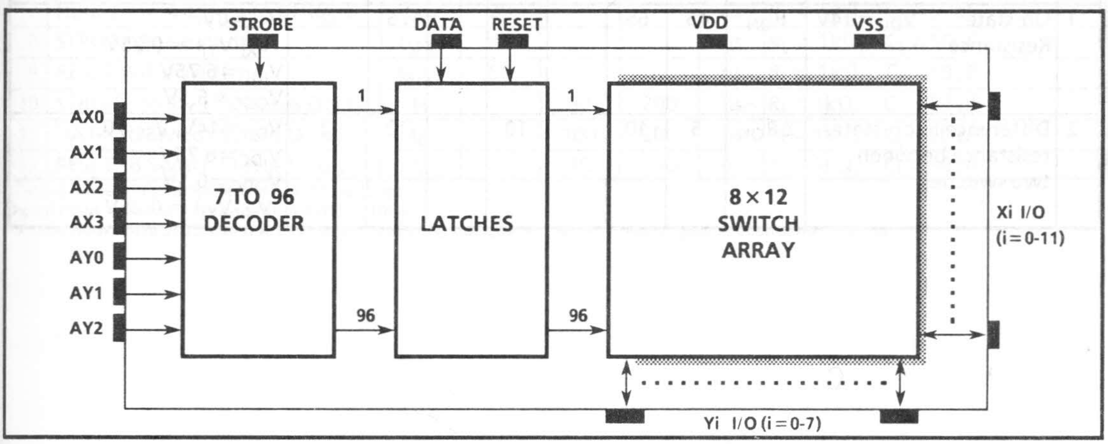


Figure 1- Functional Block Diagram

Absolute Maximum Ratings* - Voltages are with respect to V_{SS} unless otherwise stated.

	Parameter		Symbol	Min	Max	Units
1	Supply Voltage		V_{DD} V_{SS}	−0.3 −0.3	16.0 V_{DD}+0.3	V V
2	Analog Input Voltage		V_{INA}	−0.3	V_{DD}+0.3	V
3	Digital Input Voltage		V_{IN}	V_{SS}−0.3	V_{DD}+0.3	V
4	Current on any I/O Pin		I		±15	mA
5	Storage Temperature		T_S	−65	+150	°C
6	Package Power Dissipation	PLASTIC DIP CERDIP	P_D P_D		0.6 1.0	W W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{SS} unless otherwise stated

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T_O	0	25	70	°C	
2	Supply Voltage	V_{DD}	4.5		14.5	V	
3	Analog Input Voltage	V_{INA}	V_{SS}		3.5	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics† - Voltages are with respect to V_{SS}=0V and V_{DD}=14V unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DDQ}		1	100	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}
				7	15	mA	All digital inputs at V_{IN}=2.4V
2	Off-state Leakage Current	I_{OFF}			±1	μA	$\|V_{Xi}-V_{Yj}\|=V_{DD}-V_{SS}$
3	Input Logic "0" level	V_{IL}			0.8	V	
4	Input Logic "1" level	V_{IH}	2.4			V	
5	Input Leakage (digital pins)	I_{LEAK}			10	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Switch Resistance - V_{IDC}/V_{ODC} is the external DC offset applied at the analog I/O pins.

	Characteristics	Sym	25°C		60°C		70°C		Units	Test Conditions
			Typ	Max	Typ	Max	Typ	Max		
1	On-state Resistance V_{DD}=14V	R_{ON}	45	65				75	Ω	V_{SS}=0V, $\|V_{Xi}-V_{Yj}\|$ = 0.25V V_{IDC}=6.75V V_{ODC}=6.5V
2	Difference in on-state resistance between two switches	ΔR_{ON}	5	10		10		10	Ω	V_{DD}=14V, V_{SS}=0, V_{IDC}=6.75V V_{ODC}=6.5V $\|V_{Xi}-V_{Yj}\|$ = 0.25V

AC Electrical Characteristics† - Crosspoint Performance- V_{DC} is the external DC offset applied at the analog I/O pins. Voltages are with respect $V_{DD}=7V$, $V_{DC}=0V$, $V_{SS}=-7V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f = 1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f = 1 MHz
3	Frequency Response Channel "ON" 20LOG(V_{OUT}/V_{Xi}) = −3dB	F_{3dB}		45		MHz	Switch is "ON"; V_{INA} = 2Vpp sine wave; R_L = 1kΩ
4	Total Harmonic Distortion	THD		0.05		%	Switch is "ON"; V_{INA} = 2Vpp sine wave f = 1kHz; R_L = 1kΩ
5	Feedthrough Channel "OFF" Feed. = 20LOG (V_{OUT}/V_{Xi})	FDT		−95		dB	All Switches "OFF"; V_{INA} = 2Vpp sine wave f = 1kHz; R_L = 1kΩ.
6	Crosstalk between any two channels for switches Xi − Yi and Xj − Yj. Xtalk = 20LOG (V_{Yj}/V_{Xi}).	X_{talk}		−45		dB	V_{INA} = 2Vpp sine wave f = 10MHz; R_L = 75Ω.
				−90		dB	V_{INA} = 2Vpp sine wave f = 10kHz; R_L = 600Ω.
				−85		dB	V_{INA} = 2Vpp sine wave f = 10kHz; R_L = 1kΩ.
				−80		dB	V_{INA} = 2Vpp sine wave f = 1kHz; R_L = 10kΩ.
7	Propagation delay through switch	t_{PS}			50	ns	R_L = 1kΩ; C_L = 50pF

† Timing is over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5dB better.

AC Electrical Characteristics† - Control and I/O Timings- V_{DC} is the external DC offset applied at the analog I/O pins. Voltages are with respect $V_{DD}=7V$, $V_{DC}=0V$, $V_{SS}=-7V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Control Input crosstalk to switch (for DATA, STROBE, Address)	CX_{talk}		50		mVpp	V_{IN} = 3V + V_{DC} squarewave; R_{IN} = 1kΩ, R_L = 10kΩ.
2	Digital Input Capacitance	C_{DI}		10		pF	f = 1MHz
3	Switching Frequency	F_O			10	MHz	
4	Setup Time DATA to STROBE	t_{DS}	20			ns	R_L = 1kΩ, C_L = 50pF
5	Hold Time DATA to STROBE	t_{DH}	20			ns	R_L = 1kΩ, C_L = 50pF
6	Setup Time Address to STROBE	t_{AS}	.20			ns	R_L = 1kΩ, C_L = 50pF
7	Hold Time Address to STROBE	t_{AH}	20			ns	R_L = 1kΩ, C_L = 50pF
8	STROBE Pulse Width	t_{SPW}	40			ns	R_L = 1kΩ, C_L = 50pF
9	RESET Pulse Width	t_{RPW}	80			ns	R_L = 1kΩ, C_L = 50pF
10	STROBE to Switch Status Delay	t_S		80	200	ns	R_L = 1kΩ, C_L = 50 pF
11	DATA to Switch Status Delay	t_D		100	200	ns	R_L = 1kΩ, C_L = 50 pF
12	RESET to Switch Status Delay	t_R		70	200	ns	R_L = 1kΩ, C_L = 50 pF

† Timing is over recommended temperature range.
Digital Input rise time (tr) and fall time (tf) = 10ns.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

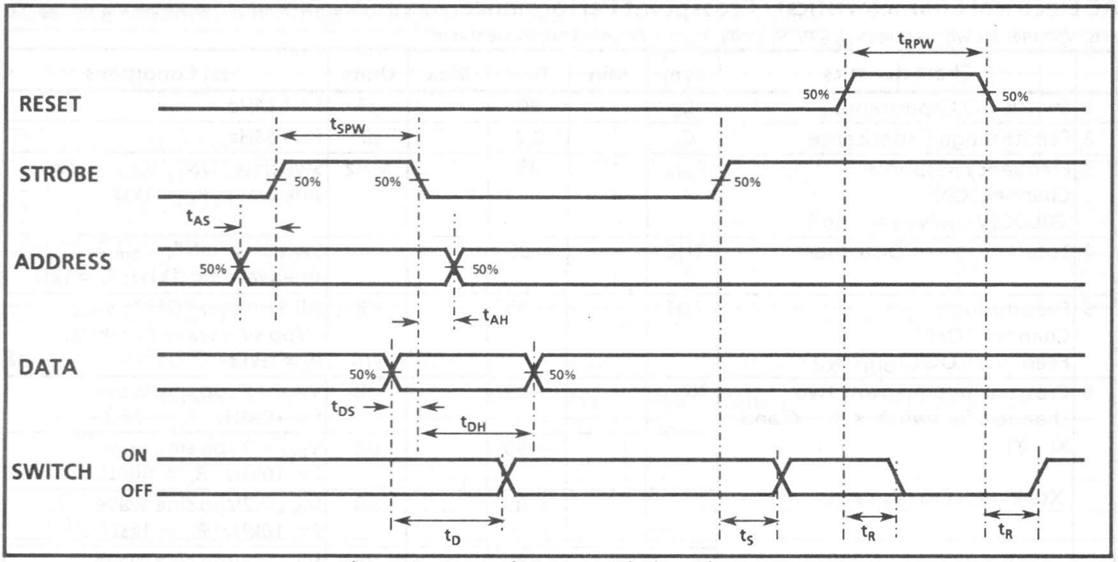


Figure 2 - Control Memory Timing Diagram

AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection
0	0	0	0	0	0	0	X0-Y0
1	0	0	0	0	0	0	X1-Y0
0	1	0	0	0	0	0	X2-Y0
1	1	0	0	0	0	0	X3-Y0
0	0	1	0	0	0	0	X4-Y0
1	0	1	0	0	0	0	X5-Y0
0	1	1	0	0	0	0	No Connection[①]
1	1	1	0	0	0	0	No Connection[①]
0	0	0	1	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
0	1	0	1	0	0	0	X8-Y0
1	1	0	1	0	0	0	X9-Y0
0	0	1	1	0	0	0	X10-Y0
1	0	1	1	0	0	0	X11-Y0
0	1	1	1	0	0	0	No Connection[①]
1	1	1	1	0	0	0	No Connection[①]
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	0 ↓ 0	X0-Y1 ↓ ↓ X11-Y1
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	0 ↓ 0	X0-Y2 ↓ ↓ X11-Y2
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	0 ↓ 0	X0-Y3 ↓ ↓ X11-Y3
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	0 ↓ 0	1 ↓ 1	X0-Y4 ↓ ↓ X11-Y4
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	1 ↓ 1	X0-Y5 ↓ ↓ X11-Y5
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	1 ↓ 1	X0-Y6 ↓ ↓ X11-Y6
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	1 ↓ 1	X0-Y7 ↓ ↓ X11-Y7

Table 1 - Address Decode Truth Table

[①]This address has no effect on device status.

Pin Description

Pin #*	Name	Description
1	Y3	**Y3 Analog (Input/Output):** this is connected to the Y3 column of the switch array.
2	AY2	**Y2 Address Line (Input).**
3	RESET	**Master RESET (Input):** this is used to turn off all switches. Active High.
4,5	AX3,AX0	**X3 and X0 Address Lines (Inputs).**
6,7	NC	**No Connection.**
8-13	X6-X11	**X6-X11 Analog (Inputs/Outputs):** these are connected to the X6-X11 rows of the switch array.
14	NC	**No Connection.**
15	Y7	**Y7 Analog (Input/Output):** this is connected to the Y7 column of the switch array.
16	NC	No Connection.
17	Y6	**Y6 Analog (Input/Output):** this is connected to the Y6 column of the switch array.
18	STROBE	**STROBE (Input):** enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High.
19	Y5	**Y5 Analog (Input/Output):** this is connected to the Y5 column of the switch array.
20	VSS	**Ground Reference.**
21	Y4	**Y4 Analog (Input/Output):** this is connected to the Y4 column of the switch array.
22, 23	AX1,AX2	**X1 and X2 Address Lines (Inputs).**
24, 25	AY0,AY1	**Y0 and Y1 Address Lines (Inputs).**
26, 27	NC	**No Connection.**
28 - 33	X5-X0	**X5-X0 Analog (Inputs/Outputs):** these are connected to the X5-X0 rows of the switch array.
34	NC	**No Connection.**
35	Y0	**Y0 Analog (Input/Output):** this is connected to the Y0 column of the switch array.
36	NC	**No Connection.**
37	Y1	**Y1 Analog (Input/Output):** this is connected to the Y1 column of the switch array.
38	DATA	**DATA (Input):** a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
39	Y2	**Y2 Analog (Input/Output):** this is connected to the Y2 column of the switch array.
40	VDD	**Positive Power Supply.**

* Plastic DIP and CERDIP only.

Functional Description

The MT093 is an analog switch matrix with an array size of 8×12. The switch array is arranged such that there are 8 columns by 12 rows. The columns are referred to as the Y input/output lines and the rows are the X input/output lines. The crosspoint analog switch array will interconnect any X line with any Y line when turned on and provide a high degree of isolation when turned off. The control memory consists of a 96 bit write only RAM in which the bits are selected by the address input lines (AY0-AY2, AX0-AX3). Data is presented to the memory on the DATA input line. Data is asynchronously written into memory whenever the STROBE input is high and is latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y lines can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input line will asynchronously return all memory locations to logical "0" turning off all crosspoint switches.

Address Decode

The seven address lines along with the STROBE input are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low while the address and data lines are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn on and off in accordance with the data. Data must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

8 x 12 Analog Switch Array

9161-002-100-NA ISSUE 2 November 1988

2

Features

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage: 4.5V to 13.2V
- 12Vpp analog signal capability
- R_{ON} 65Ω max. @ V_{DD}=12V, 25°C
- ΔR_{ON} ≤10Ω @ V_{DD}=12V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Separate analog and digital reference supplies
- Low power consumption ISO-CMOS technology

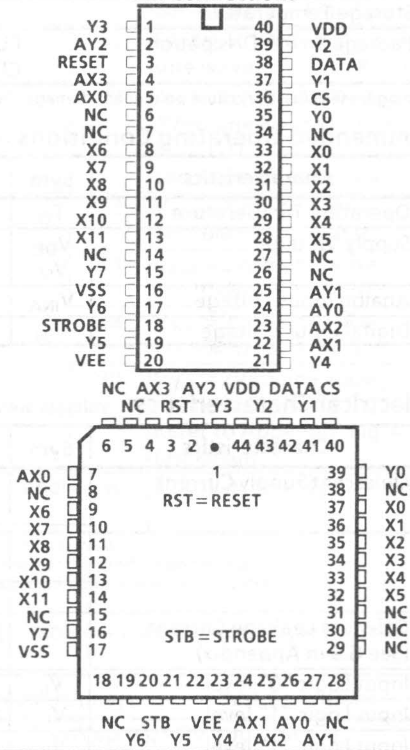
Applications

- Key systems
- PBX systems
- Mobile radio
- Test equipment /instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Description

The Mitel MT8814 is fabricated in MITEL's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8×12 array of crosspoint switches along with a 7 to 96 line decoder and latch circuits. Any one of the 96 switches can be addressed by selecting the appropriate seven address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. V_{SS} is the ground reference of the digital inputs. The range of the analog signal is from V_{DD} to V_{EE}. Chip Select (CS) allows the crosspoint array to be cascaded for matrix expansion.

Pin Connections



Ordering Information -40° to 85°C

MT8814AC	40 Pin CERDIP
MT8814AE	40 Pin PLASTIC DIP
MT8814AP	44 Pin PLCC

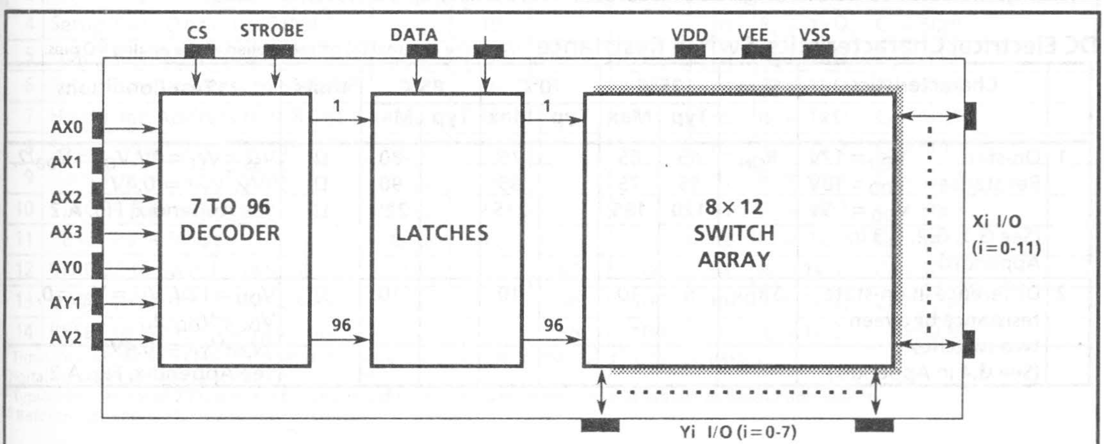


Figure 1- Functional Block Diagram

Absolute Maximum Ratings* - Voltages are with respect to V_{EE} unless otherwise stated

	Parameter		Symbol	Min	Max	Units
1	Supply Voltage		V_{DD} V_{SS}	−0.3 −0.3	15.0 $V_{DD}+0.3$	V V
2	Analog Input Voltage		V_{INA}	−0.3	$V_{DD}+0.3$	V
3	Digital Input Voltage		V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
4	Current on any I/O Pin		I		±15	mA
5	Storage Temperature		T_S	−65	+150	°C
6	Package Power Dissipation	PLASTIC DIP CERDIP	P_D P_D		0.6 1.0	W W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{EE} unless otherwise stated

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T_O	−40	25	85	°C	
2	Supply Voltage	V_{DD} V_{SS}	4.5 V_{EE}		13.2 $V_{DD}-4.5$	V V	
3	Analog Input Voltage	V_{INA}	V_{EE}		V_{DD}	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics† - Voltages are with respect to $V_{EE}=V_{SS}=0V$, $V_{DD}=12V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DD}		1	100	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}
				0.4	1.5	mA	All digital inputs at $V_{IN}=2.4+V_{SS}$; $V_{SS}=7.0V$
				5	15	mA	All digital inputs at $V_{IN}=3.4V$
2	Off-state Leakage Current (See G.9 in Appendix)	I_{OFF}		±1	±500	nA	$\lvert V_{Xi}-V_{Yj}\rvert = V_{DD}-V_{EE}$ See Appendix, Fig. A.1
3	Input Logic "0" level	V_{IL}			$0.8+V_{SS}$	V	$V_{SS}=7.5V$; $V_{EE}=0V$
4	Input Logic "1" level	V_{IH}	$2.0+V_{SS}$			V	$V_{SS}=6.5V$; $V_{EE}=0V$
5	Input Logic "1" level	V_{IH}	3.3			V	
6	Input Leakage (digital pins)	I_{LEAK}		0.1	10	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}

† DC Electrical Characteristics are over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics- Switch Resistance - V_{DC} is the external DC offset applied at the analog I/O pins.

	Characteristics	Sym	25°C		70°C		85°C		Units	Test Conditions
			Typ	Max	Typ	Max	Typ	Max		
1	On-state Resistance $V_{DD}=12V$ $V_{DD}=10V$ $V_{DD}=5V$ (See G.1, G.2, G.3 in Appendix)	R_{ON}	45 55 120	65 75 185		75 85 215		80 90 225	Ω Ω Ω	$V_{SS}=V_{EE}=0V, V_{DC}=V_{DD}/2$, $\lvert V_{Xi}-V_{Yj}\rvert = 0.4V$ See Appendix, Fig. A.2
2	Difference in on-state resistance between two switches (See G.4 in Appendix)	ΔR_{ON}	5	10		10		10	Ω	$V_{DD}=12V$, $V_{SS}=V_{EE}=0$, $V_{DC}=V_{DD}/2$, $\lvert V_{Xi}-V_{Yj}\rvert = 0.4V$ See Appendix, Fig. A.2

2

AC Electrical Characteristics† - Crosspoint Performance - Voltages are with respect to $V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-7V$, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f=1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f=1 MHz
3	Frequency Response Channel "ON" $20LOG(V_{OUT}/V_{Xi})=-3dB$	F_{3dB}		45		MHz	Switch is "ON"; V_{INA} = 2Vpp sine wave; R_L = 1kΩ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; V_{INA} = 2Vpp sine wave f= 1kHz; R_L=1kΩ
5	Feedthrough Channel "OFF" Feed.=$20LOG(V_{OUT}/V_{Xi})$ (See G.8 in Appendix)	FDT		−95		dB	All Switches "OFF"; V_{INA}= 2Vpp sine wave f= 1kHz; R_L= 1kΩ. See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi−Yi and Xj−Yj. Xtalk=$20LOG(V_{Yj}/V_{Xi})$. (See G.7 in Appendix).	X_{talk}		−45		dB	V_{INA}=2Vpp sine wave f= 10MHz; R_L = 75Ω.
				−90		dB	V_{INA}=2Vpp sine wave f= 10kHz; R_L = 600Ω.
				−85		dB	V_{INA}=2Vpp sine wave f= 10kHz; R_L = 1kΩ.
				−80		dB	V_{INA}=2Vpp sine wave f= 1kHz; R_L = 10kΩ. Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t_{PS}			30	ns	R_L=1kΩ; C_L=50pF

† Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5dB better.

AC Electrical Characteristics† - Control and I/O Timings - Voltages are with respect to $V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-7V$, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Control Input crosstalk to switch (for CS, DATA, STROBE, Address)	CX_{talk}		30		mVpp	V_{IN}=3V squarewave; R_{IN}=1kΩ, R_L=10kΩ. See Appendix, Fig. A.6
2	Digital Input Capacitance	C_{DI}		10		pF	f=1MHz
3	Switching Frequency	F_O			20	MHz	
4	Setup Time DATA to STROBE	t_{DS}	10			ns	R_L= 1kΩ, C_L=50pF ①
5	Hold Time DATA to STROBE	t_{DH}	10			ns	R_L= 1kΩ, C_L=50pF ①
6	Setup Time Address to STROBE	t_{AS}	10			ns	R_L= 1kΩ, C_L=50pF ①
7	Hold Time Address to STROBE	t_{AH}	10			ns	R_L= 1kΩ, C_L=50pF ①
8	Setup Time CS to STROBE	t_{CSS}	10			ns	R_L= 1kΩ, C_L=50pF ①
9	Hold Time CS to STROBE	t_{CSH}	10			ns	R_L= 1kΩ, C_L=50pF ①
10	STROBE Pulse Width	t_{SPW}	20			ns	R_L= 1kΩ, C_L=50pF ①
11	RESET Pulse Width	t_{RPW}	40			ns	R_L= 1kΩ, C_L=50pF ①
12	STROBE to Switch Status Delay	t_S		40	100	ns	R_L=1kΩ, C_L=50 pF ①
13	DATA to Switch Status Delay	t_D		50	100	ns	R_L=1kΩ, C_L=50 pF ①
14	RESET to Switch Status Delay	t_R		35	100	ns	R_L=1kΩ, C_L=50 pF ①

† Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
Digital Input rise time (tr) and fall time (tf) = 5ns.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
① Refer to Appendix, Fig. A.7 for test circuit.

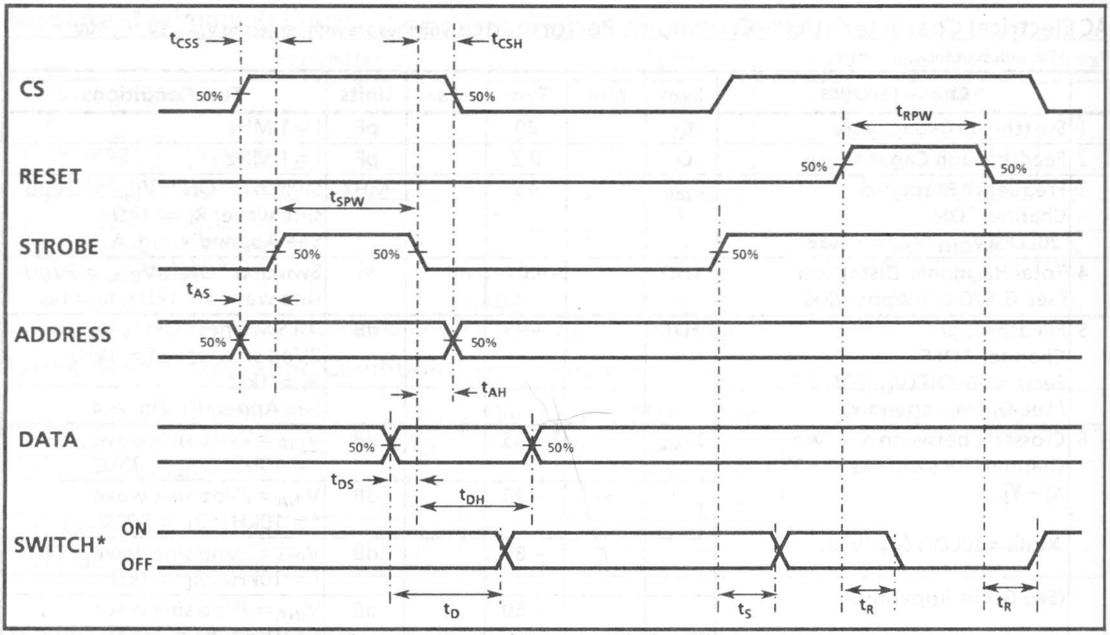


Figure 2 - Control Memory Timing Diagram

*See Appendix, Fig. A.7 for switching waveform

AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection
0	0	0	0	0	0	0	X0-Y0
1	0	0	0	0	0	0	X1-Y0
0	1	0	0	0	0	0	X2-Y0
1	1	0	0	0	0	0	X3-Y0
0	0	1	0	0	0	0	X4-Y0
1	0	1	0	0	0	0	X5-Y0
0	1	1	0	0	0	0	No Connection[1]
1	1	1	0	0	0	0	No Connection[1]
0	0	0	1	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
0	1	0	1	0	0	0	X8-Y0
1	1	0	1	0	0	0	X9-Y0
0	0	1	1	0	0	0	X10-Y0
1	0	1	1	0	0	0	X11-Y0
0	1	1	1	0	0	0	No Connection[1]
1	1	1	1	0	0	0	No Connection[1]
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	0 ↓ 0	X0-Y1 ↓ ↓ X11-Y1
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	0 ↓ 0	X0-Y2 ↓ ↓ X11-Y2
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	0 ↓ 0	X0-Y3 ↓ ↓ X11-Y3
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	0 ↓ 0	1 ↓ 1	X0-Y4 ↓ ↓ X11-Y4
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	1 ↓ 1	X0-Y5 ↓ ↓ X11-Y5
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	1 ↓ 1	X0-Y6 ↓ ↓ X11-Y6
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	1 ↓ 1	X0-Y7 ↓ ↓ X11-Y7

Table 1 - Address Decode Truth Table

[1] This address has no effect on device status

Pin Description

Pin #*	Name	Description
1	Y3	**Y3 Analog (Input/Output):** this is connected to the Y3 column of the switch array.
2	AY2	**Y2 Address Line (Input).**
3	RESET	**Master RESET (Input):** this is used to turn off all switches regardless of the condition of CS. Active High.
4,5	AX3,AX0	**X3 and X0 Address Lines (Inputs).**
6,7	NC	**No Connection.**
8-13	X6-X11	**X6-X11 Analog (Inputs/Outputs):** these are connected to the X6-X11 rows of the switch array.
14	NC	**No Connection**
15	Y7	**Y7 Analog (Input/Output):** this is connected to the Y7 column of the switch array.
16	VSS	**Digital Ground Reference .**
17	Y6	**Y6 Analog (Input/Output):** this is connected to the Y6 column of the switch array.
18	STROBE	**STROBE (Input):** enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High.
19	Y5	**Y5 Analog (Input/Output):** this is connected to the Y5 column of the switch array.
20	VEE	**Negative Power Supply.**
21	Y4	**Y4 Analog (Input/Output):** this is connected to the Y4 column of the switch array.
22, 23	AX1,AX2	**X1 and X2 Address Lines (Inputs).**
24, 25	AY0,AY1	**Y0 and Y1 Address Lines (Inputs).**
26, 27	NC	**No Connection.**
28 - 33	X5-X0	**X5-X0 Analog (Inputs/Outputs):** these are connected to the X5-X0 rows of the switch array.
34	NC	**No Connection.**
35	Y0	**Y0 Analog (Input/Output):** this is connected to the Y0 column of the switch array.
36	CS	**Chip Select (Input):** this is used to select the device. Active High.
37	Y1	**Y1 Analog (Input/Output):** this is connected to the Y1 column of the switch array.
38	DATA	**DATA (Input):** a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
39	Y2	**Y2 Analog (Input/Output):** this is connected to the Y2 column of the switch array.
40	VDD	**Positive Power Supply.**

* Plastic DIP and CERDIP only

Functional Description

The MT8814 is an analog switch matrix with an array size of 8×12. The switch array is arranged such that there are 8 columns by 12 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 96 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX3). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever both the CS (Chip Select) and STROBE inputs are high and are latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input will asynchronously return all memory locations to logical "0" turning off all crosspoint switches regardless of whether CS is high or low. Two voltage reference pins (V_{SS} and V_{EE}) are provided for the MT8814 to enable switching of negative analog signals. The range for digital signals is from V_{DD} to V_{SS} while the range for analog signals is from V_{DD} to V_{EE}. V_{SS} and V_{EE} pins can be tied together if a single voltage reference is needed.

Address Decode

The seven address inputs along with the STROBE and CS (Chip Select) are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low and CS must go high while the address and data are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

ISO-CMOS MT8815
8×12 Analog Switch Array

9161-002-104-NA ISSUE 1 November 1988

Features

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage: 4.5V to 13.2V
- 12Vpp analog signal capability
- R_{ON} 65Ω max. @ V_{DD}=12V, 25°C
- $\Delta R_{ON} \leq 10\Omega$ @ V_{DD}=12V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Separate analog and digital reference supplies
- Low power consumption ISO-CMOS technology

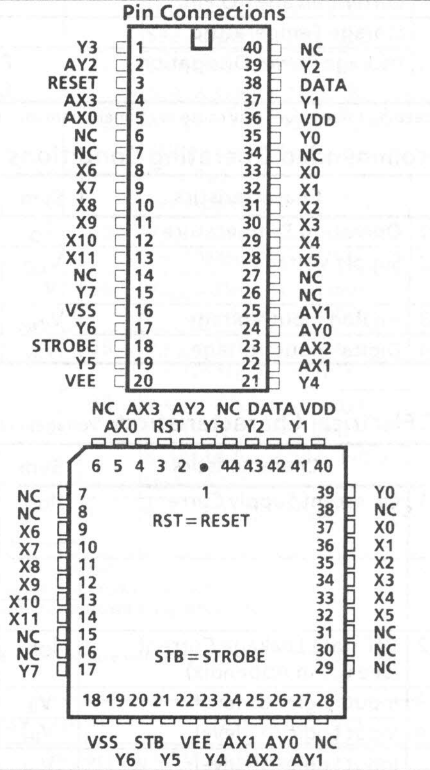
Applications

- Key systems
- PBX systems
- Mobile radio
- Test equipment /instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Description

The Mitel MT8815 is fabricated in MITEL's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8×12 array of crosspoint switches along with a 7 to 96 line decoder and latch circuits. Any one of the 96 switches can be addressed by selecting the appropriate seven address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. V_{SS} is the ground reference of the digital inputs. The range of the analog signal is from V_{DD} to V_{EE}.

Pin Connections



Ordering Information -40° to 85°C

MT8815AC	40 Pin CERDIP
MT8815AE	40 Pin PLASTIC DIP
MT8815AP	44 Pin PLCC

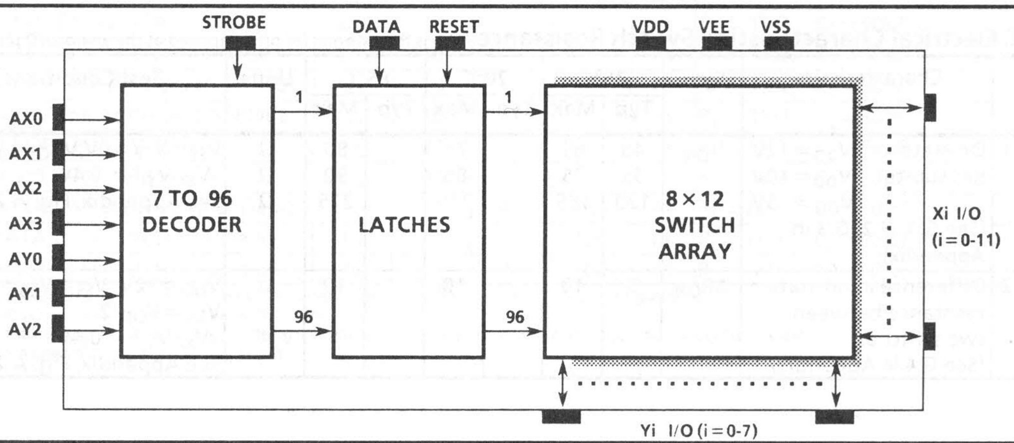


Figure 1- Functional Block Diagram

Absolute Maximum Ratings* - Voltages are with respect to V_{EE} unless otherwise stated.

	Parameter		Symbol	Min	Max	Units
1	Supply Voltage		V_{DD} V_{SS}	−0.3 −0.3	15.0 $V_{DD}+0.3$	V V
2	Analog Input Voltage		V_{INA}	−0.3	$V_{DD}+0.3$	V
3	Digital Input Voltage		V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
4	Current on any I/O Pin		I		±15	mA
5	Storage Temperature		T_S	−65	+150	°C
6	Package Power Dissipation	PLASTIC DIP CERDIP	P_D P_D		0.6 1.0	W W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{EE} unless otherwise stated.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T_O	−40	25	85	°C	
2	Supply Voltage	V_{DD} V_{SS}	4.5 V_{EE}		13.2 $V_{DD}-4.5$	V V	
3	Analog Input Voltage	V_{INA}	V_{EE}		V_{DD}	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics† - Voltages are with respect to $V_{EE}=V_{SS}=0V$, $V_{DD}=12V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DD}		1	100	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}
				0.4	1.5	mA	All digital inputs at $V_{IN}=2.4+V_{SS}$; $V_{SS}=7.0V$
				5	15	mA	All digital inputs at $V_{IN}=3.4V$
2	Off-state Leakage Current (See G.9 in Appendix)	I_{OFF}		±1	±500	nA	$\lvert V_{Xi}-V_{Yj}\rvert = V_{DD}-V_{EE}$ See Appendix, Fig. A.1
3	Input Logic "0" level	V_{IL}			$0.8+V_{SS}$	V	$V_{SS}=7.5V$; $V_{EE}=0V$
4	Input Logic "1" level	V_{IH}	$2.0+V_{SS}$			V	$V_{SS}=6.5V$; $V_{EE}=0V$
5	Input Logic "1" level	V_{IH}	3.3			V	
6	Input Leakage (digital pins)	I_{LEAK}		0.1	10	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}

† DC Electrical Characteristics are over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics- Switch Resistance - V_{DC} is the external DC offset applied at the analog I/O pins.

	Characteristics		Sym	25°C		70°C		85°C		Units	Test Conditions
				Typ	Max	Typ	Max	Typ	Max		
1	On-state Resistance (See G.1, G.2, G.3 in Appendix)	$V_{DD}=12V$ $V_{DD}=10V$ $V_{DD}=5V$	R_{ON}	45 55 120	65 75 185		75 85 215		80 90 225	Ω Ω Ω	$V_{SS}=V_{EE}=0V$, $V_{DC}=V_{DD}/2$, $\lvert V_{Xi}-V_{Yj}\rvert = 0.4V$ See Appendix, Fig. A.2
2	Difference in on-state resistance between two switches (See G.4 in Appendix)		ΔR_{ON}	5	10		10		10	Ω	$V_{DD}=12V$, $V_{SS}=V_{EE}=0$, $V_{DC}=V_{DD}/2$, $\lvert V_{Xi}-V_{Yj}\rvert = 0.4V$ See Appendix, Fig. A.2

AC Electrical Characteristics† - Crosspoint Performance

-Voltages are with respect to $V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-7V$, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f=1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f=1 MHz
3	Frequency Response Channel "ON" $20LOG(V_{OUT}/V_{Xi})=-3dB$	F_{3dB}		45		MHz	Switch is "ON"; V_{INA} = 2Vpp sine wave; R_L = 1kΩ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; V_{INA} = 2Vpp sine wave f= 1kHz; R_L=1kΩ
5	Feedthrough Channel "OFF" Feed.=20LOG (V_{OUT}/V_{Xi}) (See G.8 in Appendix)	FDT		−95		dB	All Switches "OFF"; V_{INA}= 2Vpp sine wave f= 1kHz; R_L= 1kΩ. See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi−Yi and Xj−Yj. Xtalk=20LOG (V_{Yj}/V_{Xi}). (See G.7 in Appendix).	X_{talk}		−45		dB	V_{INA}=2Vpp sine wave f= 10MHz; R_L = 75Ω.
				−90		dB	V_{INA}=2Vpp sine wave f= 10kHz; R_L = 600Ω.
				−85		dB	V_{INA}=2Vpp sine wave f= 10kHz; R_L = 1kΩ.
				−80		dB	V_{INA}=2Vpp sine wave f= 1kHz; R_L = 10kΩ. Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t_{PS}			30	ns	R_L=1kΩ; C_L=50pF

† Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5dB better.

AC Electrical Characteristics† - Control and I/O Timings

- Voltages are with respect to $V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-7V$, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Control Input crosstalk to switch (for DATA, STROBE, Address)	CX_{talk}		30		mVpp	V_{IN}=3V squarewave; R_{IN}=1kΩ, R_L=10kΩ. See Appendix, Fig. A.6
2	Digital Input Capacitance	C_{DI}		10		pF	f=1MHz
3	Switching Frequency	F_O			20	MHz	
4	Setup Time DATA to STROBE	t_{DS}	10			ns	R_L= 1kΩ, C_L=50pF ①
5	Hold Time DATA to STROBE	t_{DH}	10			ns	R_L= 1kΩ, C_L=50pF ①
6	Setup Time Address to STROBE	t_{AS}	10			ns	R_L= 1kΩ, C_L=50pF ①
7	Hold Time Address to STROBE	t_{AH}	10			ns	R_L= 1kΩ, C_L=50pF ①
8	STROBE Pulse Width	t_{SPW}	20			ns	R_L= 1kΩ, C_L=50pF ①
9	RESET Pulse Width	t_{RPW}	40			ns	R_L= 1kΩ, C_L=50pF ①
10	STROBE to Switch Status Delay	t_S		40	100	ns	R_L=1kΩ, C_L=50 pF ①
11	DATA to Switch Status Delay	t_D		50	100	ns	R_L=1kΩ, C_L=50 pF ①
12	RESET to Switch Status Delay	t_R		35	100	ns	R_L=1kΩ, C_L=50 pF ①

† Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
Digital Input rise time (tr) and fall time (tf) = 5ns.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
① Refer to Appendix, Fig. A.7 for test circuit.

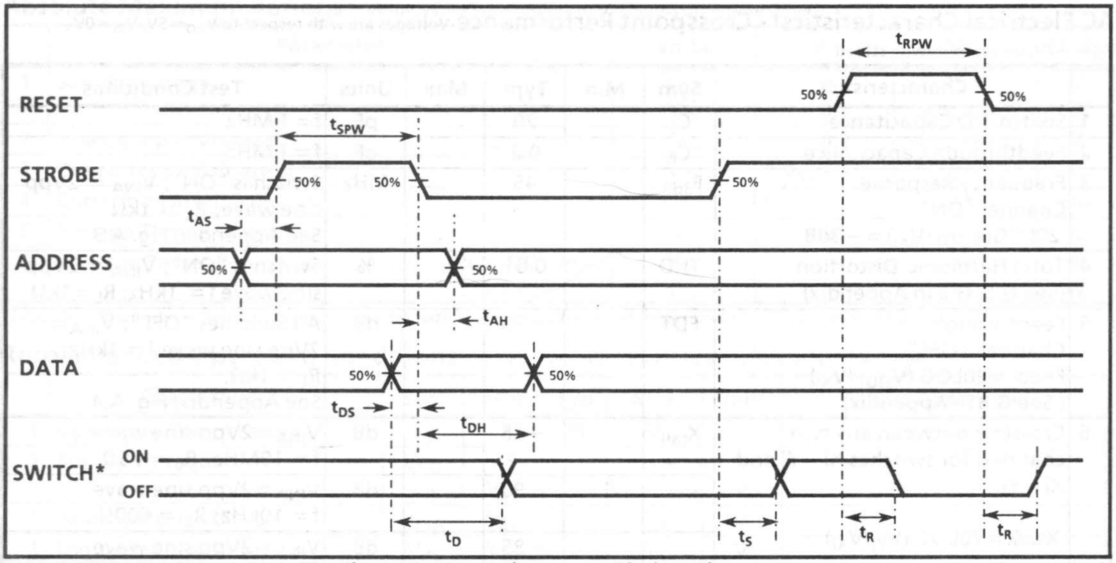


Figure 2 - Control Memory Timing Diagram

*See Appendix, Fig. A.7 for switching waveform

AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection
0	0	0	0	0	0	0	X0-Y0
1	0	0	0	0	0	0	X1-Y0
0	1	0	0	0	0	0	X2-Y0
1	1	0	0	0	0	0	X3-Y0
0	0	1	0	0	0	0	X4-Y0
1	0	1	0	0	0	0	X5-Y0
0	1	1	0	0	0	0	No Connection①
1	1	1	0	0	0	0	No Connection①
0	0	0	1	0	0	0	X6-Y0
1	0	0	1	0	0	0	X7-Y0
0	1	0	1	0	0	0	X8-Y0
1	1	0	1	0	0	0	X9-Y0
0	0	1	1	0	0	0	X10-Y0
1	0	1	1	0	0	0	X11-Y0
0	1	1	1	0	0	0	No Connection①
1	1	1	1	0	0	0	No Connection①
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	0 ↓ 0	X0-Y1 ↓ ↓ X11-Y1
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	0 ↓ 0	X0-Y2 ↓ ↓ X11-Y2
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	0 ↓ 0	X0-Y3 ↓ ↓ X11-Y3
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	0 ↓ 0	1 ↓ 1	X0-Y4 ↓ ↓ X11-Y4
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	0 ↓ 0	1 ↓ 1	X0-Y5 ↓ ↓ X11-Y5
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	0 ↓ 0	1 ↓ 1	1 ↓ 1	X0-Y6 ↓ ↓ X11-Y6
0 ↓ 1	0 ↓ 0	0 ↓ 1	0 ↓ 1	1 ↓ 1	1 ↓ 1	1 ↓ 1	X0-Y7 ↓ ↓ X11-Y7

Table 1 - Address Decode Truth Table

① This address has no effect on device status.

Pin Description

Pin #*	Name	Description
1	Y3	**Y3 Analog (Input/Output):** this is connected to the Y3 column of the switch array.
2	AY2	**Y2 Address Line (Input).**
3	RESET	**Master RESET (Input):** this is used to turn off all switches. Active High.
4,5	AX3,AX0	**X3 and X0 Address Lines (Inputs):** these are used to select X3 and X0 rows of switches.
6,7	NC	**No Connection.**
8-13	X6-X11	**X6-X11 Analog (Inputs/Outputs):** these are connected to the X6-X11 rows of the switch array.
14	NC	**No Connection**
15	Y7	**Y7 Analog (Input/Output):** this is connected to the Y7 column of the switch array.
16	VSS	**Digital Ground Reference (Input).**
17	Y6	**Y6 Analog (Input/Output):** this is connected to the Y6 column of the switch array.
18	STROBE	**STROBE (Input):** enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High.
19	Y5	**Y5 Analog (Input/Output):** this is connected to the Y5 column of the switch array.
20	VEE	**Negative Power Supply.**
21	Y4	**Y4 Analog (Input/Output):** this is connected to the Y4 column of the switch array.
22, 23	AX1,AX2	**X1 and X2 Address Lines (Inputs).**
24, 25	AY0,AY1	**Y0 and Y1 Address Lines (Inputs).**
26, 27	NC	**No Connection.**
28 - 33	X5-X0	**X5-X0 Analog (Inputs/Outputs):** these are connected to the X5-X0 rows of the switch array.
34	NC	**No Connection.**
35	Y0	**Y0 Analog (Input/Output):** this is connected to the Y0 column of the switch array.
36	VDD	**Positive Power Supply.**
37	Y1	**Y1 Analog (Input/Output):** this is connected to the Y1 column of the switch array.
38	DATA	**DATA (Input):** a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
39	Y2	**Y2 Analog (Input/Output):** this is connected to the Y2 column of the switch array.
40	NC	**No Connection.**

* Plastic DIP and CERDIP only.

Functional Description

The MT8815 is an analog switch matrix with an array size of 8×12. The switch array is arranged such that there are 8 columns by 12 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 96 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX3). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever the STROBE input is high and is latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input will asynchronously return all memory locations to logical "0" turning off all crosspoint switches. Two voltage reference pins (V_{SS} and V_{EE}) are provided for the MT8815 to enable switching of negative analog signals. The range for digital signals is from V_{DD} to V_{SS} while the range for analog signals is from V_{DD} to V_{EE}. V_{SS} and V_{EE} pins can be tied together if a single voltage reference is needed.

Address Decode

The seven address inputs along with the STROBE are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low while the address and data are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

MITEL®

ISO-CMOS MT8816
8 x 16 Analog Switch Array

9161-002-101-NA ISSUE 2 November 1988

Features

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage: 4.5V to 13.2V
- 12Vpp analog signal capability
- R_{ON} 65Ω max. @ V_{DD}=12V, 25°C
- $\Delta R_{ON} \leq 10\Omega$ @ V_{DD}=12V, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Separate analog and digital reference supplies
- Low power consumption ISO-CMOS technology

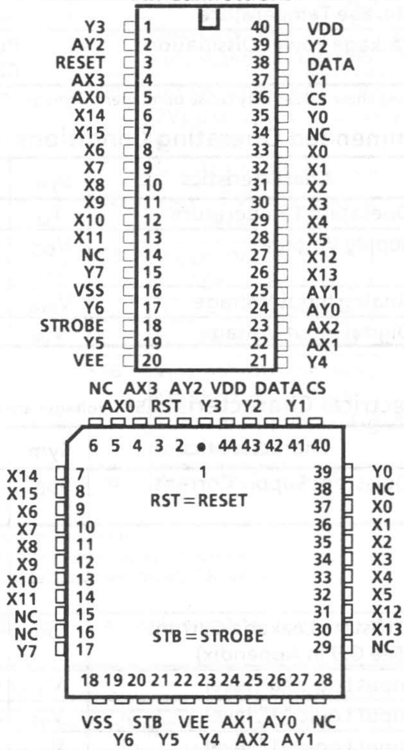
Applications

- Key systems
- PBX systems
- Mobile radio
- Test equipment /instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Description

The Mitel MT8816 is fabricated in MITEL's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8×16 array of crosspoint switches along with a 7 to 128 line decoder and latch circuits. Any one of the 128 switches can be addressed by selecting the appropriate seven address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. V_{SS} is the ground reference of the digital inputs. The range of the analog signal is from V_{DD} to V_{EE}. Chip Select (CS) allows the crosspoint array to be cascaded for matrix expansion.

Pin Connections



Ordering Information -40° to 85°C

MT8816AC	40 Pin CERDIP
MT8816AE	40 Pin PLASTIC DIP
MT8816AP	44 Pin PLCC

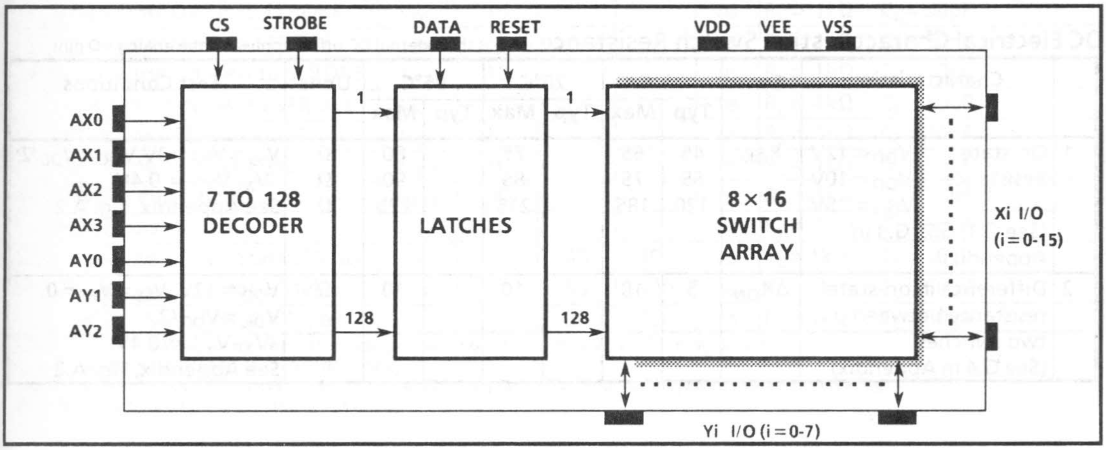


Figure 1- Functional Block Diagram

Absolute Maximum Ratings* - Voltages are with respect to V_{EE} unless otherwise stated.

	Parameter		Symbol	Min	Max	Units
1	Supply Voltage		V_{DD} V_{SS}	−0.3 −0.3	15.0 $V_{DD}+0.3$	V V
2	Analog Input Voltage		V_{INA}	−0.3	$V_{DD}+0.3$	V
3	Digital Input Voltage		V_{IN}	$V_{SS}-0.3$	$V_{DD}+0.3$	V
4	Current on any I/O Pin		I		±15	mA
5	Storage Temperature		T_S	−65	+150	°C
6	Package Power Dissipation	PLASTIC DIP CERDIP	P_D P_D		0.6 1.0	W W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{EE} unless otherwise stated.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Operating Temperature	T_O	−40	25	85	°C	
2	Supply Voltage	V_{DD} V_{SS}	4.5 V_{EE}		13.2 $V_{DD}-4.5$	V V	
3	Analog Input Voltage	V_{INA}	V_{EE}		V_{DD}	V	
4	Digital Input Voltage	V_{IN}	V_{SS}		V_{DD}	V	

DC Electrical Characteristics† - Voltages are with respect to $V_{EE}=V_{SS}=0V$, $V_{DD}=12V$ unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Quiescent Supply Current	I_{DD}		1	100	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}
				0.4	1.5	mA	All digital inputs at $V_{IN}=2.4+V_{SS}$; $V_{SS}=7.0V$
				5	15	mA	All digital inputs at $V_{IN}=3.4V$
2	Off-state Leakage Current (See G.9 in Appendix)	I_{OFF}		±1	±500	nA	$\lvert V_{Xi}-V_{Yj}\rvert = V_{DD}-V_{EE}$ See Appendix, Fig. A.1
3	Input Logic "0" level	V_{IL}			$0.8+V_{SS}$	V	$V_{SS}=7.5V$; $V_{EE}=0V$
4	Input Logic "1" level	V_{IH}	$2.0+V_{SS}$			V	$V_{SS}=6.5V$; $V_{EE}=0V$
5	Input Logic "1" level	V_{IH}	3.3			V	
6	Input Leakage (digital pins)	I_{LEAK}		0.1	10	μA	All digital inputs at $V_{IN}=V_{SS}$ or V_{DD}

† DC Electrical Characteristics are over recommended temperature range.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics- Switch Resistance - V_{DC} is the external DC offset applied at the analog I/O pins.

	Characteristics		Sym	25°C		70°C		85°C		Units	Test Conditions
				Typ	Max	Typ	Max	Typ	Max		
1	On-state Resistance (See G.1, G.2, G.3 in Appendix)	$V_{DD}=12V$ $V_{DD}=10V$ $V_{DD}=5V$	R_{ON}	45 55 120	65 75 185		75 85 215		80 90 225	Ω Ω Ω	$V_{SS}=V_{EE}=0V$, $V_{DC}=V_{DD}/2$, $\lvert V_{Xi}-V_{Yj}\rvert = 0.4V$ See Appendix, Fig. A.2
2	Difference in on-state resistance between two switches (See G.4 in Appendix)		ΔR_{ON}	5	10		10		10	Ω	$V_{DD}=12V$, $V_{SS}=V_{EE}=0$, $V_{DC}=V_{DD}/2$, $\lvert V_{Xi}-V_{Yj}\rvert = 0.4V$ See Appendix, Fig. A.2

AC Electrical Characteristics† - Crosspoint Performance

-Voltages are with respect to $V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-7V$, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Switch I/O Capacitance	C_S		20		pF	f=1 MHz
2	Feedthrough Capacitance	C_F		0.2		pF	f=1 MHz
3	Frequency Response Channel "ON" $20LOG(V_{OUT}/V_{Xi})=-3dB$	F_{3dB}		45		MHz	Switch is "ON"; $V_{INA}=2Vpp$ sine wave; $R_L=1k\Omega$ See Appendix, Fig. A.3
4	Total Harmonic Distortion (See G.5, G.6 in Appendix)	THD		0.01		%	Switch is "ON"; $V_{INA}=2Vpp$ sine wave f= 1kHz; $R_L=1k\Omega$
5	Feedthrough Channel "OFF" Feed.= $20LOG(V_{OUT}/V_{Xi})$ (See G.8 in Appendix)	FDT		−95		dB	All Switches "OFF"; $V_{INA}=$ 2Vpp sine wave f= 1kHz; $R_L=1k\Omega$. See Appendix, Fig. A.4
6	Crosstalk between any two channels for switches Xi−Yi and Xj−Yj. Xtalk= $20LOG(V_{Yj}/V_{Xi})$. (See G.7 in Appendix).	X_{talk}		−45		dB	$V_{INA}=2Vpp$ sine wave f= 10MHz; $R_L=75\Omega$.
				−90		dB	$V_{INA}=2Vpp$ sine wave f= 10kHz; $R_L=600\Omega$.
				−85		dB	$V_{INA}=2Vpp$ sine wave f= 10kHz; $R_L=1k\Omega$.
				−80		dB	$V_{INA}=2Vpp$ sine wave f= 1kHz; $R_L=10k\Omega$. Refer to Appendix, Fig. A.5 for test circuit.
7	Propagation delay through switch	t_{PS}			30	ns	$R_L=1k\Omega$; $C_L=50pF$

† Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5dB better.

AC Electrical Characteristics† - Control and I/O Timings

- Voltages are with respect to $V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-7V$, unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Control Input crosstalk to switch (for CS, DATA, STROBE, Address)	CX_{talk}		30		mVpp	$V_{IN}=3V$ squarewave; $R_{IN}=1k\Omega$, $R_L=10k\Omega$. See Appendix, Fig. A.6
2	Digital Input Capacitance	C_{DI}		10		pF	f=1MHz
3	Switching Frequency	F_O			20	MHz	
4	Setup Time DATA to STROBE	t_{DS}	10			ns	$R_L=1k\Omega$, $C_L=50pF$ ⑤
5	Hold Time DATA to STROBE	t_{DH}	10			ns	$R_L=1k\Omega$, $C_L=50pF$ ⑤
6	Setup Time Address to STROBE	t_{AS}	10			ns	$R_L=1k\Omega$, $C_L=50pF$ ⑤
7	Hold Time Address to STROBE	t_{AH}	10			ns	$R_L=1k\Omega$, $C_L=50pF$ ⑤
8	Setup Time CS to STROBE	t_{CSS}	10			ns	$R_L=1k\Omega$, $C_L=50pF$ ⑤
9	Hold Time CS to STROBE	t_{CSH}	10			ns	$R_L=1k\Omega$, $C_L=50pF$ ⑤
10	STROBE Pulse Width	t_{SPW}	20			ns	$R_L=1k\Omega$, $C_L=50pF$ ⑤
11	RESET Pulse Width	t_{RPW}	40			ns	$R_L=1k\Omega$, $C_L=50pF$ ⑤
12	STROBE to Switch Status Delay	t_S		40	100	ns	$R_L=1k\Omega$, $C_L=50pF$ ⑤
13	DATA to Switch Status Delay	t_D		50	100	ns	$R_L=1k\Omega$, $C_L=50pF$ ⑤
14	RESET to Switch Status Delay	t_R		35	100	ns	$R_L=1k\Omega$, $C_L=50pF$ ⑤

† Timing is over recommended temperature range. See Fig. 2 for control and I/O timing details.
Digital Input rise time (tr) and fall time (tf) = 5ns.
‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.
⑤ Refer to Appendix, Fig. A.7 for test circuit.

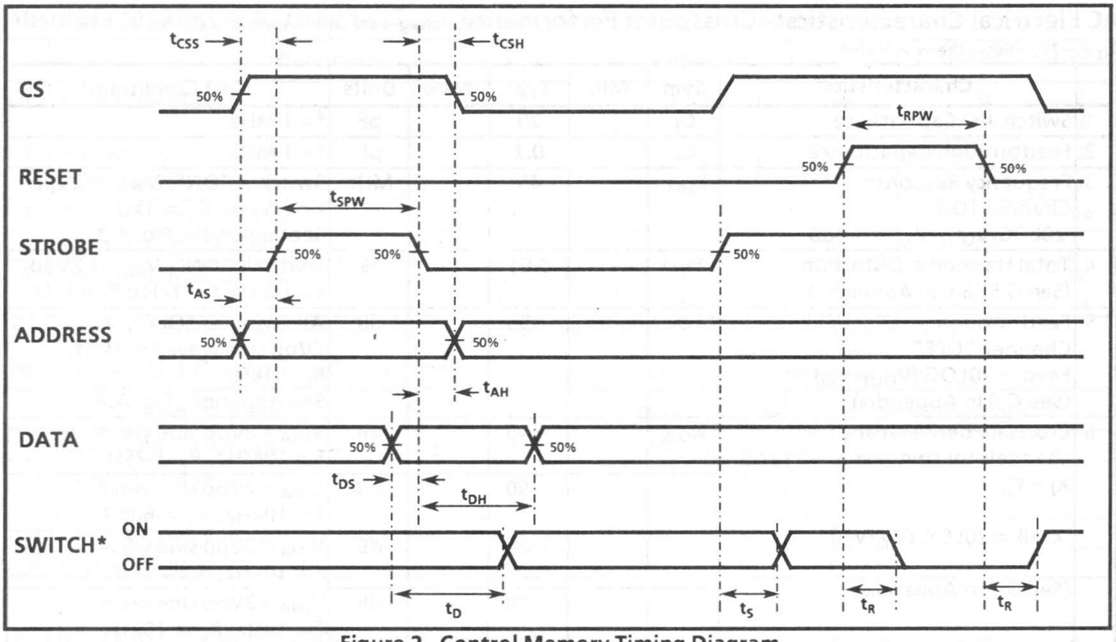


Figure 2 - Control Memory Timing Diagram

*See Appendix, Fig. A.7 for switching waveform

AX0	AX1	AX2	AX3	AY0	AY1	AY2	Connection*
0	0	0	0	0	0	0	X0 - Y0
1	0	0	0	0	0	0	X1 - Y0
0	1	0	0	0	0	0	X2 - Y0
1	1	0	0	0	0	0	X3 - Y0
0	0	1	0	0	0	0	X4 - Y0
1	0	1	0	0	0	0	X5 - Y0
0	1	1	0	0	0	0	X12 - Y0
1	1	1	0	0	0	0	X13 - Y0
0	0	0	1	0	0	0	X6 - Y0
1	0	0	1	0	0	0	X7 - Y0
0	1	0	1	0	0	0	X8 - Y0
1	1	0	1	0	0	0	X9 - Y0
0	0	1	1	0	0	0	X10 - Y0
1	0	1	1	0	0	0	X11 - Y0
0	1	1	1	0	0	0	X14 - Y0
1	1	1	1	0	0	0	X15 - Y0
0	0	0	0	1	0	0	X0 - Y1
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	0	0	X15 - Y1
0	0	0	0	0	1	0	X0 - Y2
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	0	1	0	X15 - Y2
0	0	0	0	1	1	0	X0 - Y3
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	1	0	X15 - Y3
0	0	0	0	0	0	1	X0 - Y4
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	0	0	1	X15 - Y4
0	0	0	0	1	0	1	X0 - Y5
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	0	1	X15 - Y5
0	0	0	0	0	1	1	X0 - Y6
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	0	1	1	X15 - Y6
0	0	0	0	1	1	1	X0 - Y7
↓	↓	↓	↓	↓	↓	↓	↓ ↓
1	1	1	1	1	1	1	X15 - Y7

Figure 3 - Address Decode Truth Table

*Switch connections are not in ascending order

Pin Description

Pin #*	Name	Description
1	Y3	**Y3 Analog (Input/Output):** this is connected to the Y3 column of the switch array.
2	AY2	**Y2 Address Line (Input).**
3	RESET	**Master RESET (Input):** this is used to turn off all switches regardless of the condition of CS. Active High.
4,5	AX3,AX0	**X3 and X0 Address Lines (Inputs).**
6,7	X14, X15	**X14 and X15 Analog (Inputs/Outputs):** these are connected to the X14 and X15 rows of the switch array.
8-13	X6-X11	**X6-X11 Analog (Inputs/Outputs):** these are connected to the X6-X11 rows of the switch array.
14	NC	**No Connection**
15	Y7	**Y7 Analog (Input/Output):** this is connected to the Y7 column of the switch array.
16	VSS	**Digital Ground Reference .**
17	Y6	**Y6 Analog (Input/Output):** this is connected to the Y6 column of the switch array.
18	STROBE	**STROBE (Input):** enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High.
19	Y5	**Y5 Analog (Input/Output):** this is connected to the Y5 column of the switch array.
20	VEE	**Negative Power Supply.**
21	Y4	**Y4 Analog (Input/Output):** this is connected to the Y4 column of the switch array.
22, 23	AX1,AX2	**X1 and X2 Address Lines (Inputs).**
24, 25	AY0,AY1	**Y0 and Y1 Address Lines (Inputs).**
26, 27	X13, X12	**X13 and X12 Analog (Inputs/Outputs):** these are connected to the X13 and X12 rows of the switch array.
28 - 33	X5-X0	**X5-X0 Analog (Inputs/Outputs):** these are connected to the X5-X0 rows of the switch array.
34	NC	**No Connection.**
35	Y0	**Y0 Analog (Input/Output):** this is connected to the Y0 column of the switch array.
36	CS	**Chip Select (Input):** this is used to select the device. Active High.
37	Y1	**Y1 Analog (Input/Output):** this is connected to the Y1 column of the switch array.
38	DATA	**DATA (Input):** a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High.
39	Y2	**Y2 Analog (Input/Output):** this is connected to the Y2 column of the switch array.
40	VDD	**Positive Power Supply.**

* Plastic DIP and CERDIP only

Functional Description

The MT8816 is an analog switch matrix with an array size of 8×16. The switch array is arranged such that there are 8 columns by 16 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 128 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX3). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever both the CS (Chip Select) and STROBE inputs are high and are latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input will asynchronously return all memory locations to logical "0" turning off all crosspoint switches regardless of whether CS is high or low. Two voltage reference pins (V_{SS} and V_{EE}) are provided for the MT8816 to enable switching of negative analog signals. The range for digital signals is from V_{DD} to V_{SS} while the range for analog signals is from V_{DD} to V_{EE}. V_{SS} and V_{EE} pins can be tied together if a single voltage reference is needed.

Address Decode

The seven address inputs along with the STROBE and CS (Chip Select) are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low and CS must go high while the address and data are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

MT8806/08/09/12/14/15/16 ANALOG SWITCH ARRAY FAMILY:

TEST CIRCUITS FOR KEY PARAMETER MEASUREMENTS

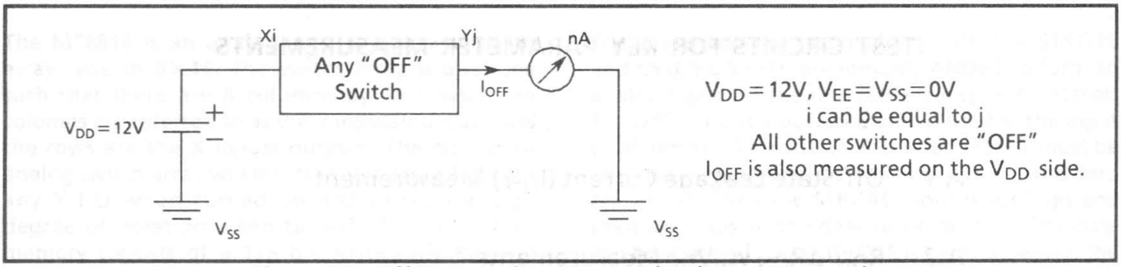


Figure A.1 - Off-State Leakage Current (I_{OFF}) Measurement *

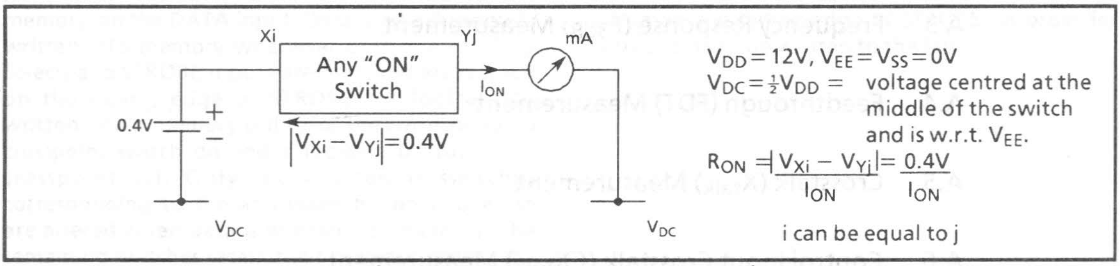


Figure A.2 - $R_{ON}/\Delta R_{ON}$ Measurement *

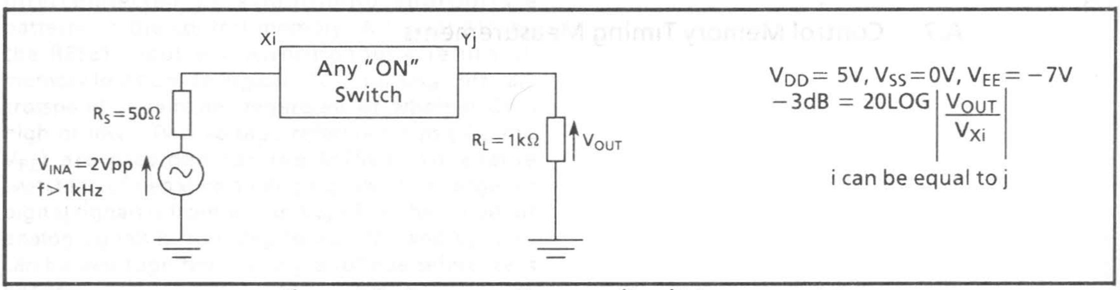


Figure A.3 - Frequency Response (F_{3dB}) Measurement †

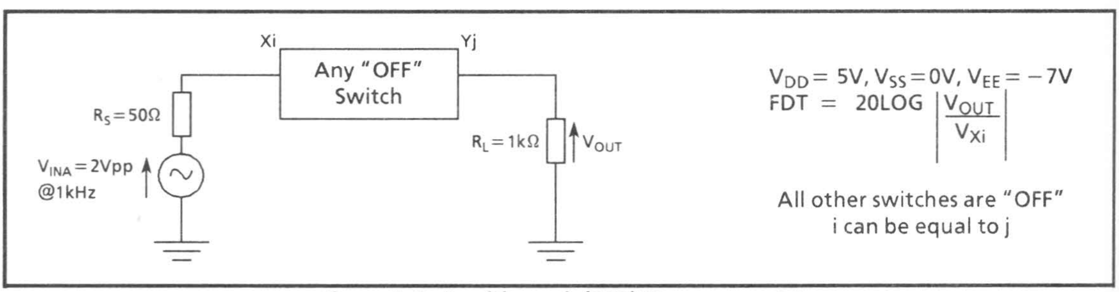


Figure A.4 - Feedthrough (FDT) Measurement †

Notes:

* Test Conditions for MT8809 and MT8812 are respectively: $V_{DD} = 12V$, $V_{SS} = 0V$ and $V_{DD} = 14V$, $V_{SS} = 0V$.

† Test Conditions for MT8809 and MT8812 are respectively: $V_{DD} = 5V$, $V_{DC} = 0V$, $V_{SS} = -7V$ and $V_{DD} = 7V$, $V_{DC} = 0V$, $V_{SS} = -7V$.

All Xi and Yj analog I/O pins can be interchanged for all measurements.

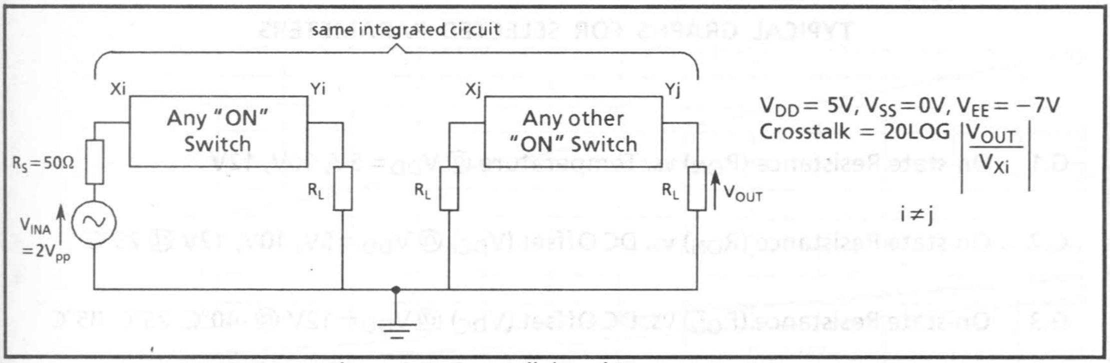


Figure A.5 - Crosstalk (X_{talk}) Measurement †

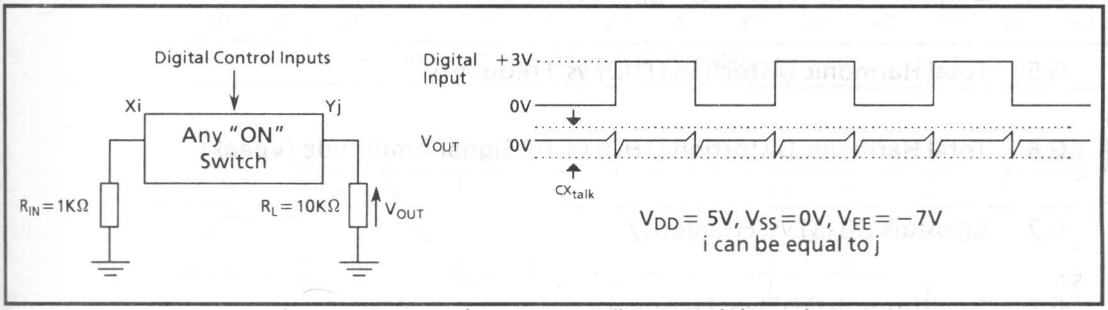
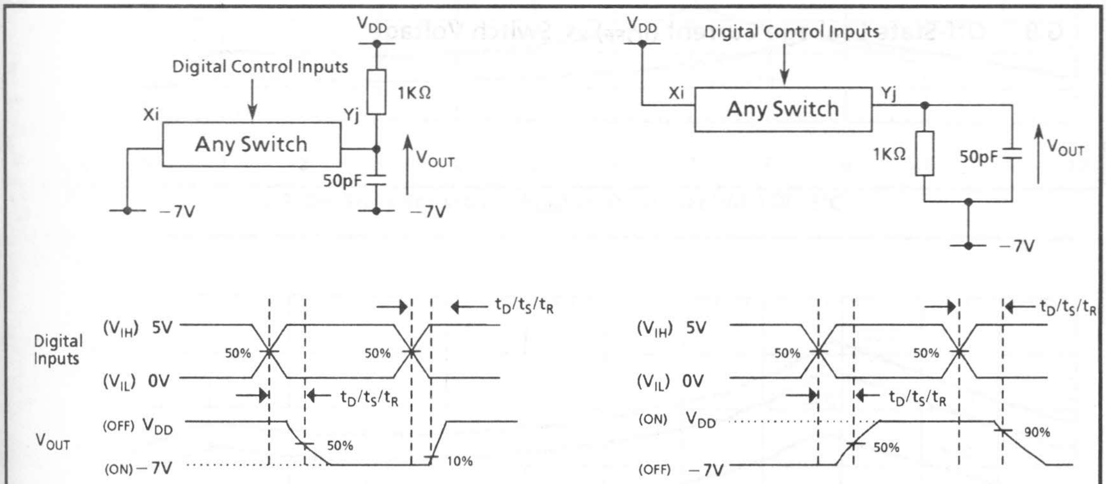


Figure A.6 - Control Input Crosstalk to Switch (CX_{talk}) †



a) R_L at V_{DD} **b) R_L at −7V**

$V_{DD} = 5V, V_{SS} = 0V, V_{EE} = -7V$
i can be equal to j
MT8809: $V_{IH} = 5V, V_{IL} = -7V$
MT8812: $V_{IH} = 7V, V_{IL} = -7V$

Figure A.7 - Control Memory Timing Measurements†

Notes:

†Test Conditions for MT8809 and MT8812 are respectively: $V_{DD} = 5V, V_{DC} = 0V, V_{SS} = -7V$ and $V_{DD} = 7V, V_{DC} = 0V, V_{SS} = -7V$.
All Xi and Yj analog I/O pins can be interchanged for all measurements.

MT8806/08/09/12/14/15/16 ANALOG SWITCH ARRAY FAMILY:

TYPICAL GRAPHS FOR SELECTED PARAMETERS

G.1 On-state Resistance (R_{ON}) vs. Temperature @ V_{DD}=5V, 10V, 12V

G.2 On-state Resistance (R_{ON}) vs. DC Offset (V_{DC}) @ V_{DD}=5V, 10V, 12V @ 25°C

G.3 On-state Resistance (R_{ON}) vs. DC Offset (V_{DC}) @ V_{DD}=12V @ -40°C, 25°C, 85°C

G.4 ΔR_{ON} vs. Temperature @ V_{DD}=5V, 10V, 12V

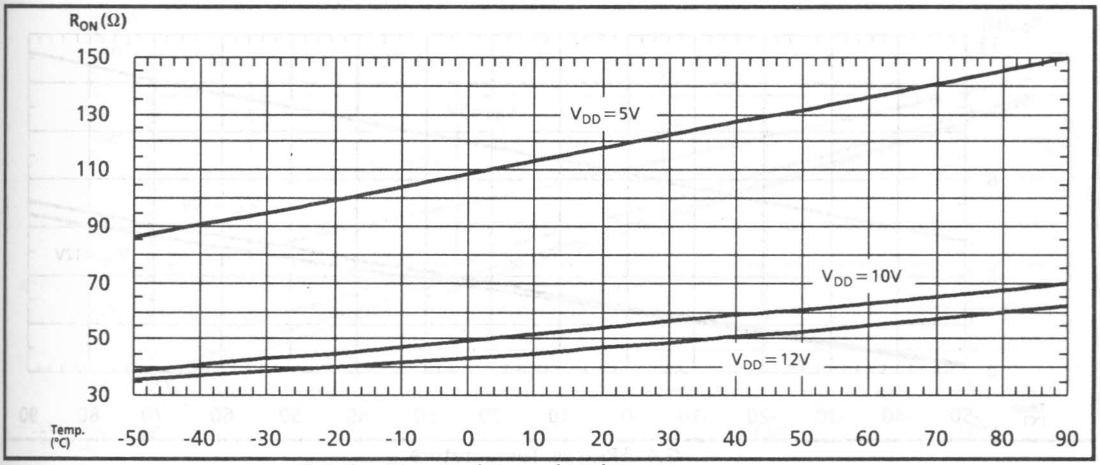
G.5 Total Harmonic Distortion (THD) vs. Frequency

G.6 Total Harmonic Distortion (THD) vs. I/P Signal Amplitude (Vpeak)

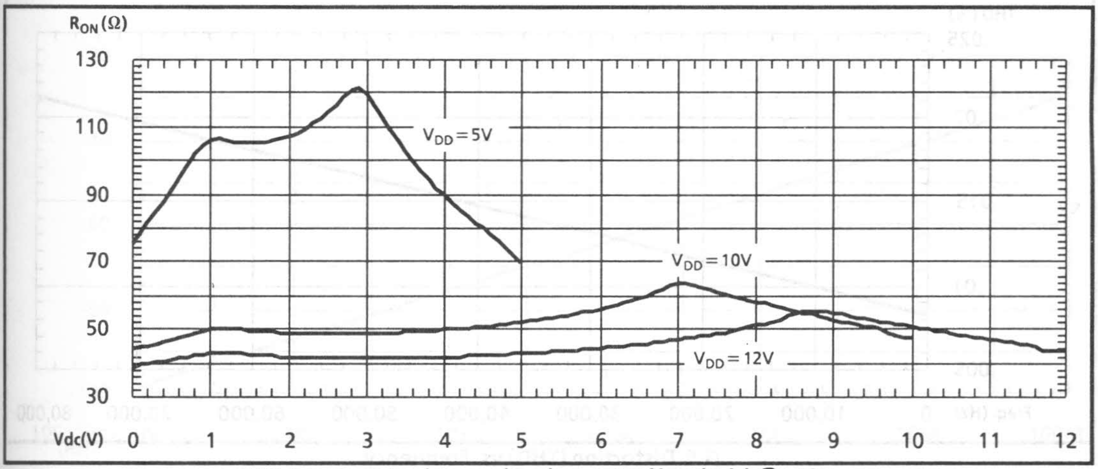
G.7 Crosstalk (X_{talk}) vs. Frequency

G.8 Feedthrough (FDT) vs. Frequency

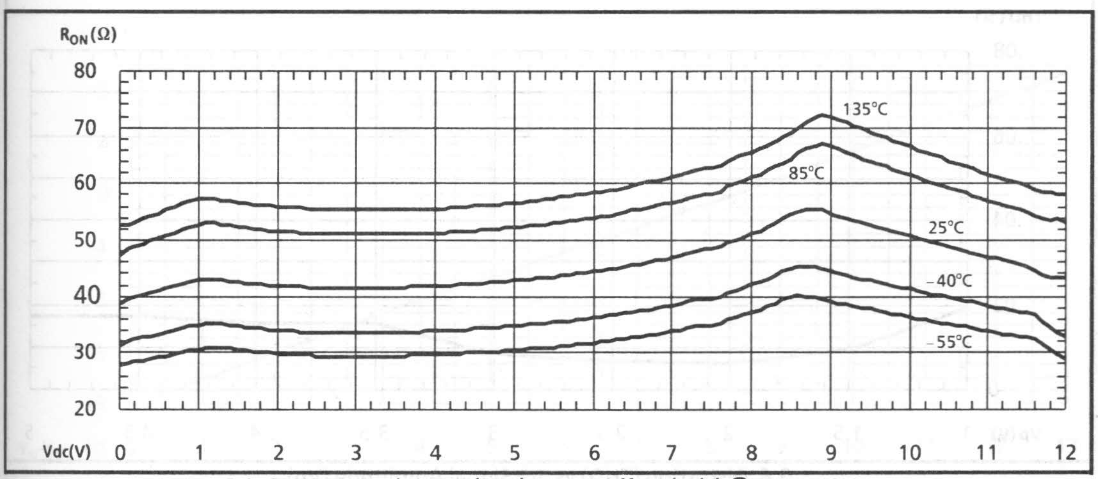
G.9 Off-State Leakage Current (I_{OFF}) vs. Switch Voltage



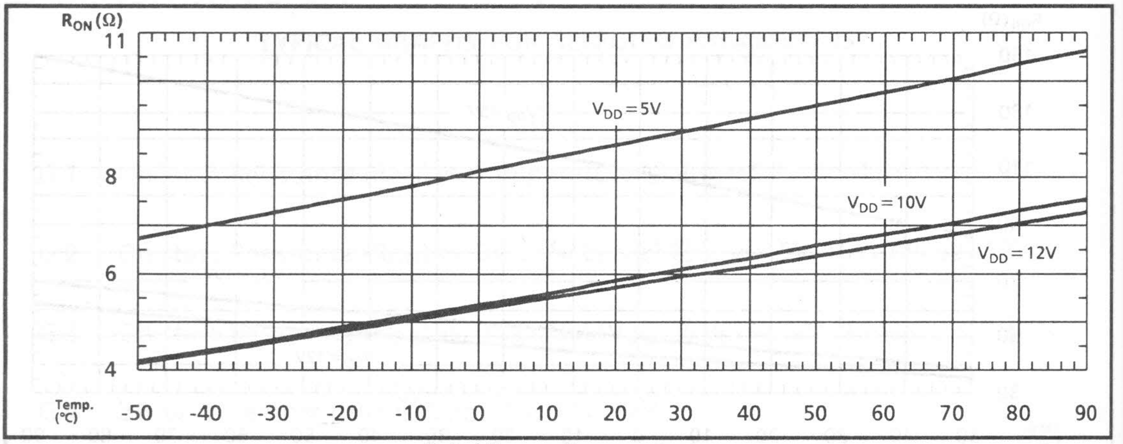
G.1 On-State Resistance (R_{ON}) vs. Temperature



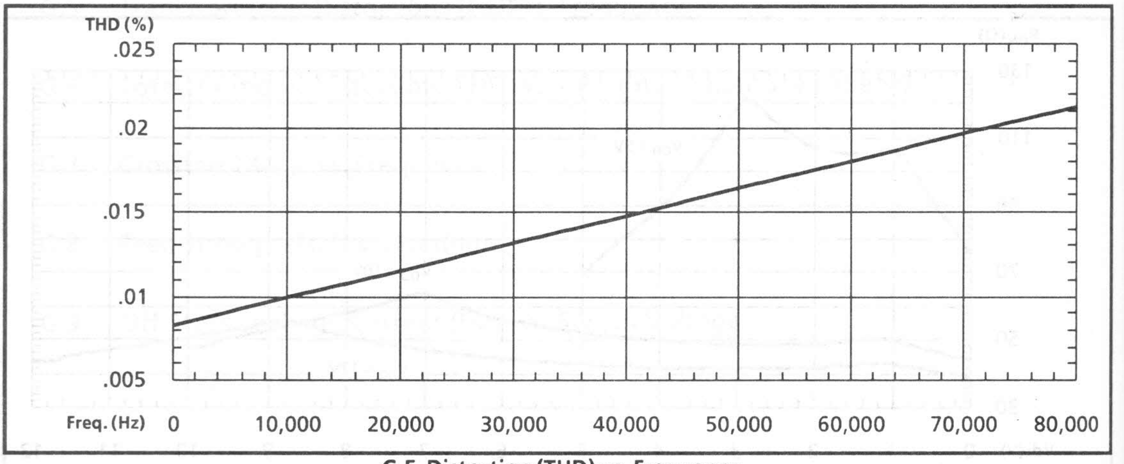
G.2 On-State Resistance (R_{ON}) vs. DC Offset (Vdc) @ 25°C



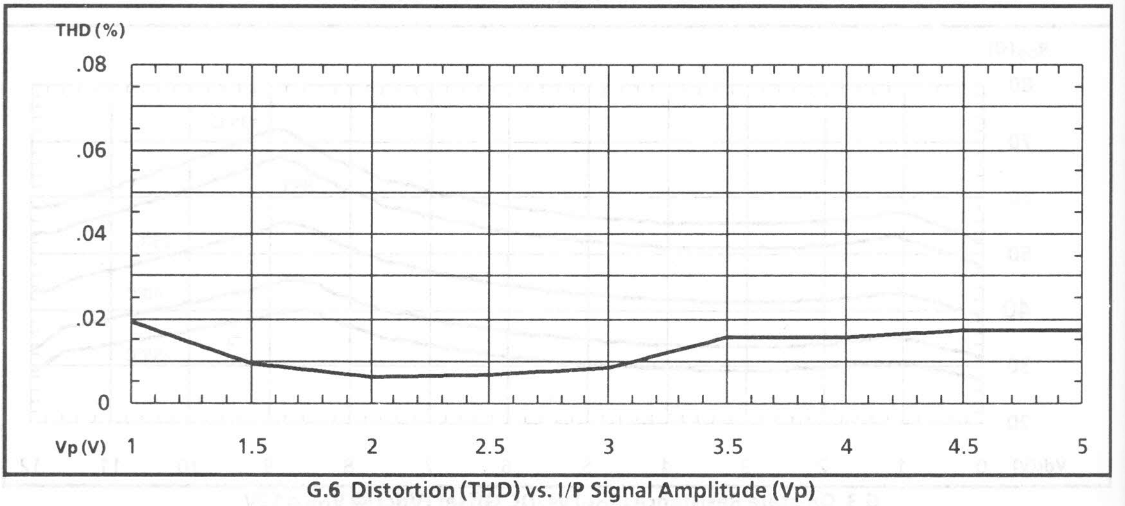
G.3 On-state Resistance (R_{ON}) vs. DC Offset (Vdc) @ V_{DD} = 12V



G.4 ΔR_{ON} vs. Temperature

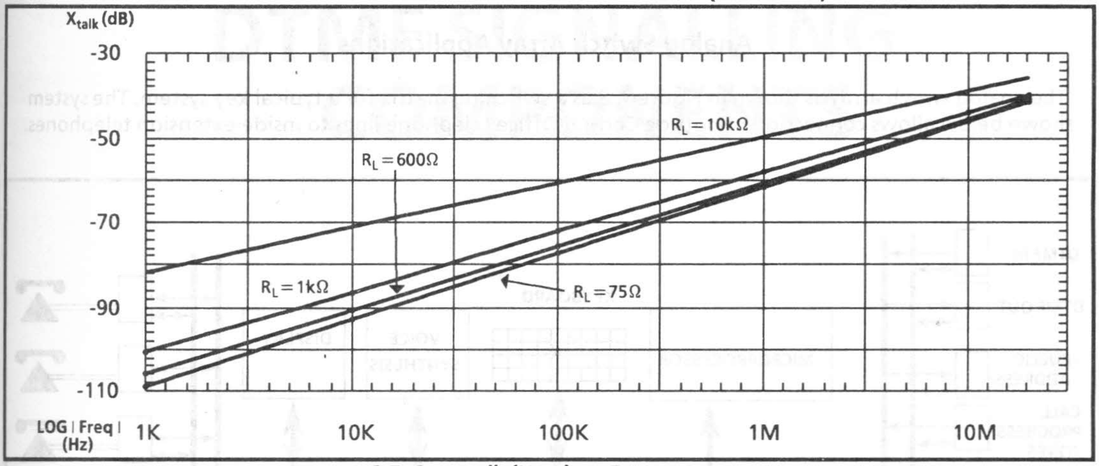


G.5 Distortion (THD) vs. Frequency

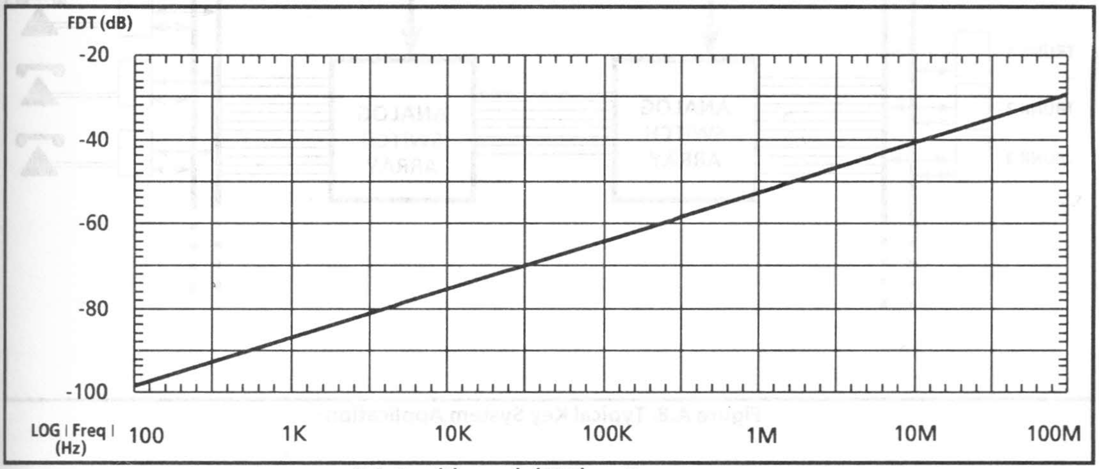


G.6 Distortion (THD) vs. I/P Signal Amplitude (Vp)

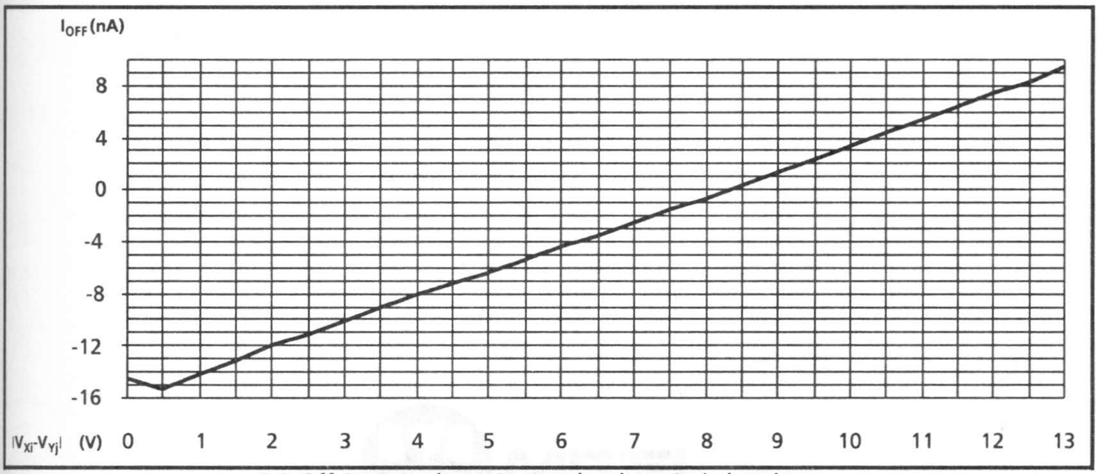
ANALOG SWITCH ARRAY MEASUREMENTS (continued)



G.7 Crosstalk (X_{talk}) vs. Frequency



G.8 Feedthrough (FDT) vs. Frequency



G.9 Off-State Leakage Current (I_{OFF}) vs. Switch Voltage

MT8806/08/09/12/14/15/16 ANALOG SWITCH ARRAY FAMILY:

Analog Switch Array Applications

The analog switch array is shown in Figure A.8 as a switching matrix for a typical key system. The system shown below allows connection of outside Central Office telephone lines to inside extension telephones.

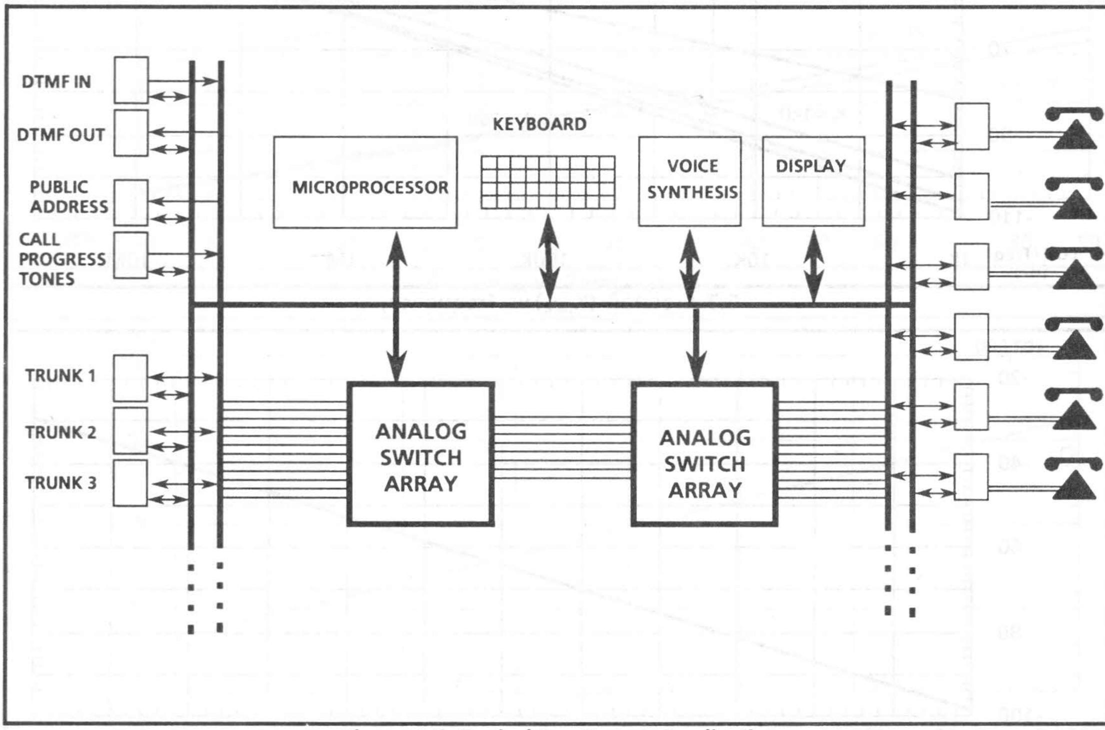


Figure A.8. Typical Key System Application

DTMF SIGNALLING COMPONENTS

3

MITEL®

MITEL®

DTMF Receiver Test Cassette

ISSUE 3 September 1989

Features

- Provides complete receiver evaluation in less than 60 minutes testing time.
- Utilizes a condensed speech recording equivalent to many hours of receiver exposure to evaluate talk-off rate.
- Checks receiver recognition bandwidths, center frequencies, maximum acceptable amplitude ratio, guard time, dynamic range, and acceptable signal to noise ratio.
- Test equipment requirement consists of a digital counter, an ac voltmeter, and a low cost cassette tape player. The tape player may require a small amplifier to achieve 2 V_{RMS} depending upon the receiver to be tested.
- Compensation factors allow tape player speed inaccuracies of up to 2% without loss of measurement accuracy.
- Convenient C60 cassette format on low noise high bias chrome tape, recorded using Dolby B noise reduction.

General Description

The Mitel CM7291 Tone Receiver Test Cassette cuts the total evaluation time of DTMF tone receivers to less than 60 minutes. Test equipment requirements are also minimized to a modest test setup.

Test Content

Side one of the tape contains a series of tests involving recorded tone bursts with the parameters varied in a number of ways. Tests are performed by sending the tone bursts to the receiver, and counting the number of bursts to which the receiver responds. The results from these tests provide direct indications of receiver performance.

Side two of the tape contains a condensed speech recording which is used to evaluate the speech immunity of the receiver. Ideally a receiver's response to the speech recording should be zero, since no intentional tone bursts are present. In practice the number of responses will vary from 2 to 100, depending on the receiver quality and dynamic range.

Prompts and instructions are included on both sides of the tape to aid in receiver testing.

Test Setup

Two test setups using the same test equipment are used. The first, shown in Fig. 1, is used to perform a 1 kHz calibration test. The second, shown in Fig. 2, is used for the receiver dynamic tests.

Calibration Test: The first test on both sides of the tape is a 1 kHz calibration test, and is used to provide a correction factor for the playback inaccuracy of the tape player.

Receiver Test: Once the calibration test has been performed the test setup is changed to that shown in Fig. 2, and remains the same that way for all other tests.

Receiver Testing

The following describes the recorded contents of both sides of the tape, and the tests provided.

The 1 kHz reference signal level output from the cassette player which is adjusted to 2.0 V_{RMS} (5.656 Vp-p) is required for tone receiver systems capable of handling this level (i.e. this level won't cause internal clipping of the signal). All levels referred to in this document are referenced to the initial 2.0 V_{RMS} level setting.

Note: To use the CM7291 with tone receivers operating from a single 5 V_{DC} supply, the 1 kHz reference signal output level of the cassette player must be reduced. For example, if using the MT8870 tone receiver, the 1 kHz reference signal level would be adjusted such that the signal observed at the devices GS pin would be a maximum without clipping. This level would be 1.738 V_{RMS} (i.e. 4.91 Vp-p). Accordingly, the levels referred to in the test descriptions must be reduced proportionally. For example, each dual tone frequency at a 1.0 V_{RMS} level would now be 869 mV_{RMS} (+1 dBm) and 35 dB down from this level would be 20 mV_{RMS} (-34 dBm). A 200 mV_{RMS} level per frequency would now be 174 mV_{RMS} (-13 dBm).

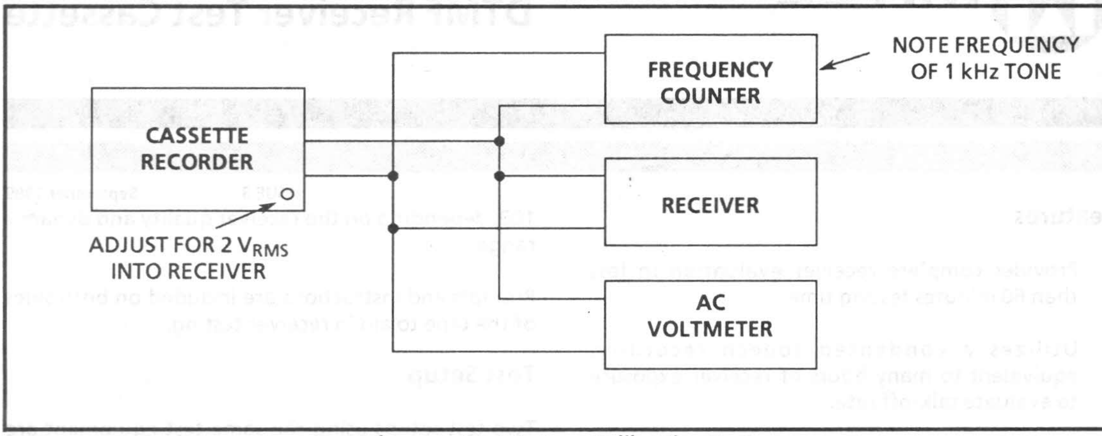


Figure 1 - Test Setup - Calibration Test

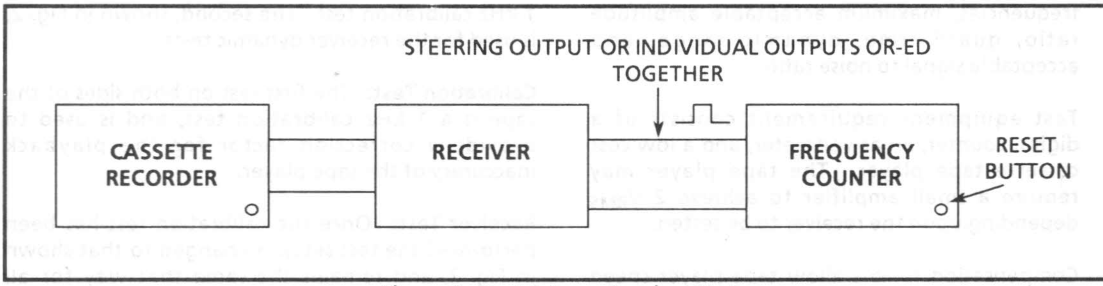


Figure 2 - Test Setup - Receiver Test

SIDE 1 - TEST 1

Calibration Tone: Consists of a continuous 1 kHz tone, present for one minute. Used to provide a correction factor for tape playback speed inaccuracy using equation 1. The correction is employed when checking receiver channel center frequencies in test 3.

$X(\%) = f_0 - 1000)/10$ .....Eqn 1

Frequency f_0 is measured as follows, using the test setup shown in Fig. 1.

- Set the level of tone at the receiver input to 2 V_{RMS}. This leveL setting must not be altered for the duration of the tests on side 1.
- Measure the frequency of the tone f_0 at the receiver input.

SIDE 1 - TEST 2

Decode Check: All tone pairs associated with standard 4 x 4 keypad digits (i.e. L1 H1 through L4 H4) are pulsed sequentially using 50 ms bursts at 1 V_{RMS} per frequency. Each tone pair is pulsed 10 times consecutively. The receiver should respond to all tone pairs it is designed to receive.

SIDE 1 - TEST 3

Recognition Bandwidth and Channel Center Frequency Check

This test utilizes the tone pairs L1 H1, L2 H2, L3 H3, and L4 H4 (i.e. digits 1, 5, 9 and 16). Each tone pair requires four tests to complete the check, making 16 sections overall. Each section contains 40 pulses of 50 ms duration, with an amplitude of 0.2 V_{RMS} per frequency.

Four sections covering the tests for one tone pair (1 digit) are:

(a) H frequency at 0% deviation from center, L frequency at +0.1%. L frequency is then incremented in +0.1% steps, up to +4%. The number of tone bursts is noted and designated N+.

(b) H frequency at 0% deviation, L frequency at -0.1%. L frequency is then incremented in -0.1% steps, up to -4%. The number of tone bursts is noted and designated N−.

(c) The test in (a) is repeated with the L frequency at 0% and the H frequency varied up to +4%.

(d) The test in (b) is repeated with the L frequency at 0% and the H frequency varied up to -4%.

Receiver Recognition Bandwidth (RRB) is calculated as follows:

$$RRB\% = (N^+ + N^-)/10 \qquad \text{.....Eqn 2}$$

Receiver Center Frequency Offset (RCFO) is calculated as follows:

$$RCFO\% = X + (N^+ - N^-)/20 \qquad \text{.....Eqn 3}$$

SIDE 1 - TEST 4

Acceptable Amplitude Ratio (Twist)

This test utilizes the tone paris L1 H1, L2 H2, L3 H3, and L4 H4 (i.e. digits 1, 5, 9 and 16). There are eight sections to the test. Each section contains 200 pulses with a 50 ms duration for each pulse. Initially the amplitude of both tones is 1 V_{RMS}.

Two sections to test one tone pair are:

(a) *Standard Twist*: H tone amplitude is maintained at 1 V_{RMS}, L tone amplitude is attenuated gradually until the amplitude ratio L/H is −20dB. Note the number of responses from the receiver.

(b) *Reverse Twist:* L tone amplitude is maintained at 1 V_{RMS}, H tone amplitude is attenuated gradually until the amplitude ratio is 20 dB. Note the number of responses from the receiver.

The Acceptable Amplitude Ratio in dB is equal to the number of responses registered in (a) or (b), divided by 10.

SIDE 1 - TEST 5

Dynamic Range

This test utilizes tone pair L1 H1 (digit 1). Thirty-five tone pair pulses are transmitted, with both frequencies starting at 1 V_{RMS}. The amplitude of each is gradually attenuated to −35 dB at a rate of 1 dB per pulse. The Dynamic Range in dB is equal to the number of responses from the receiver during the test.

SIDE 1 - TEST 6
Guard Time

This test utilizes tone pair L1 H1 (digit 1). Four hundred pulses are transmitted at an amplitude of 1 V_{RMS} per frequency. Pulse duration starts at 49 ms and is gradually reduced to 10ms. Guard time in ms is equal to (500 − number of responses) / 10.

SIDE 1 - TEST 7

Acceptable Signal to Noise Ratio

This test utilizes tone pair L1 H1, transmitted on a noise background. The test consists of three sections in which the tone pair is transmitted 1000 times at an amplitude of 1 V_{RMS} per frequency, but with a different white noise level for each section. The first level is −24 dBV, the second −18 dBV, and the third −12 dBV. The Acceptable Signal to Noise Ratio is the lowest ratio of signal to noise in the test where the receiver responds to all 1000 pulses.

SIDE 2 - TEST 1

Calibration Tone

A repetition of Test 1 - Side 1, at which time the signal level at the receiver input must be recalibrated to 2.0 V_{RMS}. This adjustment is entirely independent of the setting made at Test 1 - Side 1.

SIDE 2 - TEST 2

Talk-Off Test

The test consists of recordings of conversations on telephone trunks make over a long period of time and condensed into a 30 minute period. Receiver immunity to talk-off is determined by the number of responses occurring during this test. A receiver with an acceptable talk-off response should register less than 30.

Summary of Cassette Content

The following table lists the contents of the cassette together with the playing time from the start of the tape. It is recommended that the tape counter reading for each test be recorded in the column provided. This will provide the most convenient method of test location.

TEST	DESCRIPTION			COUNTER	TIME Minutes: Seconds
Introduction					0
Side 1, 1	1 kHz at 2 V_{RMS}				0:20
Side 1, 2	Decode test digits 1 to 16 (10 pulses each)				2:00
Side 1, 3	Recognition bandwidth and centre frequency check (40 pulses each)				3:10
Side 1, 3a	Digit 1	697Hz	+0.1 to +4%		4:10
Side 1, 3b	Digit 1	697Hz	−0.1 to −4%		
Side 1, 3c	Digit 1	1209Hz	+0.1 to +4%		

Pin Description

Pin #	Name	Description
1	DL	**Digital Loopback** (TTL Input) - A High level on this input causes the device to enter the Digital Loopback mode. In this mode, the received data from the remote end is internally looped back to TD and $\overline{\text{DSR}}$ is forced High to signal to the DTE that the modem is not ready for transmission. The received data is not available on $\overline{\text{RD}}$ pin during the DL mode.
2	TP	**Test Point** - Test pin must be connected to either V_{EE} or V_{DD} for normal operations.
3	EP	**Eye Pattern** - Output (analog) of the demodulator prior to slicing. Do not load.
4	V_{DD}	Positive power pin (+5 V).
5	RC	**Receive Carrier** - This analog input is the data carrier received by the Data Access Arrangement from the line. The modem demodulates this signal to generate the receive data bits.
6 7	TEST1 TEST0	These are test inputs and must be tied to V_{EE} for normal applications. See Table 3 under Passthru mode.
8	NC	**No Connect**
9	AGND	**Analog Ground** - (0 Volt).
10	TC	**Transmit Carrier** - This analog output is the modulated transmit data carrier. Its frequency depends upon whether the modem is in the Answer or Originate mode and if a Mark or Space condition is being sent (Table 2).
11	SL	**Select** - A High on this input selects the CCITT V.21 data transmission format. Applying a Low selects the Bell 103 data transmission format.
12	OSCi	**Oscillator Input** - A 3.579545 MHz crystal can be connected between OSCi and OSCo. All internal clock signals are derived from this time base. Additional 20 pF caps to V_{EE} from each pin are required. An external clock signal may instead be applied at the OSCi input.
13	OSCo	**Oscillator Output** -This is not connected when external clock is applied at at the OSCi input.
14	$\overline{\text{DSR}}$	**Data Set Ready** - This output, when Low, indicates to the data terminal that the modem is ready to transmit data.
15	V_{EE}	Negative power input pin (−5 V).
16	CDT	**Carrier Detect Threshold** - Applying a variable voltage between 0 and −5 V_{DC} at this input pin allows control of the receiver carrier detection threshold. This will override the internally determined threshold. If CDT is set to a voltage between +1.5 V and +2.0 V the AGC will be disabled during the test modes of pins 6 and 7.
17	DGND	**Digital Ground** - (0 Volt).
18	$\overline{\text{SH}}$	**Switch-Hook** - This input is used to manually place the device in the Originate mode. The device will make the $\overline{\text{OH}}$ output Low and start the Originate sequence if $\overline{\text{SH}}$ is Low and DTR is High. This can be a level or a momentary low going pulse input (min. 54 ms). A pulse duration of less than 27 ms will not be detected. $\overline{\text{RI}}$ should be High if $\overline{\text{SH}}$ is to be exercised. Once $\overline{\text{RI}}$ has been activated then RTS has no effect.
19	$\overline{\text{RI}}$	**Ring Indicator** - This input when High permits auto answer capability. The Data Access Arrangement should apply a Low level to $\overline{\text{RI}}$ when a ringing signal is detected. The level should be Low for at least 107 ms. The input can remain Low until reset by DTR or loss of carrier. Similarly, in Manual mode, the Answer Mode is entered by applying a Low to this input, unless RTS is High.

Pin Description (continued)

Pin #	Name	Description
20	RTS	**Request To Send** - This controls data transmission from the modulator. A High on this input with the DTR input High (in the On condition) causes the device to enter the Originate mode. $\overline{\text{OH}}$ will go Low to seize the phone line. Auto dialing can be performed by turning the RTS input High and Low to effect dial pulsing. This input must remain High for the duration of data transmission. (Auto and manual answer will not function if RTS is High.)
21	$\overline{\text{CD}}$	**Carrier Detect** - The output goes Low (On) to indicate that the receive data carrier has been received. It goes High (Off) if the received data carrier falls below the carrier detection threshold.
22	$\overline{\text{RD}}$	**Received Data** - The device presents data bits demodulated from the received data carrier at this output. This output is forced High if DTR is Low or Carrier Detect is High (Off).
23	$\overline{\text{CTS}}$	**Clear To Send** - This output goes Low at the completion of the handshaking sequence and goes High when the modem disconnects. It is always High if the device is in the Digital Loopback mode. Data to be transmitted should not be applied at the TD input until this output goes Low (active).
24	$\overline{\text{OH}}$	**Off-Hook** - This output goes to Low when either the RTS or $\overline{\text{SH}}$ input is active in the Originate mode and when a valid ring signal is detected on the $\overline{\text{RI}}$ input in the Answer mode.This output is High if DTR is Low or if the disconnect sequence has been completed.
25	DTR	**Data Terminal Ready** - A High on this input enables all the other inputs and outputs and must be present before the device will enter the data mode either manually or automatically. The device will enter an irreversible disconnect sequence if the input goes Low for more than 14 ms during a data call. A pulse duration of less than 6 ms will not be detected.
26	AL	**Analog Loopback**- This input allows the data terminal to make the telephone line busy (Off-Hook) and implement the Analog Loopback mode. A High at this input while DTR is High causes the device to make the OH output Low and to enter the Analog Loopback mode. The receive filter center frequency is switched to correspond to the transmit filter center frequency and the transmit data carrier output is internally connected to the receive data carrier input, as well as being available at TC.
27	TD	**Transmit Data** - Data bits to be transmitted are presented to this input serially by the data terminal. A High is considered a binary '1' or Mark and a Low is considered a binary '0' or Space. The data terminal should hold this input in the Mark state when data is not being transmitted. During handshaking this input is ignored.
28	CLK	**Clock** - A 4.8 kHz LSTTL compatible squarewave output is provided for supplying the 16 times clock signal required by a UART for 300 bps data rate. This output facilitates the integration of the modem function in the data terminal.

Introduction

The MT3530 is a low-speed full duplex modem designed for use in stand-alone modem applications and applications in which the modem function is designed directly into the Data Terminal Equipment (DTE). The MT3530 contains on-chip FSK modulator and demodulator, transmit and receive filters and a supervisory control section. The modem can be used in many different modes. These include Answer/Originate modes, automatic/manual modes, automatic abort, automatic disconnect and Passthru.

Functional Description

Figure 1 illustrates the functionality of the MT3530 modem. The modulator section converts input serial digital data into a squarewave of the frequency corresponding to the Mark/Space being sent. The transmit filter outputs a Frequency Shift Keying signal at the TC (Transmit Carrier) output. The frequency of the FSK signal corresponds to the fundamental frequency of the square wave at the input of the filter. The incoming analog signal from the telephone network is bandlimited (filtered) and limited (amplified/clipped) prior to the demodulator carrier input to remove adjacent channel interference and system noise. The output at the receive data pin is a digital logic "1" or "0". The supervisory control and timing section contains the necessary logic to provide initial inter-modem handshaking as well as operational protocol, such as automatic Answer, Originate only and automatic disconnect. Two diagnostic modes, analog and Digital Loopbacks, allow for system tests. In addition, Passthru mode is available whereby the protocol handshake is disabled. The modem I.C. may be operated in Bell 103/113 or CCITT V.21 type applications. The select (SL) pin defines the operating mode. See Table 2.

Operation of MT3530 Modem Chip

A. Bell 103/113

Answer Mode

In the answer mode the MT3530 is idle waiting for an incoming call. As long as DTR is High, when a Low from the ring detector is presented to $\overline{RI}$ the MT3530 sets $\overline{OH}$ and $\overline{DSR}$ Low. This enables the hook-switch relay. This connects the modem to the phone line in the Answer mode. The MT3530 waits 2.0 s (min.), then sends carrier at 2225 Hz (Mark) to the originating modem. When the originating modem returns with 1270 Hz (Mark) the carrier detect circuits turns on within 120 ms and sets $\overline{CD}$ and $\overline{CTS}$ Low, indicating the handshaking sequence is completed. Data can now be sent and received.

Originate Mode

In the Originate mode a call is initiated, if DTR is High, by applying a High to the RTS input in auto mode or a negative pulse or Low to $\overline{SH}$ in manual mode. This will cause $\overline{OH}$ to go Low pulling in the hook-switch relay to connect the telephone line, and putting the MT3530 in the Originate mode.

After a suitable time, or when dial tone is detected, RTS can be pulsed Low/High to provide dial pulses. (N.B., $\overline{OH}$ only follows RTS. The proper timing for dialing must come from the terminal on the RTS line.) The $\overline{OH}$ will go Low and High, pulsing the line with desired digits. When the answering modem comes on line it will wait 2.0 s minimum ("billing delay") and then send the 2225 Hz Answer Tone. 120 ms later the $\overline{CD}$ output goes Low indicating received carrier. 200 ms later it will respond with 592 ms (min.) of 1270 Hz carrier. At the end of that time $\overline{CTS}$ (Clear-to-Send) will go Low indicating to the terminal side that the communications link has been established.

SL (Select)	Mode	Transmit Frequency (Hz)*		Receive Frequency (Hz)*	
		Mark	Space	Mark	Space
0	Bell 103 Originate Bell 103 Answer	1270 2225	1070 2025	2225 1270	2025 1070
1	CCITT V.21 Channel 1 (Originate) CCITT V.21 Channel 2 (Answer)	980 1650	1180 1850	1650 980	1850 1180
	CCITT V.25 Answer Tone	2100			

Table 2 - Bell 103/CCITT V.21 Operating Modes

Space = Binary 0, Mark = Binary 1, Crystal Frequency = 3.579545 MHz, *Frequency drift = ±3 Hz

Abort Mode

There is an automatic abort feature in the MT3530 to avoid tying up a system should there be difficulty in establishing the link. If no carrier is detected within 14 seconds after the device has been put into the Answer or Originate mode it will abort the call by setting High $\overline{OH}$ and disconnecting the telephone line. $\overline{DSR}$ will, also, go High. This abort time can be extended by pulsing RTS Low for 1 ms minimum before the 14 seconds have elapsed. This will reset the abort timer. If it does time out DTR will need to be pulsed High to reset the MT3530. After Abort mode it resorts to Originate mode.

Shutdown Mode

Should the received carrier fall below −50 dBm during data exchange for more than 190 ms the MT3530 will terminate the call and go on-hook, disconnecting the telephone line. (See Figure 4a.)

Manual Operation

The MT3530 can be operated manually as well as automatically. To put it in the Answer mode apply a negative pulse (−5V) on $\overline{RI}$ of greater than 107 ms. If $\overline{RI}$ is tied Low then the device will go into the Answer mode whenever DTR is set High.

Similarly, to put it into the Originate mode, $\overline{SH}$ can be pulled Low for more than 54 ms. By tying $\overline{SH}$ Low, the MT3530 will go into the Originate mode whenever DTR is set High.

Passthru Mode

With the control of "TEST0" and "TEST1" pins the MT3530 can be put into the Passthru mode. See Table 3 for setup. In this mode the modem stands idle in the Originate mode and the transmit and receive functions become independent of each other. In this mode the timing and handshake protocol can be suspended, depending on the status of DTR.

With DTR set Low, the transmit and receive functions become independent of the timing and handshake protocol. All the events on Switch-Hook, Ring Indicator and Request-To-Send input pins are ignored.

With DTR High, Answer or Originate mode is selected in the same manner as in the normal mode. The transmit and receive functions are dependent on the timing and handshake protocol. Carrier Detect operates as in the normal mode. Auto

TEST0 PIN 7	TEST1 PIN 6	MT3530 STATUS	H = + 5 V (V_{DD}) L = − 5 V (V_{EE})
L	L	Normal	
H	L	Passthru	

Table 3 - Passthru Mode Control Inputs

Shutdown applies but Auto Abort does not apply. After call termination the modem is placed in the Originate mode.

B. CCITT V.21 Mode

The MT3530 will perform the same operations described above in the CCITT V.21 mode if the SL pin is tied High. The basic principle is the same but the frequencies and the timings are switched to conform to V.21 specifications. See the timing charts (Figures 3 and 4) and Table 2 for additional details. When in V.21 mode the V.25 Answer Tone of 2100 Hz will be generated upon answering.

External Clock Requirements

To use an external 3.579545 MHz clock a TTL level, 50 % duty cycle, squarewave can be applied to pin 12, OSCi, through a 0.1 µF capacitor.

Diagnostic Modes

The MT3530 has two diagnostic modes available to the operator. By putting the AL pin High while DTR is High, the device enters the Analog Loopback Mode. $\overline{OH}$ goes Low to busy out the phone line.

The receive filter center frequency moves to the transmit center frequency and TC signal is internally connected to the RC input. The transmit signal also remains available on the TC pin. Thus, any digital input at TD is coded and sent out via TC, and at the same time back through the analog input, decoded, and out on the $\overline{RD}$ pin.

By putting the DL pin High the MT3530 enters Digital Loopback mode. In this mode any data received from the remote end of the telephone line is retransmitted back to its source and $\overline{DSR}$ is forced High. Note that the digital data is not available at the $\overline{RD}$ output in this mode. See Table 4.

Test Mode	Status Lines†						
	DTR	RTS	$\overline{DSR}$	$\overline{OH}$	$\overline{CTS}$	$\overline{CD}$	$\overline{RD}$
AL	H	H	L	L	L	L	L
DL	H	H	H	L	H	H	H

Table 4 - Control Status During Diagnostic Modes

† (L = Low, H = High)

Application

Two typical MT3530 system configurations are illustrated. Figure 6 shows a stand-alone RS-232 interface modem to be used as a peripheral accessory to a communications terminal or computer.

Figure 7 shows an add-on modem for building into a computer and connecting to the internal parallel bus structure. The ACIA or UART does the parallel-to-serial and serial-to-parallel conversion required.

Both configurations are intended for direct connection to the telephone line. This requires meeting FCC Part 68 for network protection.

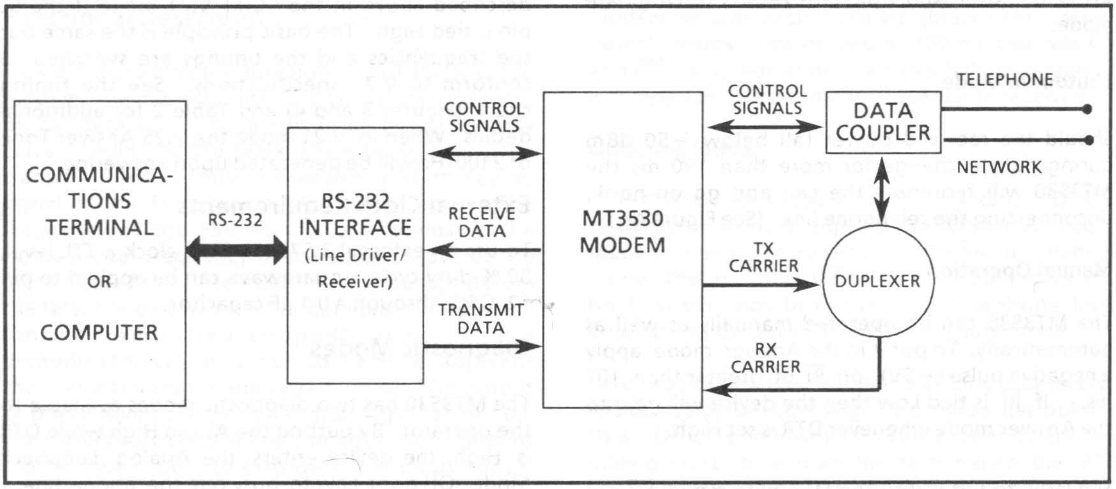


Figure 6 - Serial Interface System Configuration for MT3530

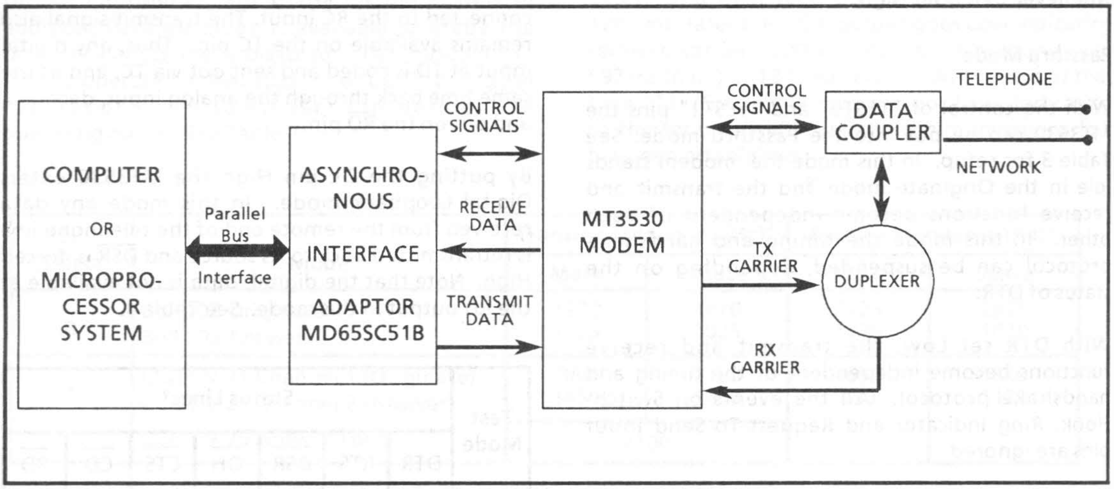


Figure 7 - Parallel Interface System Configuration for MT3530

ISO²-CMOS **MT8840**

Data Over Voice Modem

9161-002-011-NA ISSUE 4 November 1990

Features

- Performs ASK (amplitude shift keyed) modulation and demodulation
- 32 kHz carrier frequency
- Up to 2 kbit/s full duplex data transfer rate
- On-chip oscillator
- On-chip tone caller for alerting functions
- Adjustable tone caller frequencies
- Selectable self-loop test mode
- 5V/2.5mA power supply
- ISO2-CMOS and switched capacitor technologies
- 18 Pin DIP

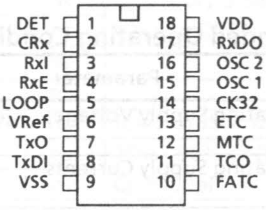
Applications

- Simultaneous data and voice communication in PABXs
- 2 kbit/s data modem
- "Smart" telephone sets

Description

The MT8840 is a carrier over voice modem which allows simultaneous transfer of voice and data over a single pair of wires. Data is transferred on anamplitude shift keyed (ASK) 32 kHz carrier. On-chip filters remove voice frequency signals from the received composite voice and data signal prior to demodulation. The modulating signal is a bit stream with a typical data rate of 2 kbit/s. In addition, the device contains a two tone warbler which functions as a telephone ringer. The device is fabricated in Mitel's double-poly ISO2-CMOS™ technology utilizing switched-capacitor techniques.

Pin Connections



Ordering Information 0°C to +85°C

MT8840AE 18 Pin PDIP
MT8840AS 18 Pin SOIC

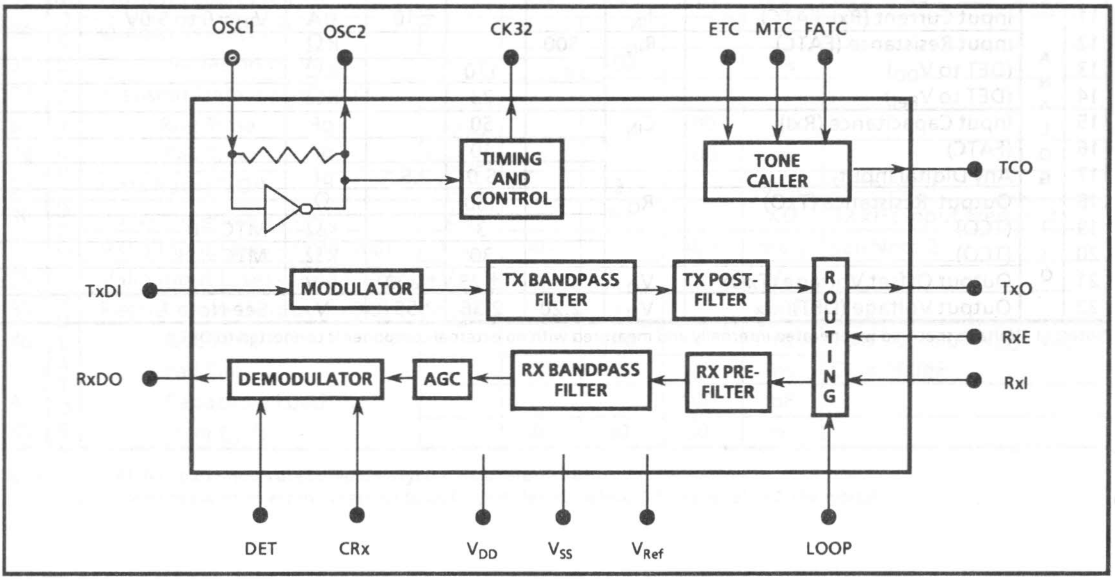


Figure 1 - Functional Block Diagram

5

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Unit
1	Supply Voltage	V_{DD}-V_{SS}	-0.3	+7.0	V
2	Voltage On Any Pin	V_{Max}	V_{SS}-0.3	V_{DD}+0.3	V
3	Current On Any Pin	I_{Max}		20	mA
4	Storage Temperature	T_S	-65	+150	°C
5	Package Power Dissipation	P_{Diss}		850	mW

*Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

	Parameter	Symbol	Min	Typ	Max	Unit
1	Operating Supply Voltages	V_{DD}	4.75	5	5.25	V
2		V_{Ref}		0.4V_{DD}		V
3	Operating Supply Currents	I_{DD}		2.5	5.0	mA
4		I_{Ref}			200	µA
5	Operating Temperature	T_O	0		+85	°C
6	Load Capacitance (TxO)	C_L			50	pF
7	Load Resistance (TxO)	R_L	10			KΩ

D.C. Characteristics - V_{DD} = 5.0 V ± 5% V_{SS} = 0V T = 0 - 85°C (All voltages are referenced to V_{SS} /GND)

		Characteristics	Sym	Min	Typ	Max	Unit	Test Conditions
1	DIGITAL I/O	Input Current	I_{IN}			±10	µA	V_{IN}=0 to V_{DD}
2		Input Low Voltage	V_{IL}	0		1.5	V	
3		Input High Voltage	V_{IH}	3.5		5.0	V	
4		Output Low Voltage	V_{OL}			0.4	V	I_{OL}=0.4mA
5		Output High Voltage	V_{OH}	4.6			V	I_{OH}=0.4mA
6		Output Drive Current						
7		N Channel Sink (Except OSC2)	I_{OL}	0.4			mA	V_{OL}=0.4V
8		OSC2		0.1			mA	
9		P Channel Source (Except OSC2)	I_{OH}	0.4			mA	V_{OH}=4.6V
10		OSC2		0.1			mA	
11	ANALOG I/O	Input Current (RxI, FATC)	I_{IN}			±10	µA	V_{IN}=0 to 5.0V
12		Input Resistance (FATC)	R_{IN}	500			KΩ	
13		(DET to V_{DD})			170		KΩ	
14		(DET to V_{Ref})			23		KΩ	
15		Input Capacitance (RxI)	C_{IN}		50		pF	
16		(FATC)			10		pF	
17		Any Digital Input			5.0	7.5	pF	
18		Output Resistance (TxO)	R_O		100		Ω	
19		(TCO)			3		KΩ	MTC=0
20		(TCO)			30		KΩ	MTC=1
21		Output Offset Voltage (TxO)	V_O		±25	±200	mV	
22		Output Voltage (DET)	V_O	2.20	2.36	2.55	V	See Note 1

Notes: 1. Voltage specified is generated internally and measured with no external components connected to DET

A.C. Characteristics - $V_{DD}=5.0V \pm 5\%$ $V_{SS}=0V$ $T=0$ - 85°C (All voltages are referenced to V_{SS}/GND)

		Characteristics	Sym	Min	Typ	Max	Unit	Test Conditions
1	DIGITAL I/O	Crystal/Clock Frequency	f_C	3.5759	3.5795	3.5831	MHz	OSC 1, OSC 2
2		Clock Input (OSC 1)						
3		Rise Time	t_{LHCI}			100	ns	10% - 90% of (V_{DD} - V_{SS})
4		Fall Time	t_{HLCI}			100	ns	
5		Duty Cycle	DC_{CI}	40	50	60	%	
6		Clock Output (OSC 2)						
7		Rise Time	t_{LHCO}		100		ns	$C_L=30pF$, 3.58MHz ext.
8		Fall Time	t_{HLCO}		100		ns	clock to OSC1
9		Duty Cycle	DC_{CO}		50		%	
10		Capacitive Load	C_{LCO}			30	pF	
11		Clock Output (CK32)	F_{C32}	32508	32541	32574	Hz	fc=3.5795MHz
12		Rise Time	t_{LH32}		100		ns	10% - 90% of (V_{DD} - V_{SS})
13		Fall Time	t_{HL32}		100		ns	$C_L=100pF$
14		Duty Cycle	DC_{32}		50		%	
15		Capacitive Load	C_{L32}			100	pF	
16	TONE CALLER	Warbler Frequency (TCO)	f_W	7.935	7.945	7.955	Hz	fc=3.5795MHz±0.1%
17		Low Tone Frequency	f_{LT}	352	390	428	Hz	FATC=0, f_c=3.5795MHz
18				1036	1148	1260	Hz	FATC=V_{DD}, f_c=3.5795MHz
19		High Tone Frequency	f_{HT}	440	487	535	Hz	FATC=0, f_c=3.5795MHz
20				1295	1434	1574	Hz	FATC=V_{DD}, f_c=3.5795MHz
21		Harmonic Relationship	f_{HT}/f_{LT}		1.25			
22		Warbler Output ($\overline{TCO}$)						
23		Rise Time	t_{LHWO}		500		ns	100KΩ load to V_{Ref}
24		Fall Time	t_{HLWO}		500		ns	$C_L=30pF$, MTC=0
25		Duty Cycle	DC_{WO}		50		%	
26		Output Level (TCO)	V_{TCC}		V_{DD}		V_{pp}	MTC=0
27					0.625		V_{pp}	MTC=1 (100KΩ load to V_{Ref})
28	MODULATOR	Modulated Frequency	f_{MOD}		32541		Hz	
29		Output Level (TxO)	V_{TxO}	225	250	270	mV_{pp}	V_{DD} = 5V
30		Output Level (TxO)						
31		variation vs. V_{DD}	V_{TxO}		100		%	
32		Transmit Data Input (TxDI)						
33		Rise Time	t_{LHTxDI}			100	ns	
34		Fall Time	t_{HLTxDI}			100	ns	
35		Data Rate (TxDI)	f_{Data}		2		kbit/s	See Note 1
36	DEMODULATOR	Input Impedance (RxI)	Z_{IN}		50		KΩ	32 kHz Input Frequency
37		Valid Input Level - Data (RxI)	V_{RxI}	40		400	mV_{pp}	See Note 2
38		Valid Input Level - Data + Voice	V_{RxI}			3.0	V_{pp}	
39		Receive Data Output (RxDO)	f_{Data}		2		kbit/s	
40		Rise Time			100		ns	10% - 90% of (V_{DD} - V_{SS})
41		Fall Time			100		ns	C_L = 100pF
42		Capacitive Load				100		pF	
43		Duty Cycle		40	50	60	%	

Notes:
1. All A.C. parameters are based on a typical data rate of 2 kbit/s.
2. Measured with no external resistor to DET input. Detection level internally set to 2.36V typical

A.C. Characteristics (Continued)

		Characteristics	Sym	Min	Typ	Max	Unit	Test Conditions
44	DEMOD	Inband Noise Rejection (S/N)		12			dB	Input Sig. (RxI) = $400mV_{pp}$
45		Attenuation to Voice Signals		40			dB	f_{in} = 0 - 5KHz
46		Detect Filter Q	Q		3.8			
47		Detector Center Frequency			32		kHz	

Pin Description

Pin #	Name	Description	
1	DET	Demodulator detection level adjust input (Analog). Internal resistor divider applies 2.36V in open circuit condition. Connection of external resistor will vary detect level.	
2	CRx	External AGC time constant adjust input (Analog). Connect external capacitor to V_{SS}.	
3	RxI	Modulated receive signal input (Analog). Biased at V_{Ref}.	
4	RxE	Receive enable input (Digital) with internal pull up. Active high.	
5	LOOP	Self-test mode select input (Digital) with internal pull down. Active high.	
6	V_{Ref}	Internal reference supply voltage input (Analog).	
7	TxO	Modulated transmit carrier output (Analog).	
8	TxDI	Transmit data input (Digital).	
9	V_{SS}	Negative power supply.	
10	FATC	Tone caller center frequency adjust input (Analog).	
11	TCO	Tone caller output (Digital).	
12	MTC	Mute tone caller input (Digital) with internal pull down. Active high.	
13	ETC	Enable tone caller input (Digital) with internal pull down. Active high.	
14	CK32	32 kHz data strobe output (Digital).	
15	OSC1	Clock Input	3.579545 MHz crystal connected between these pins completes internal oscillator.
16	OSC2	Clock Output to drive external devices.	
17	RxDO	Receive data output (Digital). Synchronized to CK32.	
18	V_{DD}	Positive power supply.	

Functional Description

The MT8840 contains the modulator and demodulator circuitry for 32 kHz ASK signalling as well as a two-tone warbler (tone caller) to replace the function of the mechanical telephone ringer.

A 32 kHz carrier is 100% amplitude modulated by the digital bit stream applied to input TxDI. This results in an amplitude shift keyed (ASK) 32 kHz carrier. A logical high at TxDI disables the carrier and a logical low enables it. The digitally modulated waveform is shaped by the Tx BANDPASS FILTER and smoothed by the Tx POST FILTER. The signal then enters the routing block where it is transferred to the TxO output.

The modulated 32 kHz receive signal is applied to RxI. With a logical low applied to LOOP and a logical high applied to RxE, receive signals are routed to the Rx PREFILTER. High frequencies are removed by the Rx PREFILTER to prevent aliasing in the switched capacitor Rx BANDPASS FILTER. Voice signals are removed by the bandpass filter which is followed by an AGC circuit. This provides a dynamic range of 20dB for the receiver. An external 1µF capacitor connected from CRx to V_{SS} is required to control the AGC attack and decay time constants. Data is recovered from the received signal in the demodulator. The minimum voltage level to which the demodulator responds may be adjusted by connecting a resistor from DET to V_{DD} or V_{Ref}. Since DET is the input to a comparator, noise should be kept to a minimum at this pin. The recovered receive data is synchronized to the leading edge of the 32 kHz clock (available at CK32) before appearing at RxDO.

When in loop around mode, the Rx PREFILTER input is internally disconnected from the RxI input pin and connected to TxO. The transmitter output is still available at TxO.

A two tone warbling audio signal is available at TCO when the tone caller enable input (ETC) is high. TCO is internally clamped to V_{Ref} when the tone caller is disabled. The tone output can be attenuated by 20dB if a logical high is applied to the tone caller mute input (MTC).

Applications

Figures 2 through 4 show how the MT8840 may be utilized to transfer data and voice simultaneously over a single pair of wires in digital or analog PABXs and "smart" telephone sets. In all three figures a microprocessor sends/receives data to/from the MT8840 via a UART which converts the data format from parallel-to-serial or serial-to-parallel for the transmit and receive directions respectively. In the receive direction the MT8840 has on-board filters to reject voice-band signals leaving only the 32 kHz carrier. This carrier is then demodulated to recover the received data. In the transmit direction the data to be sent is modulated and passed on to a summing circuit which sums the modulated 32 kHz carrier and voiceband signals for transmission over the telephone line. In the PABX the Filter/Codec has filters which reject the 32 kHz carrier from the received composite voice and data signal allowing only voiceband signals to pass through which are then PCM encoded for digital switching. However, in both the analog PABX and smart telephone set, lowpass filters could be included to bandlimit the received signal leaving only voice signals to be passed on to the switch array or handset earpiece.

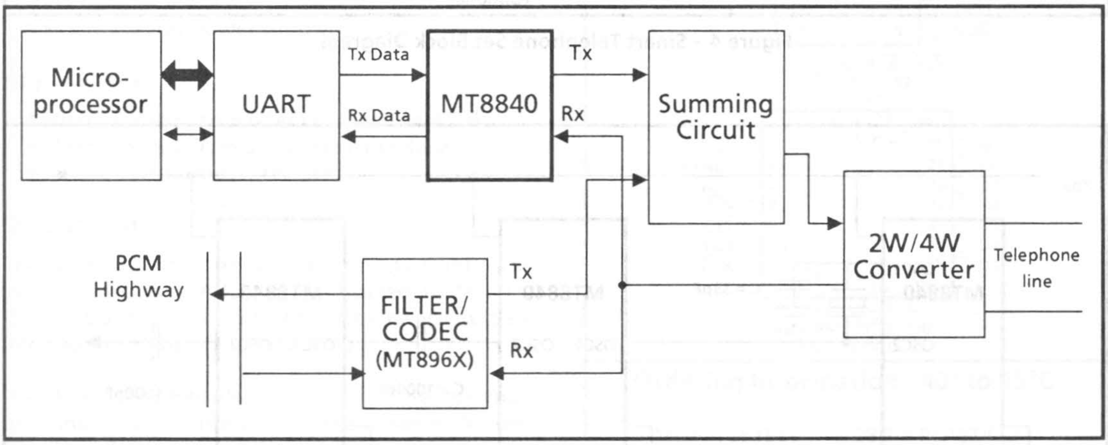


Figure 2 - Digital PABX Block Diagram

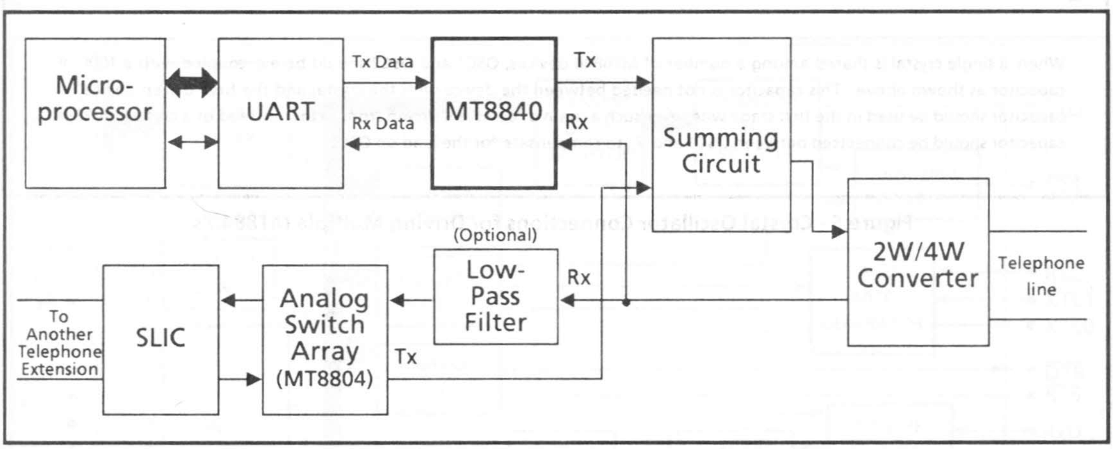


Figure 3 - Analog PABX Block Diagram

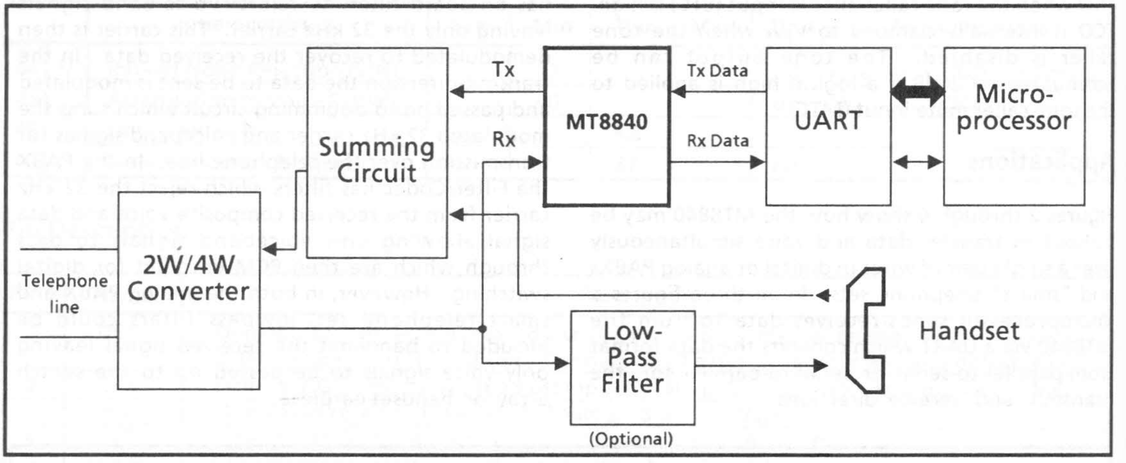
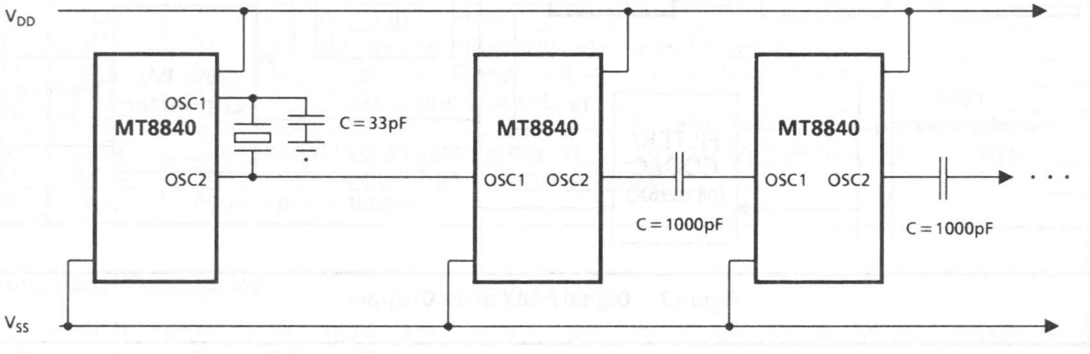


Figure 4 - Smart Telephone Set Block Diagram



When a single crystal is shared among a number of MT8840 devices, OSC1 and OSC2 should be a.c. coupled with a 1000 pF capacitor as shown above. This capacitor is not needed between the device with the crystal and the first driven device. A capacitor should be used in the first stage whenever such a chain of devices is driven from a clock instead of a crystal. A 33pF capacitor should be connectced between OSC1 and V_{ss} to compensate for the load on OSC2.

Figure 5 - Crystal Oscillator Connections for Driving Multiple MT8840's

Asynchronous Communications Interface Adaptor

9161-002-052 NA ISSUE 5 November 1990

Features

- Replacement for existing NMOS part.
- 15 selectable baud rates from 50 bit/s to 19.2 kbit/s or 1/16th of an external clock rate.
- Selectable word length & number of stop bits.
- Selectable echo mode.
- Full or half duplex operation.
- Data set/modem control functions.
- Parity generation and checking.
- Low power ISO-CMOS technology.
- TTL compatible.
- Single 3-6 volt power supply.

Applications

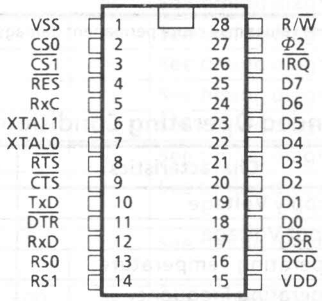
- Microprocessor to modem bidirectional link.
- Microprocessor (μP) serial data interface.
- Serial input/output interface.

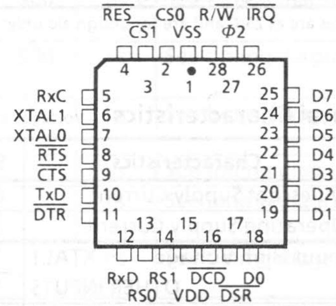
Description

The MD65SC51B is an Asynchronous Communications Interface Adaptor fabricated in Mitel's ISO-CMOS technology. The device provides interfacing between a μP and a modem.

The MD65SC51B will also control all of the interrupt handling between the μP and the modem. An on-board baud rate generator is available to derive one of 15 selectable baud rates or 1/16th of an external clock rate.

Pin Connections





Ordering Information -40° to 85°C

MD65SC51BE	28 Pin PLASTIC DIP
MD65SC51BP	28 Pin PLCC

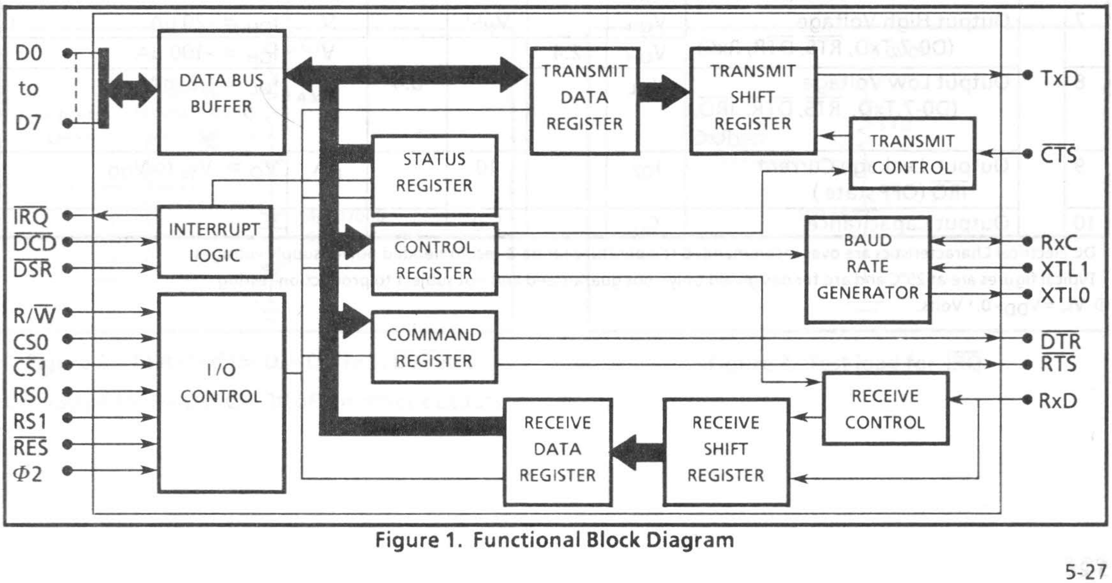


Figure 1. Functional Block Diagram

Absolute Maximum Ratings*

	Parameter		Symbol	Min	Max	Units
1	Supply Voltage		V_{DD} - V_{SS}	- 0.3	7.0	V
2	Voltage on any I/O pin		V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Current on any I/O pin		I_I		±10	mA
4	Storage Temperature		T_S	-65	+150	°C
5	Power Dissipation	Plastic	P_D		0.6	W
		Ceramic	P_D		1.0	W

*Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	3.0	5.0	6.0	V	
2	Input Voltage	V_I	0		V_{DD}	V	
3	Operating Temperature	T_A	-40	+25	+85	°C	
4	Operating Frequency	f	0		2.0	MHz	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1		Quiescent Supply Current	I_{DD1}		2		μA	Outputs Unloaded
2		Operating Supply Current	I_{DD}		2		mA/MHz	Outputs Unloaded
3	INPUTS	Input High Voltage XTAL1	V_{IH}	3.0		V_{DD}	V	
		OTHER INPUTS	V_{IH}	2.0		V_{DD}	V	
4		Input Low Voltage	V_{IL}	0		0.8	V	
5		Input Leakage Current RxC, (D_0-D_7)	I_{IZ}			10	μA	V_{IN}=0 to V_{DD}
		Other Inputs (Except XTAL1)	I_{IZ}			2.5	μA	V_{IN}=0 to V_{DD}
6		Input Capacitance (D_0-D_7)	C_{IN}		5.0		pF	
		Other Inputs (Except XTAL1)	C_{IN}		10.0		pF	
7		Output High Voltage	V_{OH}		V_H①		V	I_{OH} = -20 μA
		(D0-7,TxD, $\overline{RTS}$, $\overline{DTR}$, RxC)	V_{OH}	2.4			V	I_{OH} = -100 μA
8		Output Low Voltage (D0-7,TxD, $\overline{RTS}$, $\overline{DTR}$, $\overline{IRQ}$, RxC)	V_{OL}			0.4	V	I_{OL} = 1.6 mA
9		Output Leakage Current $\overline{IRQ}$ (OFF state)	I_{OZ}		10		μA	V_O = V_{SS} to V_{DD}
10		Output Capacitance	C_O		5.0		pF	

† DC Electrical Characteristics are over recommended temperature range & recommended power supply voltages.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

① V_H = V_{DD} - 0.1 Volts.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes
1	MPU INTERFACE	Φ_2 Cycle Period	t_{CYC}	500	310		ns	See timing diagram 1
2		Φ_2 HIGH Pulse Width	t_C	200			ns	See timing diagram 1
3		Address Setup Time	t_{AS}	70			ns	See timing diagram 2, 3
4		Address Hold Time	t_{AH}	0			ns	See timing diagram 2, 3
5		Φ_2 to Valid Data Delay	t_{DDR}			150	ns	See timing diagram 2
6		Data Hold Time (Read)	t_{DHR}	10			ns	See timing diagram 2
7		Data Setup Time (Write)	t_{DSW}	60			ns	See timing diagram 3
8		Data Hold Time (Write)	t_{DHW}	10			ns	See timing diagram 3
9		Read/Write Setup Time	t_{RWS}	70			ns	See timing diagram 2,3
10		Read/Write Hold Time	t_{RWH}	0			ns	See timing diagram 2,3
11	COMMUNICATION INTERFACE	External TxD Clock Cycle Period	t_{ECP}	0.4			µs	See timing diagram 4
12		External TxD Clock High Duration	t_{ECH}	175			ns	See timing diagram 4
13		External TxD Clock Low Duration	t_{ECL}	175			ns	See timing diagram 4
14		External Clock to Valid Data Transmitted	t_{TXDD}			500	ns	See timing diagram 4
15		$\overline{RTS}$ and $\overline{DTR}$ Propagation Delay from Φ_2	t_{DLY}			500	ns	See timing diagram 5
16		$\overline{IRQ}$ Propagation Delay from $\Phi 2$ (CLEAR)	t_{IRQD}			500	ns	See timing diagram 5
17		External RxD Clock Cycle Period	t_{ECP}	0.4			µs	See timing diagram 6
18		External RxD Clock High Duration	t_{ECH}	175			ns	See timing diagram 6
19		External RxD Clock Low Duration	t_{ECL}	175			ns	See timing diagram 6

† Timing is over recommended temperature range & recommended power supply voltages. Test loads shown in Figures 2 and 3.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Note : Rise and Fall times (t_R & t_F) are 10 to 30 ns.

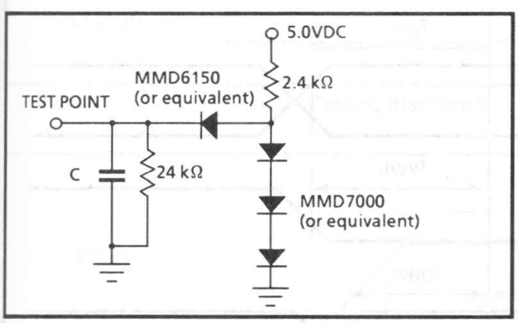


Figure 2. Test load for D_0 - D_7, TxD, $\overline{DTR}$ $\overline{RTS}$

C= 130 pF for D_0-D_7, C= 30 pF for other outputs

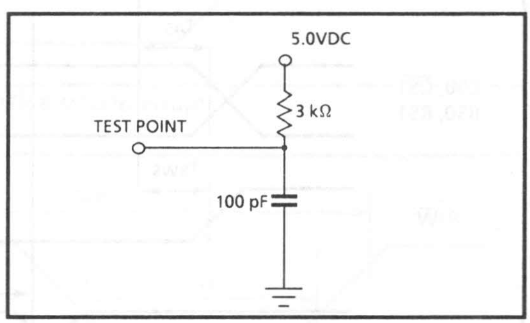
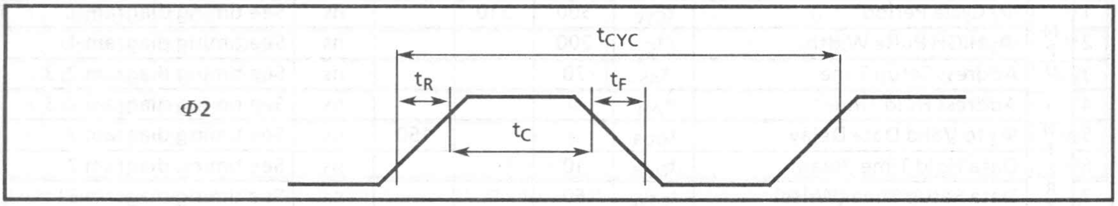


Figure 3. Test load for $\overline{IRQ}$

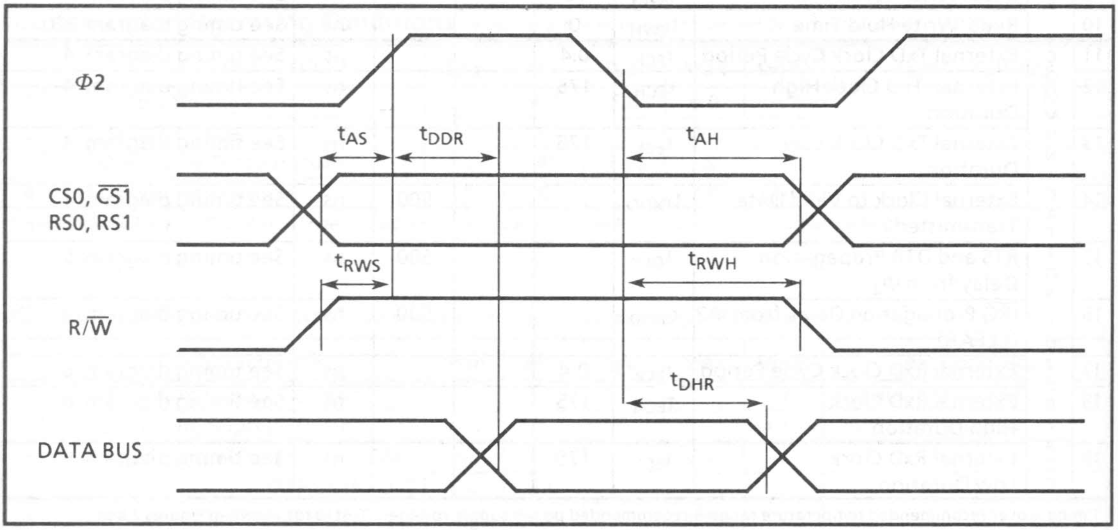
5

Timing Diagrams

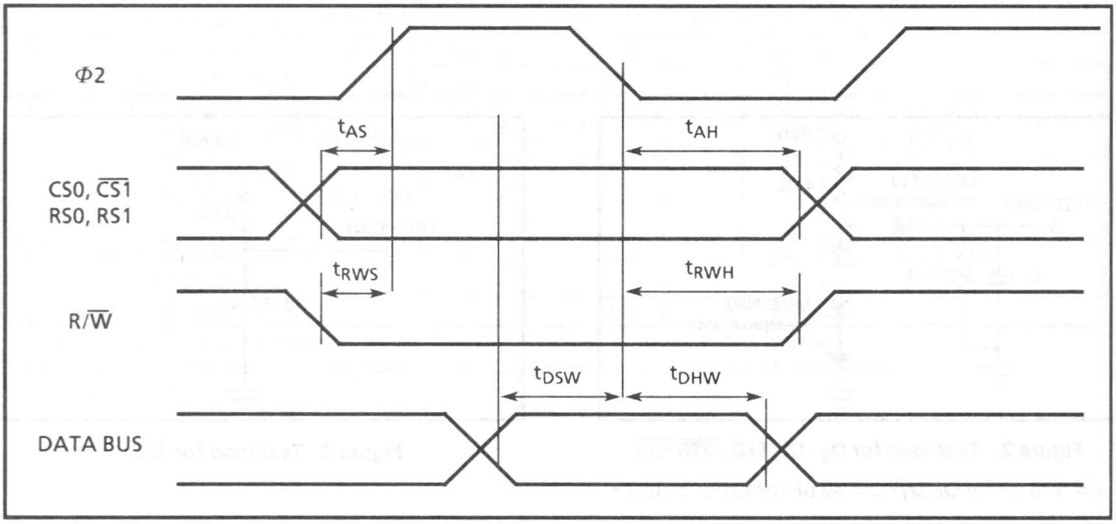
The points from which these timing values are measured are V_{IH} & V_{IL} for inputs and V_{OH} & V_{OL} for outputs.



Timing diagram 1 - Φ2 clock



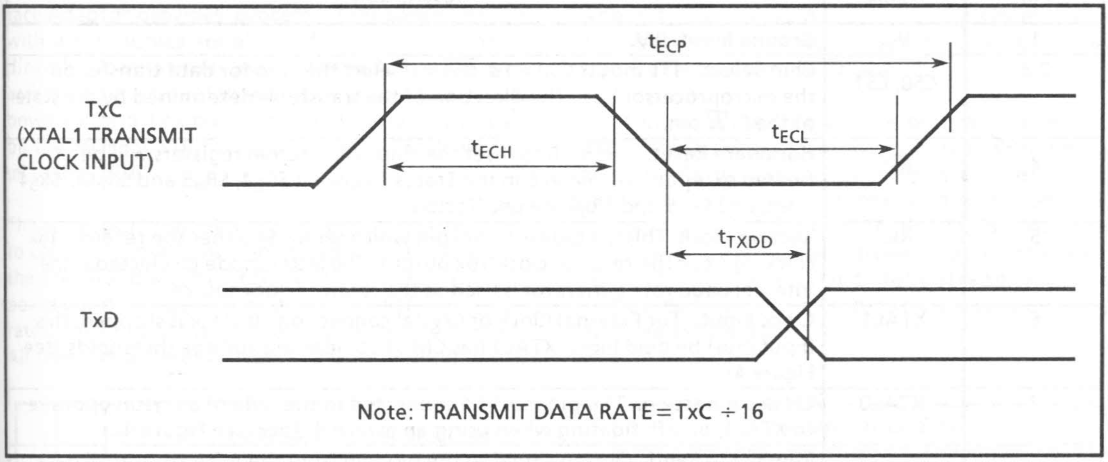
Timing diagram 2 - MPU Read Cycle



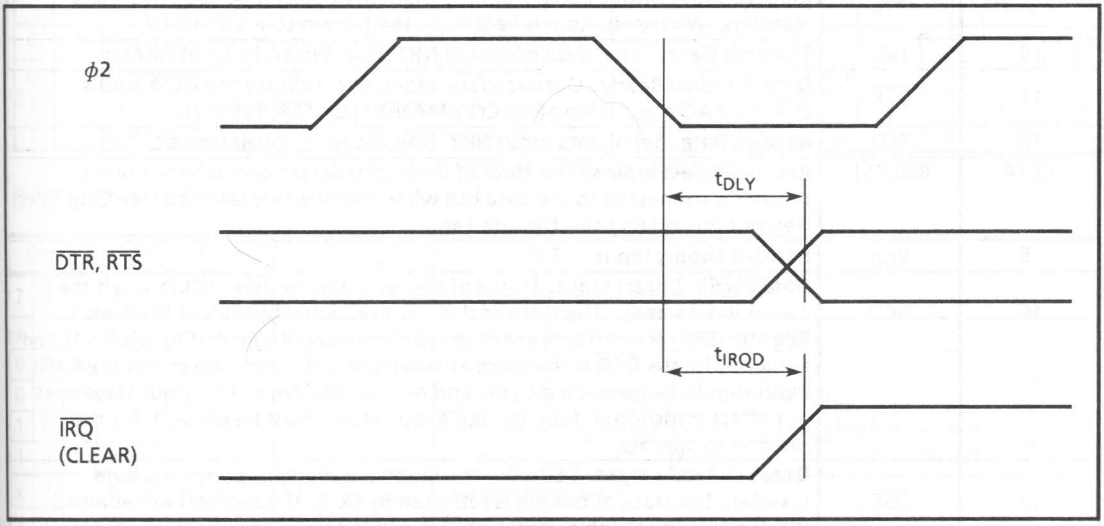
Timing diagram 3 - MPU Write Cycle

Timing Diagrams

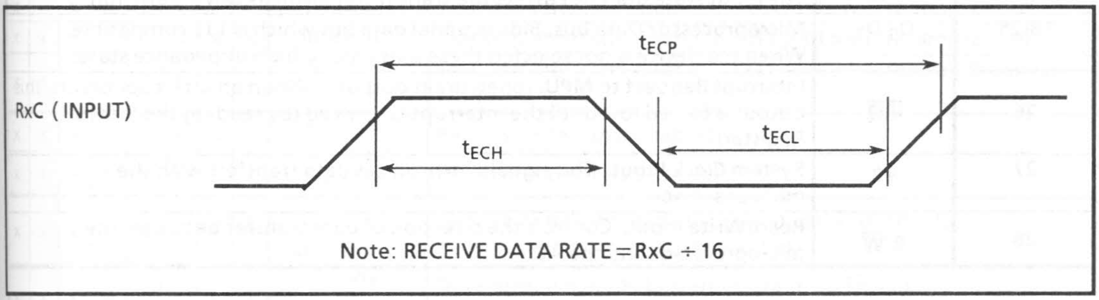
The points from which these timing values are measured are V_{IH} & V_{IL} for inputs and V_{OH} & V_{OL} for outputs.



Timing diagram 4 - Transmit Data with External Clock



Timing diagram 5 - $\overline{RTS}$, $\overline{DTR}$ & MPU Interrupt



Timing diagram 6 - Receive External Clock Timing

Pin Description

Pin	Name	Description
1	V_{SS}	**Ground Input.** 0 V.
2,3	CS0, $\overline{CS1}$	**Chip Select.** TTL inputs CS0 = 1& $\overline{CS1}$ = 0 select the chip for data transfer on the microprocessor bus. The direction of the transfer is determined by the state of the R/$\overline{W}$ pin.
4	$\overline{RES}$	**Hardware Reset.** $\overline{RES}$ = 0 to reset the chip. All internal registers will be cleared except bits 4, 5 and 6 in the Status Register (SR_b4, SR_b5 and SR_b6). SR_b4 is set, and SR_b5 and SR_b6 are unaffected.
5	RxC	**Receive Clock.** This is a bidirectional pin which serves as either the receiver 16x clock input or the receiver clock 16x output. The latter mode is selected if the internal baud rate generator is used as the receiver clock source.
6	XTAL1	**Clock Input.** For External Clock or Crystal connection. If clock is stopped, this input must be held high. XTAL1 has CMOS compatible voltage thresholds (see Figure 4).
7	XTAL0	**Clock connection.** This pin must be connected to the side of a crystal opposite to XTAL1, or left floating when using an external clock (see Figure 4).
8	$\overline{RTS}$	**Request to Send.** Output signal to the modem from the ACIA to control data transfers (see COMMAND REGISTER, Table 2).
9	$\overline{CTS}$	**Clear to Send.** Input signal from the modem to the ACIA to control data transfers. When this input is held high, the transmitter is disabled.
10	TxD	**Transmit Data.** Serial data output in NRZ (Non Return to Zero) format.
11	$\overline{DTR}$	**Data Terminal Ready.** Output to the modem to indicate the ACIA status. $\overline{DTR}$ = 1 if ACIA is disabled (see COMMAND REGISTER, Table 2).
12	RxD	**Receive Data.** Serial data input NRZ (Non Return to Zero) format.
13,14	RS0,RS1	**Register Select Inputs.** The state of these pins determines which internal register is connected to the data bus when the device is selected (see Chip Select Description and Register Decode Table).
15	V_{DD}	**Positive Supply Input.** +5 V.
16	$\overline{DCD}$	**Data Carrier Detect Input.** Status of carrier at the modem. [$\overline{DCD}$ = 0 if the carrier is detected]. The state of this pin is reflected by bit 5 of the Status Register (SR). If interrupts are enabled (Command Register (CR) bit 0 = 1), and the logical state $\overline{DCD}$ is changed, an interrupt will occur. When not used, this input should be connected to ground or to a logic high. The input state does not affect transmitter function but a logical low must be present for the receiver to operate.
17	$\overline{DSR}$	**Data Set Ready Input.** $\overline{DSR}$ = 0 if the modem is ready to perform a data transfer. The state of this pin is reflected by SR_b6. If interrupts are enabled (CR_b0 = 1), and the logical state of $\overline{DSR}$ is changed, an interrupt will occur . When not used, this input should be connected to ground or to a logic high. The input state does not affect the transmitter or the receiver function.
18-25	D_0-D_7	**Microprocessor Data Bus.** Bidirectional data bus which is TTL compatible. When the device is not selected these pins enter a high impedance state.
26	$\overline{IRQ}$	**Interrupt Request to MPU.** (open drain output). When an interrupt occurs, this output is forced low until the interrupt is serviced (by reading the Status Register).
27	ϕ_2	**System Clock Input.** This signal synchronizes data transfers with the microprocessor.
28	R/$\overline{W}$	**Read/Write Input.** Controls the direction of data transfer between the microprocessor and the ACIA.

Functional Description

MD65SC51B Asynchronous Communications Interface Adaptor provides processor (μP) based systems with a full duplex serial interface. The μP port is directly compatible with 6800/6500 style bus architectures. Coupled with the Status Register, a powerful and flexible interrupt facility is included on the MD65SC51B to allow fast response from the μP to the ACIA.

The serial port provides signals which may be used to control a communication channel compatible to the EIA Standard RS-232C specification. An on-board baud rate generator allows 16 different baud rates, for data transmission and reception timing. All frequencies are derived from an external clock or crystal. The receive frequency may be received separately from the transmit frequency, allowing reception and transmission at independent speeds. Alternatively, the ACIA will produce a signal that is 16 times the baud rate, for use by a remote ACIA (See Pin Description - RxC).

The format of the data word is programmable. The word length ranges from five to nine bits (including parity). Parity can be odd, even or deselected altogether. The parity bit may also be forced high or low. Either 1, 1.5, or 2 stop bits may be added to the end of the serial data stream. For maintenance applications, the received data stream may be looped back onto the transmit data stream using echo mode operation.

RS1	RS0	Internal Register Selected		Reset Operation Effect															
				Hardware Reset								Programmed Reset							
		Write	Read	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
0	0	Transmit Data Register	Receive Data Register	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
0	1	Programmed Reset	Status Register	0	-	-	1	0	0	0	0	-	-	-	-	-	0	-	-
1	0	Command Register	Command Register	0	0	0	0	0	0	0	0	-	-	-	0	0	0	0	0
1	1	Control Register	Control Register	0	0	0	0	0	0	0	0	-	-	-	-	-	-	-	-

Table 1 - Register Address Decoding

Note: "-" denotes no change from state previous to reset

7	6	5	4	3	2	1	0	Control Function	Resulting Function
x	x	0	x	x	x	x	x	Parity Mode Control	No Parity Bit transmitted or received.
0	0	1	x	x	x	x	x		Odd Parity Bit transmitted or received.
0	1	1	x	x	x	x	x		Even Parity Bit transmitted or received.
1	0	1	x	x	x	x	x		Parity Bit set to MARK (Receive parity check disabled).
1	1	1	x	x	x	x	x		Parity Bit set to SPACE (Receive parity check disabled).
x	x	x	0	x	x	x	x	Echo Mode Enable	Normal Operation.
x	x	x	1	0	0	x	x		Echo Mode Enabled (bits 2 and 3 must be 0).
x	x	x	x	0	0	x	x	Transmit Interrupt Control	Transmit interrupt disabled. $\overline{RTS}$ set High (Transmitter off).
x	x	x	x	0	1	x	x		Transmit interrupt enabled. $\overline{RTS}$ set Low (Transmitter on).
x	x	x	x	1	0	x	x		Transmit interrupt disabled. $\overline{RTS}$ set Low (Transmitter on).
x	x	x	x	1	1	x	x		Transmit interrupt disabled. $\overline{RTS}$ set Low (Transmit Break on TxD).
x	x	x	x	x	x	0	x	Receiver Interrupt Enable	Receiver interrupts enabled.
x	x	x	x	x	x	1	x		Receiver interrupts disabled.
x	x	x	x	x	x	x	0	Data Terminal Ready	Data terminal not ready to transfer data ($\overline{DTR}=1$). Receiver and all interrupts disabled.
x	x	x	x	x	x	x	1		Data terminal ready to transfer data ($\overline{DTR}=0$). Receiver and all interrupts enabled.

Table 2 - Command Register Description

Note: "x" is intended to represent don't care in all binary representations in this and all following tables.

Serial Interface Description

Transmitted and Received Data

Data is transmitted from the ACIA on the TxD pin, and received on the RxD pin. The inactive state of either data channel (RxD or TxD) is a mark condition (logical high). This type of data code is termed Non-Return to Zero (NRZ). Data transmitted or received by the MD65SC51B is always preceded by a "start bit".

The start bit is a space condition (logical low) which signifies the start of active data on the channel. The receiving ACIA also uses the start bit to optimize its sampling for the middle of the data bits that follow. Between received words, the ACIA samples the channel at 16x Baud rate. When a low is detected, the ACIA waits half a bit period before sampling again. This delay allows subsequent bits (sampled at the same frequency as the baud rate) to be sampled as far from the bit boundaries as possible. Noise or "glitch" immunity is also added by this mechanism. Low going pulses of less than 1/2 a bit period wide will not be mistaken for the start bit (the ACIA resumes the 16x sampling rate).

Data bits following the start bit are in ascending order, with the least significant bit (LSB) first, and the most significant bit (MSB) last. The MSB depends on the number of bits per word selected; the ACIA can be programmed for 5 bit, 6 bit, 7 bit or 8 bit data word transmission/reception. Each bit has a period equal to the reciprocal of the selected baud rate, which in turn is dependent on the clock source frequency (see Table 4).

Parity sensing and generation can be chosen for odd parity, even parity or no parity. When parity is selected, the parity bit follows the MSB of the data word. For even parity, the condition of the parity bit will be such that there are an even number of

Control Register Bit								Control Function	Resulting Function
7	6	5	4	3	2	1	0		
0	x	x	x	x	x	x	x	Stop Bit Control	1 stop bit.
1	x	x	x	x	x	x	x	Stop Bit Control	2 stop bits except in the following cases: a/ 1 stop bit if word length set for 8 bits & parity enabled ② b/ 1.5 stop bits if word length set for 5 bits & parity disabled
x	0	0	x	x	x	x	x	Word Length Setting	8 bits
x	0	1	x	x	x	x	x	Word Length Setting	7 bits.
x	1	0	x	x	x	x	x	Word Length Setting	6 bits.
x	1	1	x	x	x	x	x	Word Length Setting	5 bits.
x	x	x	0	x	x	x	x	Receiver Clock Source	External clock source. (RxC is Input)
x	x	x	1	x	x	x	x	Receiver Clock Source	Internal baud rate generator. (RxC is Output)
x	x	x	x	0	0	0	0	Baud Rate Control	115.2 kbaud① or (Frequency) ÷ 16
x	x	x	x	0	0	0	1	Baud Rate Control	50 baud① or (Frequency) ÷ 36,864
x	x	x	x	0	0	1	0	Baud Rate Control	75 baud① or (Frequency) ÷ 25,576
x	x	x	x	0	0	1	1	Baud Rate Control	109.92 baud① or (Frequency) ÷ 16,769
x	x	x	x	0	1	0	0	Baud Rate Control	134.58 baud① or (Frequency) ÷ 13,704
x	x	x	x	0	1	0	1	Baud Rate Control	150 baud① or (Frequency) ÷ 12,288
x	x	x	x	0	1	1	0	Baud Rate Control	300 baud① or (Frequency) ÷ 6,144
x	x	x	x	0	1	1	1	Baud Rate Control	600 baud① or (Frequency) ÷ 3,072
x	x	x	x	1	0	0	0	Baud Rate Control	1200 baud① or (Frequency) ÷ 1,536
x	x	x	x	1	0	0	1	Baud Rate Control	1800 baud① or (Frequency) ÷ 1,024
x	x	x	x	1	0	1	0	Baud Rate Control	2400 baud① or (Frequency) ÷ 768
x	x	x	x	1	0	1	1	Baud Rate Control	3600 baud① or (Frequency) ÷ 512
x	x	x	x	1	1	0	0	Baud Rate Control	4800 baud① or (Frequency) ÷ 384
x	x	x	x	1	1	0	1	Baud Rate Control	7200 baud① or (Frequency) ÷ 256
x	x	x	x	1	1	1	0	Baud Rate Control	9600 baud① or (Frequency) ÷ 192
x	x	x	x	1	1	1	1	Baud Rate Control	19.2 kbaud① or (Frequency) ÷ 96

Table 4 - Control Register Description

Notes : ① The preset baud rates given assume a crystal frequency of 1.8432 MHz
② To enable and disable parity, see Table 2.

marks when considering the data word and the parity bit. With odd parity, the condition of the parity bit will be such that there is an odd number of marks when considering the data word and the parity bit (both cases exclude the start and stop bits).

Transmit and Receive Clocks

The signals used by the ACIA for transmit/receive timing are found on three pins: XTAL0, XTAL1 and RxC. XTAL1 and XTAL0 are the input and output, respectively, of a crystal oscillator circuit. The crystal can be connected to these pins as seen in Figure 4. This oscillator circuit drives the internal baud rate generator, which divides the squarewave output of the oscillator by the divisor selected (see Table 4). If a crystal is not used, an external clock may drive the oscillator input while the oscillator output is left floating. If the clock is stopped (device still powered), the oscillator input should be held to a logical high.

The clock for the receiver may be taken from one of two sources: the output of the internal baud rate generator, or from an external clock input on the RxC pin. In the latter case, the baud rate is 1/16th of the external clock. If the source of receiver timing is the internal baud rate generator, RxC becomes an output and sources a clock 16 times (16x) the baud rate (for driving remote ACIAs).

Control Signals

These signals are compatible with the RS-232C modem control circuits. The signals are the Request To Send ($\overline{RTS}$), Data Terminal Ready

Characteristics	Spec.
Temperature stability @ -45 to +85°C	±0.01%
Frequency* (MHz)	1.8432
Frequency tolerance* (±%)	0.02
Resonance mode*	parallel
Equivalent resistance* (ohms)	400 max.
Drive level* (mW)	2
Shunt capacitance* (pF)	7 max.
Load capacitance* (pF)	16.5 typ.
Oscillation mode*	Funda-mental

Table 6 - Crystal Specification

*characteristics at 25°C ± 2°C

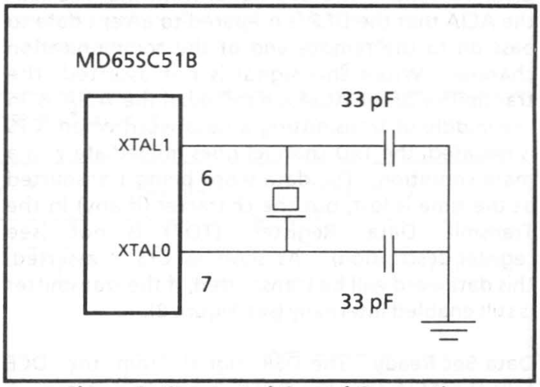


Figure 4. Suggested Crystal Connection

Status Register bit	Control Signal	Status Flag Set by	Status Flag Cleared by
0	PARITY ERROR③	Parity error detected.	Cleared Automatically after a read of the Receive Data Register and next error free reception of data.
1	FRAMING ERROR③	Framing error detected.	
2	OVERRUN③	Overrun has occurred.	
3	RECEIVE REGISTER	Register full.	Read Receive Data Register
4	TRANSMIT REGISTER	Register empty.	Write Transmit Data Register.
5	$\overline{DCD}$	Carrier not detected (a high on $\overline{DCD}$).④	Carrier detected (a low on $\overline{DCD}$).④
6	$\overline{DSR}$	Data set not ready (a high on $\overline{DSR}$).④	Data set ready (a low on $\overline{DSR}$).④
7	INTERRUPT	Interrupt has occurred. The $\overline{IRQ}$ signal to the microprocessor also goes low.	Read Status Register. This also clears the $\overline{IRQ}$ signal to the microprocessor.

Table 5 - Status Register Description

Notes ③ No interrupt is generated from these conditions.
④ These bits are not resetable and reflect the state of the input.

($\overline{DTR}$) outputs and the Clear To Send ($\overline{CTS}$), Data Set Ready (DSR) and Data Carrier Detect ($\overline{DCD}$) inputs. Note that the ACIA is viewed as the Data Termination Equipment (DTE) as opposed to the Data Communication Equipment (DCE) when referencing the RS-232C specification.

Request To Send . $\overline{RTS}$ is used to indicate to the DCE that it should assume the data channel transmit mode. The state of this output is controlled by bits 2 and 3 of the Command Register ($COMR_b2$ and $COMR_b3$, see Table 2). When it is high (not asserted, or in other words, "negated") the ACIA's transmitter is disabled.

Data Terminal Ready . The $\overline{DTR}$ signal indicates to the DCE that the ACIA is ready for communication. This output is asserted when $COMR_b0$ is set.

Clear To Send . The $\overline{CTS}$ signal from the DCE tells the ACIA that the DCE is prepared to accept data to pass on to the remote end of the communication channel. When this signal is not asserted, the transmitter of the ACIA is disabled. If the ACIA is in the middle of transmitting a data word when $\overline{CTS}$ is negated, the TxD channel goes immediately to a mark condition. The data word being transmitted at the time is lost, but the character (if any) in the Transmit Data Register (TDR) is not (see register description). As soon as $\overline{CTS}$ is asserted, this dataword will be transmitted, if the transmitter is still enabled internally (see Figure 8).

Data Set Ready. The $\overline{DSR}$ signal from the DCE tells the ACIA that the DCE is ready to operate. A transition on this pin can cause an interrupt (if interrupts are enabled) and the state of the pin is reflected in the state of SR_b6. Transitions that follow will not affect the status bit until after the µP has serviced the first interrupt (read the SR). At that point the SR will again reflect the current level of the $\overline{DSR}$ input, and an interrupt will occur again if it has changed. Transmitter and receiver operation is not affected by the level of this pin.

Data Carrier Detect. The $\overline{DCD}$ signal from the DCE indicates to the ACIA that the received signal is within specified limits. When $\overline{DCD}$ is not true, the receiver of the ACIA will be disabled and the data being shifted in at that moment is lost. A transition on this pin, like the $\overline{DSR}$ input, causes an interrupt. Subsequent transitions will not affect the status bit until the first interrupt is serviced. If the pin has changed since the first occurred and before it was serviced, another interrupt will occur. An even number of level changes on $\overline{DSR}$ and $\overline{DCD}$, before the first interrupt has been serviced, will not cause another interrupt. This is because the status bits will be at the same logic level that caused the original interrupt.

Register Description

The MD65SC51B contains seven registers, five that are visible to the µP. These registers are: the Transmit Shift Register (TSR, not available toµ P), the Receive Shift Register (RSR, not available to µP), the Transmit Data Register (TDR), the Receive Data Register (RDR), the Status Register (SR), the Command Register (COMR), and the Control Register (CR). One of the five latter registers is visible to the µP when the chip selects (CS0, CS1) are asserted and the E clock is true (high); the register chosen by the state of the register selects (RS0, RS1). The direction of µP bus transfer is determined by the state of the R/$\overline{W}$ signal (a high indicates a read of the contents of the register, a low a write to a register). When the SR is written to (the data written doesn't matter) a software reset will occur. For a comparison between the effect of a hardware reset and a software reset, see Table 1.

Transmit Data Register

The Transmit Data Register (TDR), in conjunction with the Transmit Shift Register, is used to place data on the transmit channel (TxD). If no word is being transmitted, a data word written to the TDR is immediately transferred into the TSR to be shifted out. A start bit precedes the data on the TxD channel; parity is added to the end of the word as needed (after the valid MSB is shifted out); and 1, 1.5, or 2 stop bits follow to end the transmitted information. If the ACIA is programmed to send a data word that is less than 8 bits in length (5, 6 or 7 bits), the extra bits in the data word are ignored.

While the TSR is occupied shifting out active data on to TxD (including the bit periods for the transmission of parity bits and stop bits), information written to TDR will be latched and held. When the last stop bit of the previous word is finished, the ACIA will transfer the data word in the TDR into the TSR and transmit it. If the TDR is written to more than once while information is being transmitted on TxD, the data word in TDR will be overwritten and retain the data associated with the last write.

If transmit interrupts are enabled, when the TDR is empty an interrupt will occur and SR_b4 will be set (SR_b4 will be set even if interrupts are disabled). This coincides with the beginning of the start bit for the data just transferred to the TSR. The interrupt must be serviced to be removed (by reading SR), but SR_b4 may only be cleared by a write to the TDR. If the interrupt is serviced but TDR is not written to,

another interrupt will occur at the next word boundary (word boundaries are referenced to the start of the last transmitted word, and occur every full word period after the end of that word. This timing is reset by a new transmission because, if TxD is idle the new word is transmitted immediately - see Figures 5 & 7.

Receive Data Register

Data on the receive channel (RxD) is stripped of the overhead bits (start, parity and stop) by the ACIA and shifted into the Receive Shift Register (RSR). When a full data word has been received (depending on the programmed length), the contents of the RSR are transferred into the Receive Data Register (RDR). If receive interrupts are

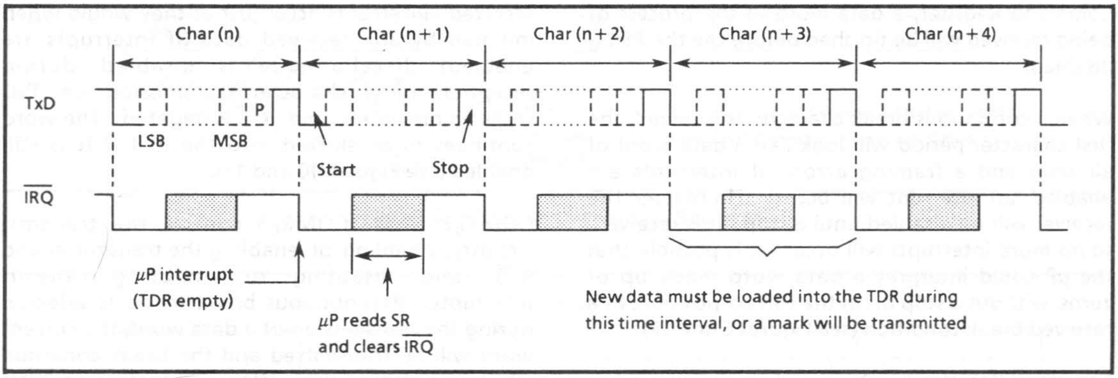


Figure 5. Continuous Data Transmit

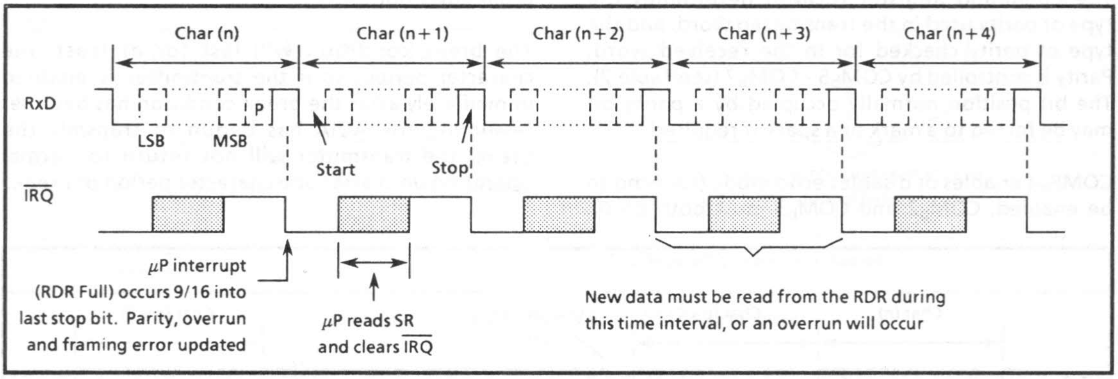


Figure 6. Continuous Data Receive

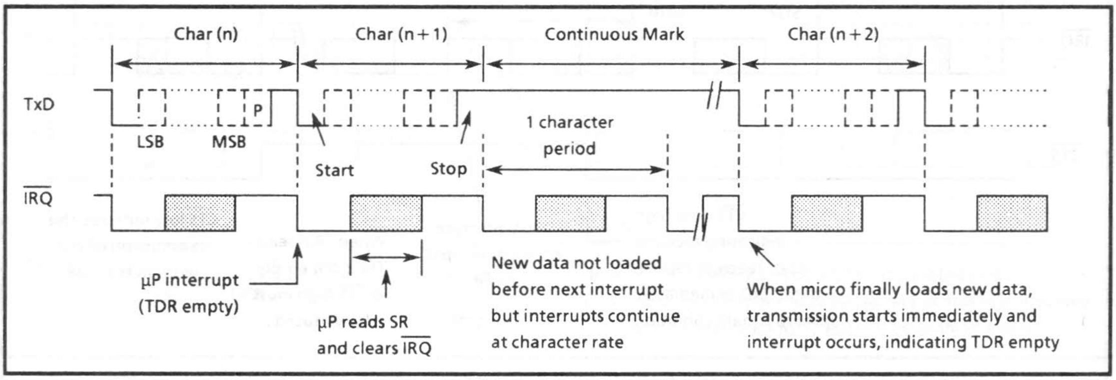


Figure 7. TDR not loaded by Processor

enabled, this transfer will cause an interrupt to occur and SR_b3 to be set (SR_b3 is set even when interrupts are disabled). The interrupt actually occurs about 9/16 through the last stop bit. As with the TDR, the interrupt is removed by reading SR and SR_b3 is cleared by reading the RDR.

If $\overline{DCD}$ is not asserted, the RSR is immediately disabled and any word being received at the time is lost. If the receive circuitry is disabled through the Command Register, a data word in the process of being received will be finished before the the RSR is disabled.

When a continuous break character is received, the first character period will look like a data word of all zeros and a framing error. If interrupts are enabled, an interrupt will occur. Thereafter the receiver will be disabled until a stop bit is received, so no more interrupts will occur. It is possible that the μP could interpret a data word made up of zeros, without a stop bit in the correct position, as a received break condition (see Figures 6 and 12).

Command Register

The Command Register (COMR) determines the type of parity used in the transmitted word, and the type of parity checked for in the received word. Parity is controlled by COM_b5 - COM_b7 (see Table 2). The bit position normally occupied by a parity bit may be forced to a mark or a space if required.

$COMR_b4$ enables or disables echo mode (for echo to be enabled, COM_b2 and COM_b3 must both be 0). When in echo mode, the ACIA's receive circuitry is still operational, but data written to the TDR will not be transmitted until echo mode is disabled and the transmitter is re-enabled. $\overline{RTS}$ is asserted in echo mode, even though it is not programmed to be active by $COMR_b3$ and $COMR_b2$.

When data is received on RxD (the receiver must be enabled internally and $\overline{DCD}$ true) it is transmitted 1/2 bit period after it has been received. Interrupts occur just as they would when initiated by any received data (If interrupts are enabled). If echo mode is disabled during reception of a character, transmission on TxD stops immediately and $\overline{RTS}$ is negated. The word continues to be shifted into the RSR if it is still enabled (see Figures 10 and 11).

$COMR_b2$ and $COMR_b3$ control the transmit circuitry, disabling or enabling the transmitter and $\overline{RTS}$, and disabling or enabling transmit interrupts. If continuous break mode is selected during the transmission of a data word, the current word will be transmitted and the break condition will begin immediately after. Transmit interrupts are automatically disabled during the transmit break condition.

The break condition will last for at least one character period, so if the transmitter is enabled immediately after the break condition has been set (assuming the ACIA has begun to transmit the break) the transmitter will not return to normal operation until after one character period of break.

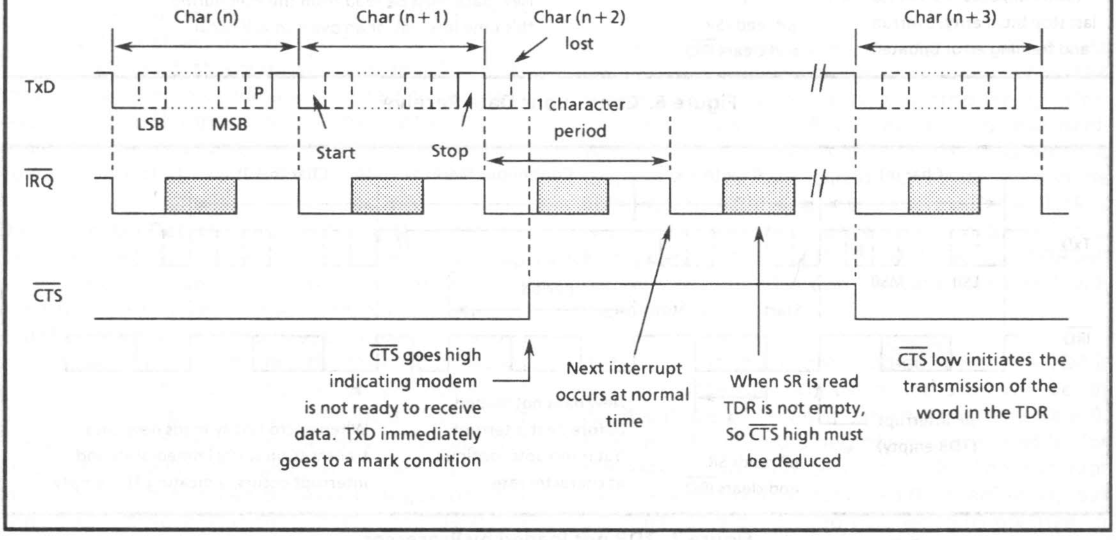


Figure 8. Effect of $\overline{CTS}$ on TxD

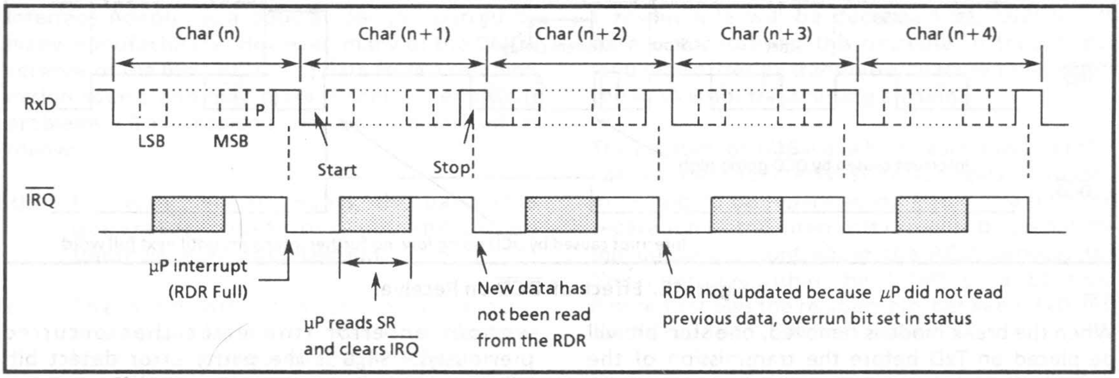


Figure 9. Effect of Overrun on Receiver

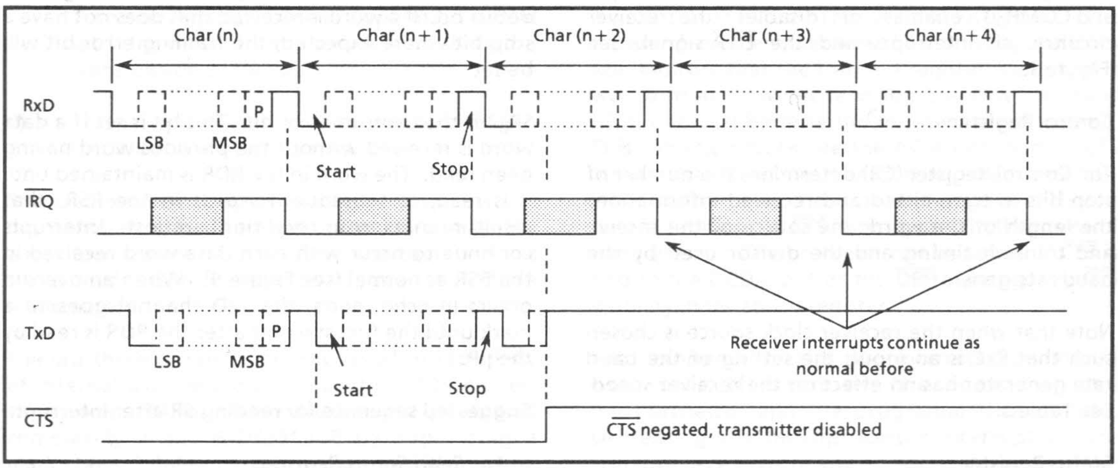


Figure10. Effect of $\overline{CTS}$ on Echo Mode operation

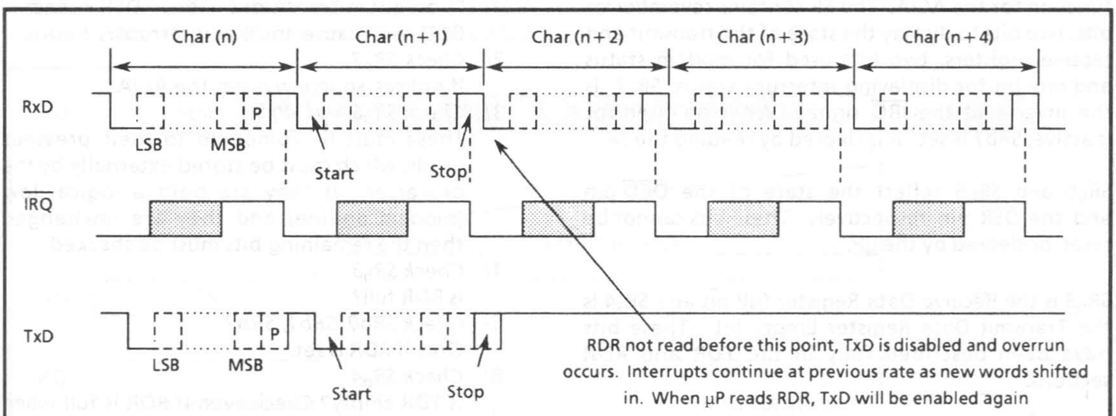


Figure 11. Overrun in Echo Mode

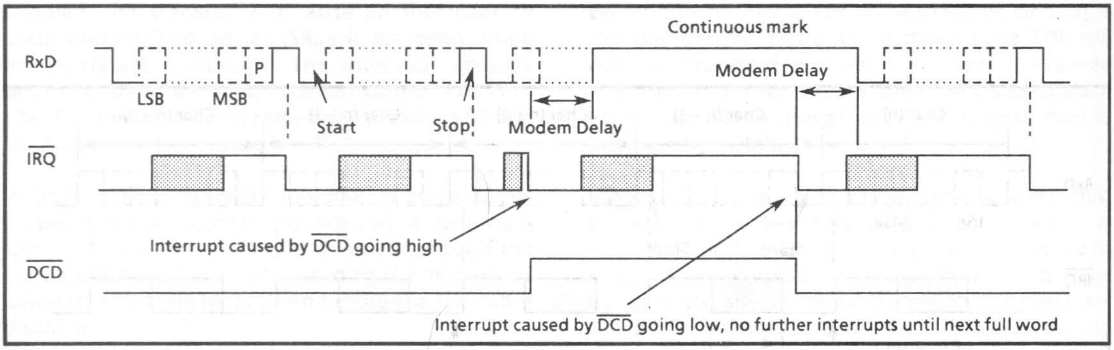


Figure12. Effect of $\overline{DCD}$ on Receiver

When the break mode is removed, one stop bit will be placed on TxD before the transmission of the next word.

$COMR_b1$ enables or disables receiver interrupts and $COMR_b0$ enables or disables the receiver circuitry, all interrupts and the $\overline{DTR}$ signal. See Figure 3.

Control Register

The Control Register (CR) determines the number of stop bits in transmitted and received information; the length of the word: the source of the receive and transmit timing and the divisor used by the baud rate generator.

Note that when the receiver clock source is chosen such that RxC is an input, the setting of the baud rate generator has no effect on the receiver speed. See Table 3.

Status Register

The Status Register (SR) performs a "housekeeping" function for the ACIA. The SR contains several error bits, two bits to display the state of the transmit and receive registers, two bits used for modem status and one bit for displaying interrupt status. SR_b7 is the inverse of the $\overline{IRQ}$ signal. When an interrupt is active, SRb7 is set. It is cleared by reading the SR,

SR_b5 and SR_b6 reflect the state of the $\overline{DCD}$ pin and the $\overline{DSR}$ pin respectively. These bits cannot be reset or cleared by the µP.

SR_b3 is the Receive Data Register full bit and SR_b4 is the Transmit Data Register Empty bit. These bits have been described fully in the TDR and RDR sections.

The three LSB bits in the SR are error bits, set when a specific error condition occurs. These bits may only be cleared if the RDR is read and a word is received without an error (the error that occurred previously). SR_b0 is the parity error detect bit. When this bit is set, it indicates that parity is enabled and the level of the parity bit received by the ACIA was incorrect. SR_b1 is the framing error detect bit. If a word is received that does not have a stop bit where expected, the framing error bit will be set.

SR_b2 is the overrun error bit. This bit is set if a data word is received without the previous word having been read. The word in the RDR is maintained until it is read, so subsequent words in the RSR, that result in an overrun condition, are lost. Interrupts continue to occur with each data word received in the RSR as normal (see Figure 9). When an overrun occurs in echo mode, the TxD channel goes to a mark until the first start bit after the RDR is read by the µP.

Suggested sequence for reading SR after interrupt:

1/ *Read Status Register.*
This operation automatically clears SR_b7 and negates the IRQ signal. Subsequent transitions on DSR and DCD will cause another interrupt.

2/ *Check SR_b7*
If not set, source was not the ACIA.

3/ *Check SR_b6 and SR_b5*
These must be compared to their previous levels, which must be stored externally by the processor. If they are both a logical low (modem on-line) and they are unchanged then the remaining bits must be checked.

4/ *Check SR_b3*
Is RDR full?

5/ *Check SRb0, SRb1, SRb2*
Only if RDR is set.

6/ *Check SR_b4*
Is TDR empty? Check even if RDR is full when in full duplex operation.

7/ If none of the above occurred, $\overline{CTS}$ must have been negated.

MD65SC51B ACIA Improvements

The MD65SC51B Asynchronous Communications Interface Adapter is a popular design, sourced by many manufacturers. However, many of the CMOS versions of the 6551 ACIA originate from a common design source and may present some intermittent problems. The problems may be summarized as follows:

a) In "noisy" environments, the baud rate generator could lock up, inhibiting transmission and/or reception.

b) The start bit of a character would occasionally be shorter than it should have been for a particular baud rate setting.

c) Information being transmitted could be overwritten by information meant for the Transmit Register. Correct operation would latch the new information while finishing the transmission of the old.

d) The parity bit would occasionally be set when it should have been cleared.

The first problem may occur when noise sets the programmable baud rate generator logic array into a disallowed state. The solution was to detect this state and upon detection, leave the state immediately.

The last three problems are the result of sensitivity of internal asynchronous signals to CMOS process variations. Mitel eliminated these problems completely in the MD65SC51B by appending a mark state, 1/16th of a bit period in width, to the last stop bit of each transmitted character. This extra mark time may affect device operation in instances where the total bandwidth of the ACIA transmit channel is used. In such a case, if the ACIA is set up to transmit characters that are for example, 10 bits in length (including start, stop and parity bits), the maximum throughput of the ACIA on the transmit side will be decreased by 0.625%. In normal applications, this decrease in throughput would be offset by transmitter inactive time, where the ACIA is not transmitting anything.

The addition of 1/16th of a bit to each character also causes two formerly simultaneous transmit interrupts to be separated by 1/16th of a bit. This separation of the interrupts can only be seen if the microprocessor controlling the ACIA services the first interrupt within the 1/16th of a bit time. Figure 13 shows the relationship between TxD, $\overline{\text{IRQ}}$ and the added 1/16th mark state.

The transmit interrupts are caused by the end of the stop bit of the last transmitted character and the falling edge of the start bit of the next character being transmitted. The second interrupt is a potential problem, because the status register does not indicate that the transmit register is empty if it was written to when servicing the first interrupt (this is logical because the register is not empty). This condition looks like the ACIA just had its $\overline{\text{CTS}}$ input negated while transmitting one character with another in the transmit register. This is only a problem if $\overline{\text{CTS}}$ is being used in flow control applications. The problem can be solved if $\overline{\text{CTS}}$ is tied to the $\overline{\text{DCD}}$ input or the $\overline{\text{DSR}}$ input, giving $\overline{\text{CTS}}$ visibility in the status register.

The occurrence of the two interrupt condition is obviously affected by the speed of the microprocessor and the programmed baud rate. Decreasing the microprocessor interrupt service routine execution speed or increasing the programmed baud rate of the ACIA decreases the chances of servicing the first interrupt within 1/16th of a bit.

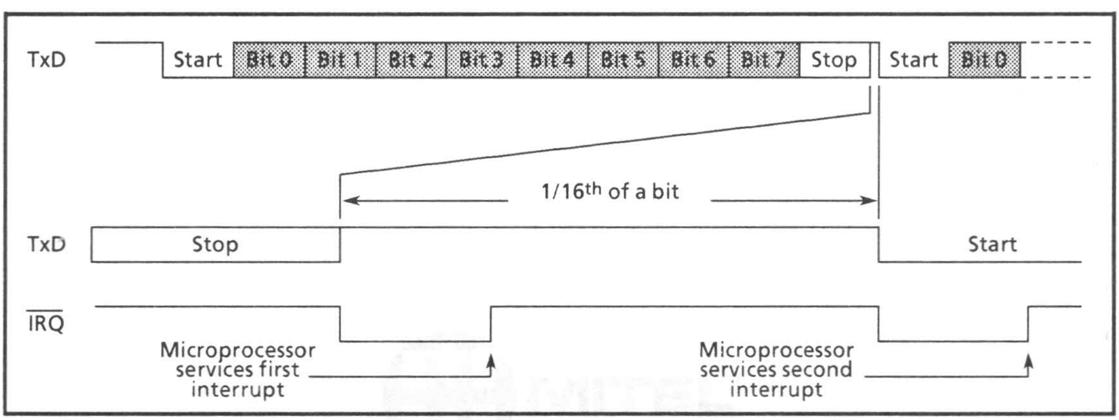


Figure 13 - Relationship between TxD and $\overline{\text{IRQ}}$

NOTES:

CUSTOM HYBRIDS

6

Custom SLIC

9161-002-122-NA ISSUE 1 September 1989

Features

- Total customized SLIC solution
- Compact package outline
- Low tooling costs
- Flexible design approach
- Few external components necessary

Applications

SLIC interface for:

- PABX's
- Key Systems
- Intercoms
- Central Office
- Channel Bank

Description

Mitel Semiconductor's thick film hybrid facility is dedicated to the manufacture of hybrids for the telecommunications industry. A major portion of the facility is for the manufacture of ASIMs (Applications Specific Integrated Modules).

ASIMs combine Mitel's applications expertise and design with manufacturing technologies to offer unique customer specific solutions.

Design experience in communications, combined with Mitel's VLSI and advanced interconnect technologies, result in integrated modules tailored for individual customer applications.

ASIMs offer significant systems cost reductions together with all the inherent advantages of modular design approach.

This data sheet is intended as a guide to Mitel's capabilities in SLIC design and manufacture. A menu of customer requirements is outlined within the following pages.

By the options detailed, please fill in all of the relevant information and requirements for your slic function. Upon receipt of the details, Mitel will be able to assess the feasibility and propose technical solutions tailored to your needs.

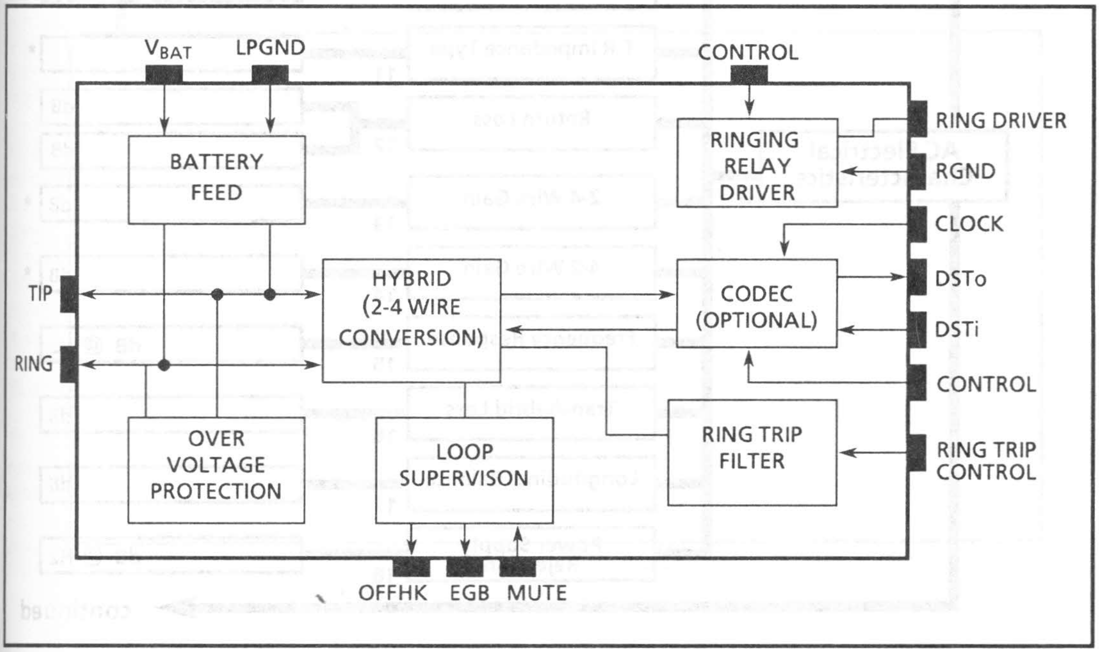
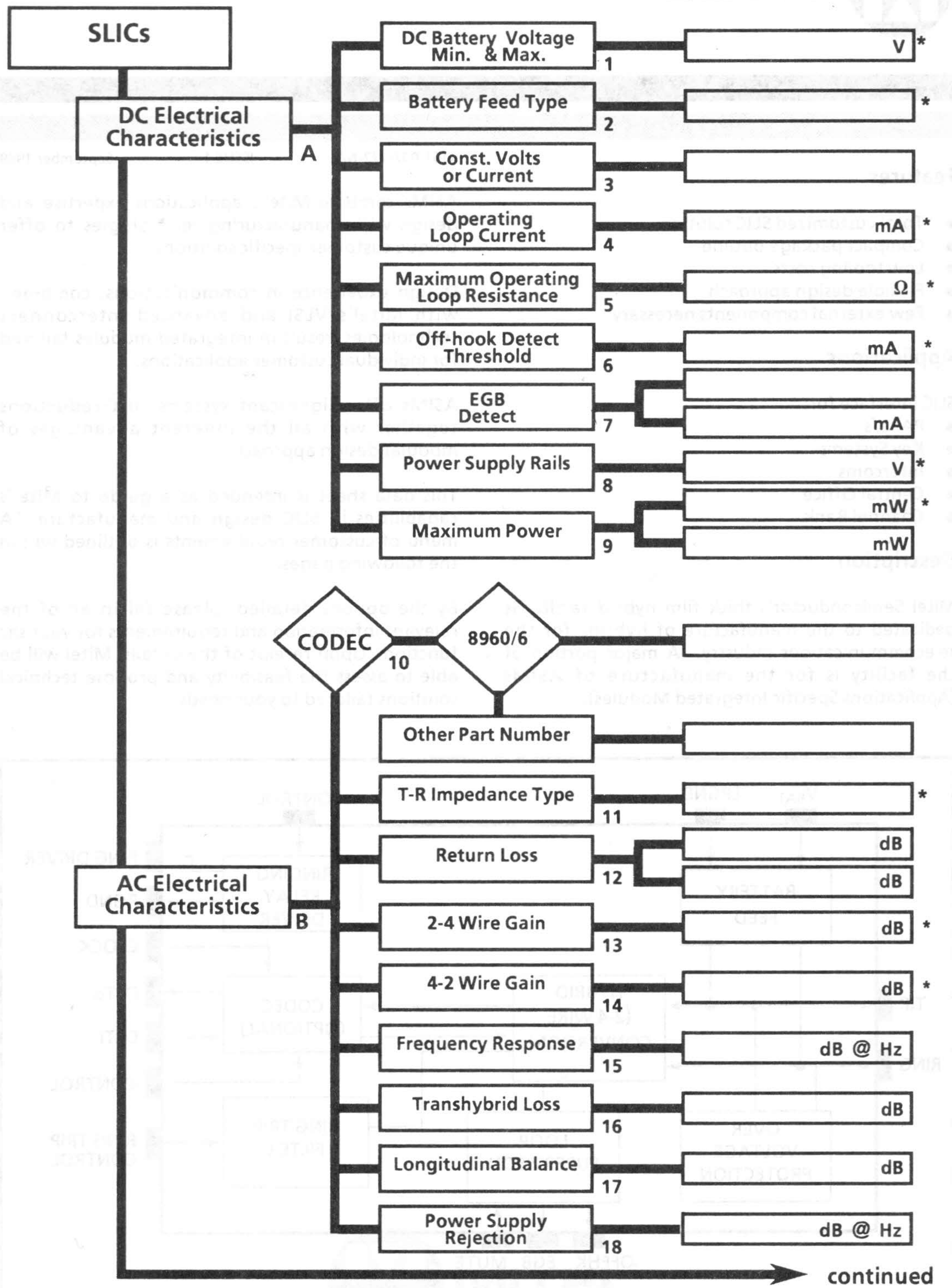
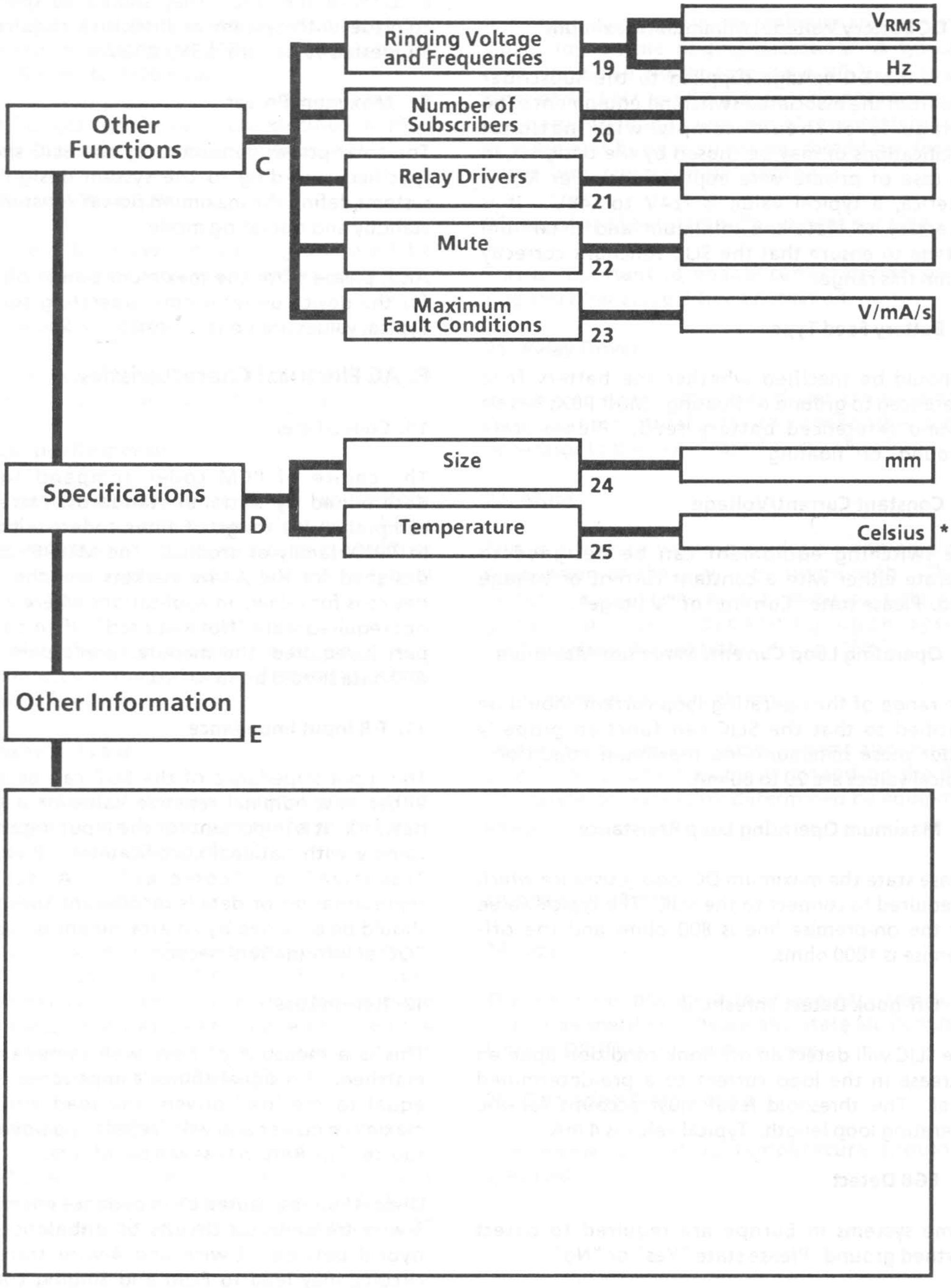


Figure 1. Functional Block Diagram


SLICs
DC Electrical Characteristics
A
DC Battery Voltage Min. & Max.
1
V *
Battery Feed Type
2
*
Const. Volts or Current
3
Operating Loop Current
4
mA *
Maximum Operating Loop Resistance
5
Ω *
Off-hook Detect Threshold
6
mA *
EGB Detect
7
mA
Power Supply Rails
8
V *
Maximum Power
9
mW *
mW
CODEC
10
8960/6
Other Part Number
AC Electrical Characteristics
B
T-R Impedance Type
11
*
Return Loss
12
dB
dB
2-4 Wire Gain
13
dB *
4-2 Wire Gain
14
dB *
Frequency Response
15
dB @ Hz
Transhybrid Loss
16
dB
Longitudinal Balance
17
dB
Power Supply Rejection
18
dB @ Hz
continued


Other Functions
C
Ringing Voltage and Frequencies
19
V_RMS
Hz
Number of Subscribers
20
Relay Drivers
21
Mute
22
Maximum Fault Conditions
23
V/mA/s
Specifications
D
Size
24
mm
Temperature
25
Celsius
*
Other Information
E

Functional Description

A. DC Electrical Characteristics

1. DC Battery Voltage: Minimum/Maximum

This is the DC voltage supplied to the subscriber loop from the associated switching equipment. The voltage level should comply with national specifications or may be chosen by the designer, in the case of private wire applications. For North America, a typical value is -24V to -48V. It is necessary to state the minimum and maximum voltage to ensure that the SLIC functions correctly within this range.

2. Battery Feed Type

It should be specified whether the battery feed referenced to ground or floating. Most PBXs have a ground referenced battery feed. Please state "ground" or "floating".

3. Constant Current/Voltage

The switching equipment can be designed to operate either with a constant current or voltage feed. Please state "Current" or "Voltage".

4. Operating Loop Current: Minimum/Maximum

The range of the operating loop current should be specified so that the SLIC can function properly under these minimum and maximum conditions. Typical values are 20 to 60 mA.

5. Maximum Operating Loop Resistance

Please state the maximum DC loop resistance which is required to connect to the SLIC. The typical value for the on-premise line is 800 ohms and the off-premise is 1800 ohms.

6. Off-hook Detect Threshold

The SLIC will detect an off-hook condition upon an increase in the loop current to a pre-determined level. This threshold level must account for the operating loop length. Typical value is 4 mA.

7. EGB Detect

Some systems in Europe are required to detect earthed ground. Please state "Yes" or "No".

The EGB (Earth Ground Button) detect threshold determines the difference in current flowing in the Tip Lead and Ring Lead indicating an activation of the Earth Ground Button. A typical value is 20 mA.

8. Power Supply Rails

These are required to supply voltage to the internal circuitry of the SLIC. They should be specified to coincide with system architecture requirements. Suggested values are ±5V, ±12V.

9. Maximum Power

The total power consumed by the SLIC should be specified according to the system design. Some systems define the maximum power consumption in standby and operating mode.

Also, please state the maximum power dissipation for the device under normal operating conditions. Typical values are up to 2 watts.

B. AC Electrical Characteristics

10. Codec/Filter

The choice of PCM codec companding law is determined by national standards. Mitel has a comprehensive range of filter codecs within their MT89XX family of product. The MT8965 has been designed for the A-law markets and the MT8960 device is for μ-law. In applications where a codec is not required state "Not Required". If an alternative part is required, the manufacturer's part number and data should be specified.

11. T-R Input Impedance

The input impedance of the SLIC can be specified either as a nominal resistive value or a complex network. It is important for the input impedance to comply with national specifications. Please state "resistive" or "complex". A schematic representation or details or relevant specifications should be provided by an attachment or within the "Other Information" section.

12. Return Loss

This is a measure of how well impedances are matched. If a signal source's impedance is exactly equal to the load driven, the load will absorb maximum power and will "reflect" no power to the source. The Return Loss will be infinite.

Discontinuities, caused by impedance mismatches in 2-wire transmission circuits or unbalances in the hybrid between 2-wire and 4-wire transmission circuits, may lead to Echo and Singing conditions. Return Loss may be more accurately defined in terms of Echo Return Loss (ERL) and Singing Return Loss (SRL) as follows:

Echo Return Loss (ERL) is a weighted average of the return loss values over the frequency range 500 Hz and 2500 Hz.

Singing Return Loss (SRL) is the lower value of the average return losses in the 200 Hz to 500 Hz band, and the 2500 Hz to 3200 Hz band.

ERL and SRL loss requirements are specified in dB as measured a specified reference impedance.

13. 2-Wire to 4-Wire Gain

This is the T-R to system gain and should be specified as part of the loss plan for the system.

14. 4-Wire to 2-Wire Gain

This is the system to T-R gain and should be considered in conjunction with the above.

15. Frequency Response

The operational bandwidth template required for the interface. For voice communications, this is generally the loss, in dB, from 300 Hz to 3400 Hz relative to the loss measured at 1000 Hz. A typical value is $\pm$0.1 dB.

The template should also detail any tone rejection. All tone rejections should be specified in the "other information" section.

16. Transhybrid Loss

This is a measure of the return signal power from the input pair to the output pair of the same 4-wire interface. A typical value is 20 dB.

17. Longitudinal Balance

This is a measure of the degree of balance to ground for both Tip and Ring circuits. Improper Longitudinal balance results in poor common mode rejection and produces a net voltage between the two sides, generating metallic noise audible to the user. A typical value is 53 dB at 3000 Hz.

18. Power Supply Rejection

This is the ability of the interface to prevent any ripple or noise on the power supply rails from entering the transmission path. Typical value is 30 dB.

C. Other Functions

19. Ringing Voltages and Frequencies

It is necessary to specify in minimum and maximum values for reliable ringing detection. A typical B type ringing in North America is 40 V_{RMS} to 150 V_{RMS} at 15.3 Hz to 68.0 Hz, superimposed on -56.5 V_{DC} battery voltage. Any special requirements such as pulse and burst suppression, should be detailed in the "other information" section.

20. Number of Subscriber Equipment per Line

This is important to enable correct design of the ring trip filter and off-hook detection.

21. Relay Drivers

In line card design, the relay driver can be used to turn on the external relay to connect the ringing generator to the line. State "Yes" or "No".

22. Mute

This is a feature which provides an analog signal suppression of the 2-wire to 4-wire path. This is useful in applications such as music on hold, tone generation, etc., depending upon system configuration. Please state "Yes" or "No".

23. Maximum Fault Condition

This is the maximum voltage, current and duration of a fault condition to be withstood by the SLIC. The conditions would be determined by equipment design.

D. Specifications

24. Size

The maximum physical size allowed for the device should be specified. Please also state SIL (Single-in-Line) or DIL (Dual-in-Line) package.

25. Operating Temperature

The normal operating temperature should be specified.

E. Other Information

Any other details which will assist Mitel in the proposal for the SLIC design should be stated here. An understanding of the system design and application is generally helpful.

***Please Note**

To assist in the assessment of your interface requirement the options labelled with an asterisk (*) **MUST** be answered. The other options are referenced to illustrate the capability of Mitel Custom SLICs. Many of the functions have default values which will be an inherent feature of the design.

Custom CO Trunk Interface

9161-002-123-NA ISSUE 1 September 1989

Features

- Total customized trunk interface solution
- Compact package outline
- Low tooling costs
- Flexible design approach
- Few external components necessary

Applications

Trunk interface for:

- PABXs
- Key Systems
- Intercoms
- Central Office
- Channel Bank

Description

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ASIMs combine Mitel's applications expertise and design with manufacturing technologies to offer unique customer specific solutions.

Design experience in communications, combined with Mitel's VLSI and advanced interconnect technologies result in integrated modules tailored for individual customer applications.

ASIMs offer significant systems cost reductions together with all the inherent advantages of a modular design approach.

This data sheet is intended as a guide to Mitel's capabilities in trunk interface design and manufacture. A menu of customer requirements is outlined within the following pages.

By the options detailed, please fill in all of the relevant information and requirements for your line interface function. Upon receipt of the details, Mitel will be able to assess the feasibility and propose technical solutions tailored to your needs.

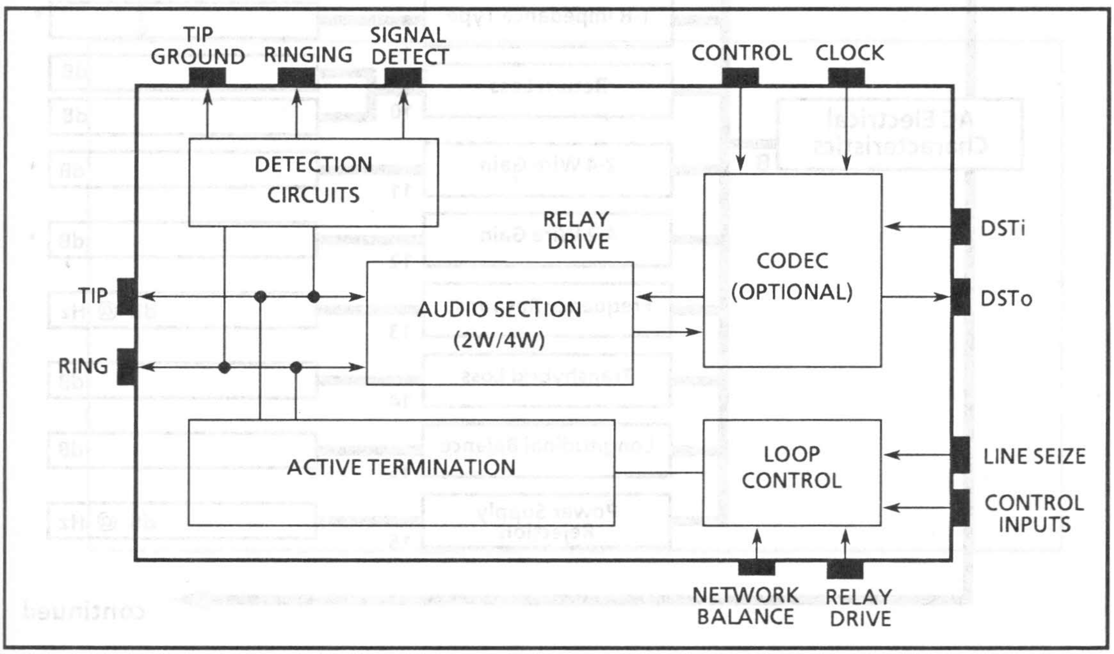
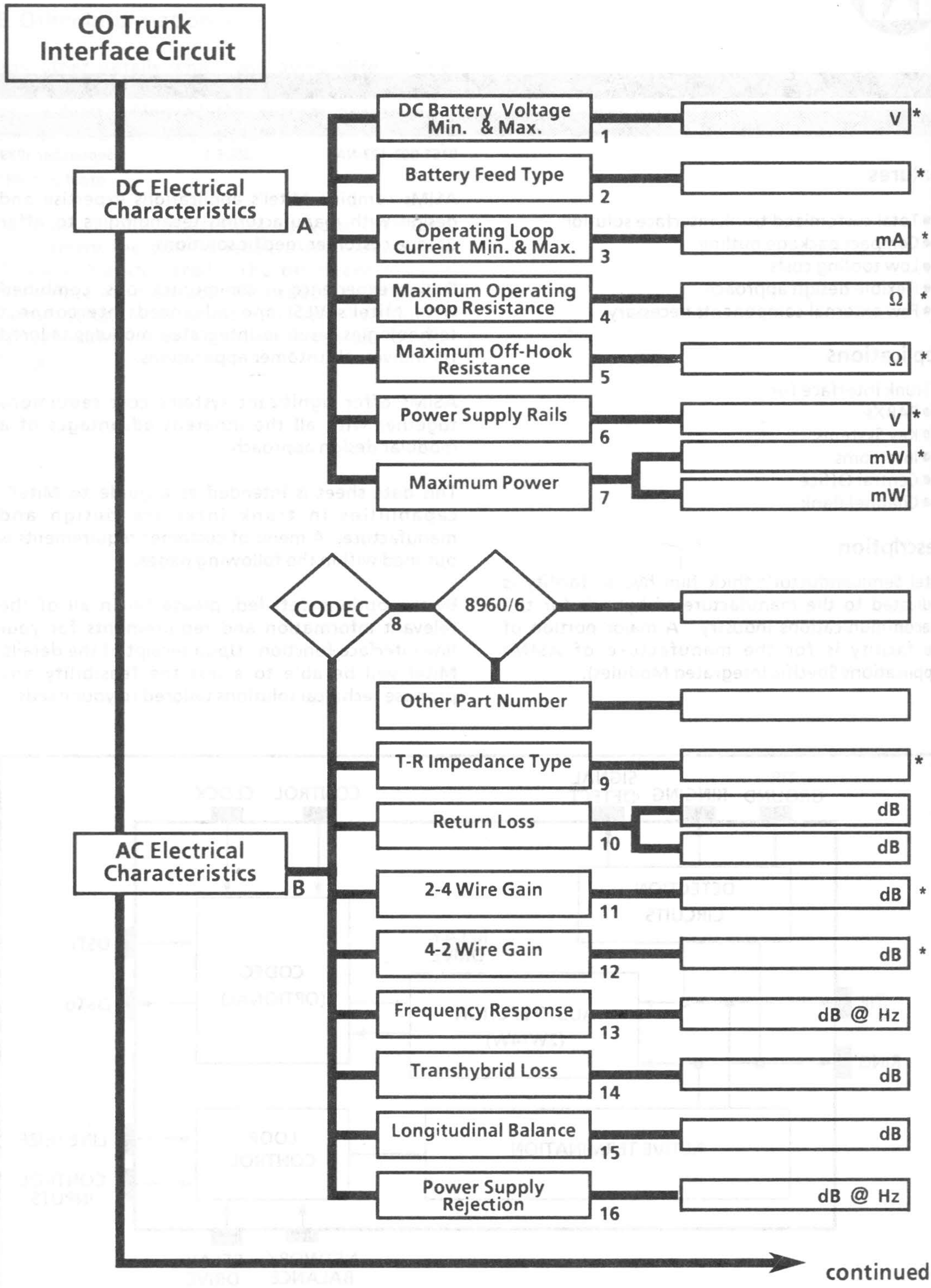
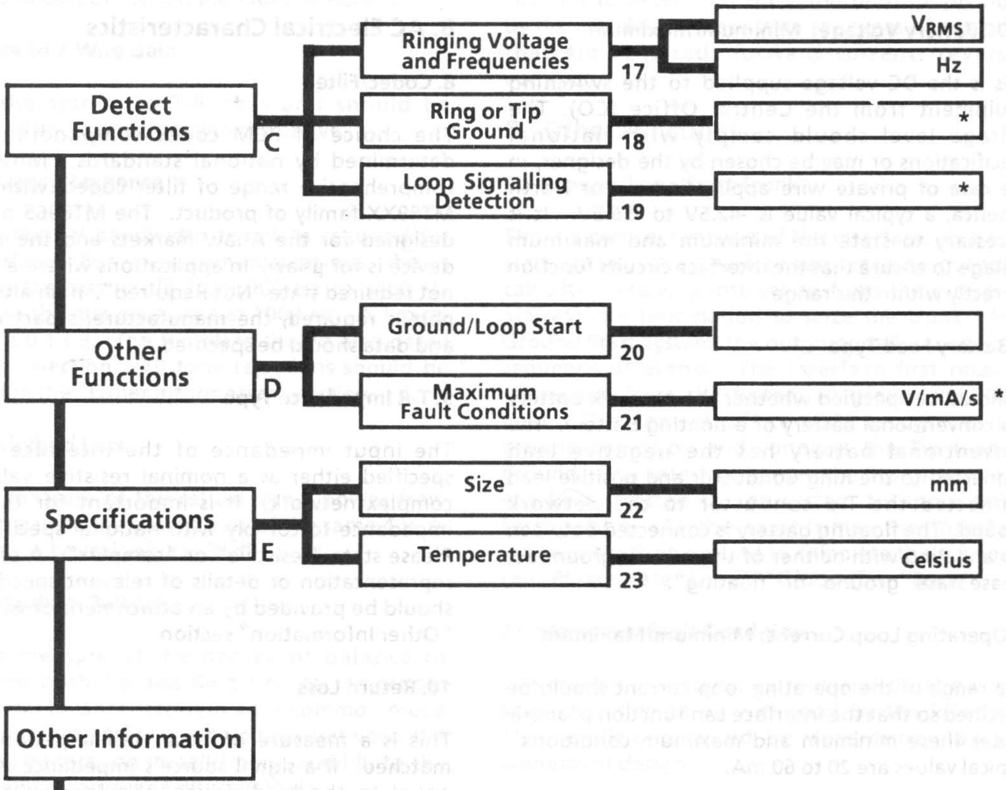


Figure 1 - Functional Block Diagram

6


CO Trunk Interface Circuit
DC Electrical Characteristics
A
DC Battery Voltage Min. & Max.
1
V *
Battery Feed Type
2
*
Operating Loop Current Min. & Max.
3
mA *
Maximum Operating Loop Resistance
4
Ω *
Maximum Off-Hook Resistance
5
Ω *
Power Supply Rails
6
V *
Maximum Power
7
mW *
mW
CODEC
8
8960/6
Other Part Number
T-R Impedance Type
9
*
AC Electrical Characteristics
B
Return Loss
10
dB
dB
2-4 Wire Gain
11
dB *
4-2 Wire Gain
12
dB *
Frequency Response
13
dB @ Hz
Transhybrid Loss
14
dB
Longitudinal Balance
15
dB
Power Supply Rejection
16
dB @ Hz

continued


Detect Functions
C
Ringing Voltage and Frequencies
17
VRMS
Hz
Ring or Tip Ground
18
*
Loop Signalling Detection
19
*
Other Functions
D
Ground/Loop Start
20
Maximum Fault Conditions
21
V/mA/s *
Specifications
E
Size
22
mm
Temperature
23
Celsius
Other Information

FUNCTIONAL DESCRIPTION

A. DC Electrical Characteristics

1. DC Battery Voltage: Minimum/Maximum

This is the DC voltage supplied to the switching equipment from the Central Office (CO). The voltage level should comply with national specifications or may be chosen by the designer, in the case of private wire applications. For North America, a typical value is -42.5V to -56.5V. It is necessary to state the minimum and maximum voltage to ensure that the interface circuits function correctly within this range.

2. Battery Feed Type

It should be specified whether the network battery is a conventional battery or a floating battery. The conventional battery has the negative lead connected to the Ring Conductor and positive lead connected the Tip conductor to the network ground. The floating battery is connected between Tip and Ring with neither of these leads grounded. Please state "ground" or "floating".

3. Operating Loop Current: Minimum/Maximum

The range of the operating loop current should be specified so that the interface can function properly under these minimum and maximum conditions. Typical values are 20 to 60 mA.

4. Maximum Operating Loop Resistance

Please state the maximum DC loop resistance which is required to connect to the interface. Typical value is 1800 ohms.

5. Maximum Off-Hook Resistance

This is the DC resistance to be presented to the trunk with the interface in an active (Off-hook) state. A typical value is 250 ohms.

6. Power Supply Rails

These are required to supply voltage to the internal circuitry of the interface. They should be specified to coincide with system architecture requirements. Suggested values are ±5V, ±12V.

7. Maximum Power

The total power consumed by the interface should be specified according to the system design. Some systems define the maximum power consumption in standby and operating mode.

Also, please state the maximum power dissipation for the device under normal conditions. Typical values are up to 2 watts.

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The choice of PCM codec companding law is determined by national standards. Mitel has a comprehensive range of filter codecs within their MT89XX family of product. The MT8965 has been designed for the A-law markets and the MT8960 device is for μ-law. In applications where a codec is not required state "Not Required". If an alternative part is required, the manufacturer's part number and data should be specified.

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The operational bandwidth template required for the interface. For voice communications, this is generally the loss, in dB from 300 Hz to 3400 Hz relative to the loss measured at 1000 Hz. A typical value is ± 0.1 dB. The template should also detail any tone rejection. All tone rejections should be specified in the "Other Information" section.

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This is a measure of the return signal power from the input pair to the output pair of the same 4-wire interface. A typical value is 20 dB.

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It is necessary to specify in minimum and maximum values for reliable ringing detection. A typical B type ringing in North America is 40 V_{RMS} to 150 V_{RMS} at 15.3 Hz to 68.0 Hz, superimposed on -56.5 V_{DC} battery voltage. Any special requirements such as pulse and burst suppression, should be detailed in the "Other Information" section.

18. Ring Ground/Tip Ground

If ground start signalling is used in the network it may be necessary to detect a ground condition on either, or both wires. Please state "Tip", "Ring" or "Both".

19. Loop Signalling Detection

If the network uses reverse-battery signalling, circuitry to detect this condition must be provided by the interface. Please state the types of detection that are required: forward current, reversed current.

D. Other Functions

20. Ground/Loop Start Trunk

This is a control function of the interface. In a loop start system, the interface can make an outgoing call after receiving instruction from the system to activate the termination to seize the trunk. In a Ground Start System, the outgoing call is made by a sequence of events. The interface first receives instruction from the system to ground the Ring lead. The Central Office (CO) recognizes the ground condition and connects the Tip lead to ground. The interface senses the Tip ground and will be instructed by the system to apply active termination. At the same time, the interface removes the Ring ground to complete the outgoing call. Please state "Loop", "Ground" or "Both".

21. Maximum Fault Condition

The maximum voltage, current and duration of a fault condition to be withstood by the interface. The conditions would be determined by the equipment design.

E. Specifications

22. Size

The maximum physical size allowed for the device should be specified. Please also state SIL (Single-in-Line) or DIL (Dual-in-Line) package.

23. Operating Temperature

The normal operating temperature should be specified.

F. Other Information

Any other details which will assist Mitel in the proposal of the interface design should be stated here. An understanding of the system design and application is generally helpful.

***Please Note**

To assist in the assessment of your interface requirement the options labelled with an asterisk (*) **MUST** be answered. The other options are referenced to

illustrate the capability of Mitel Custom CO Trunk Interface Circuits. Many of the functions have default values which will be an inherent feature of the design.

DIGITAL SWITCHES

7

MITEL®

MITEL®

Digital Switches

November 1989

Product Family

MT8980D	Digital Switch
MT8981D	Digital Switch
MT8982	Small Digital Switch
MT9080	SMX - Switch Matrix Module
MT9085	PAC - Parallel Access Circuit

Applications

- Digital PBX and KTS
- Central office switches/Digital Cross-Connects
- T1/CEPT multiplexor
- Digital loop carrier
- ST-BUS™ controller

Key Features

- Non-blocking digital switches
- Low power CMOS

MT8980/81
- 256/128 channel capacity (64 kb/s)
- 8 or 4 - 2 mb/s serial ST-BUS inputs/outputs
- Parallel microprocessor interface
- Patented messaging/broadcast capabilities

MT8982
- 64 channel capacity
- 2 serial input/output streams - 2mb/s max.
- Serial microprocessor interface
- Small size 16 pin package

MT9080
- Flexible building block for >500 line switches
- Data memory and connect memory modes
- Up to 16 bit wide parallel interface
- 16 MHz maximum clock rate
- Per channel single or double buffering

MT9085
- Serial-to-parallel, parallel-to-serial companion chip for SMX
- 32/16 serial inputs to 8 bit parallel interface
- 1024 channel capacity
- 2 mb/s, 4 mb/s serial rates

Description

The MT8980 provides simultaneous time switching capabilities for up to 256 64 kb/s channels. Data interface to the device is via 8 serial inputs and outputs operating at 2 mb/s. The MT8980 also provides microprocessor read/write access to individual ST-BUS channels, providing access to the control and status information on other Mitel ST-BUS components.

The MT8981 is identical to the MT8980, but provides the switching capabilities for four serial input and output streams (128 channels).

The MT8982 MiniDX is a low cost time switch providing simultaneous connections for up to 64 kb/s channels, via two serial inputs and output streams Control interface to the 16 pin device is via a serial microport.

The MT9080 Switch Matrix Module, SMX, is a flexible memory module suitable for construction of large digital switches. It can be configured as either a Connection Memory (CM) or a Data Memory (DM). Interface to the system is via a 16 bit wide parallel bus, with clock rates up to 16 MHz.

SMX is optimized for use in an applications larger than 500 lines. The basic configuration of two SMX's (1 DM, 1 CM) will handle switching of up to 1024 16 bit wide words in either a low delay single-buffered, or double-buffered configuration. Larger size matrices can be constructed with multiple MT9080s.

The MT9085 Parallel Access Circuit (PAC) provides an interface between 2/4 mb/s serial architectures and the parallel SMX interface. It provides either a serial-to-parallel or parallel-to-serial conversion between 32 serial streams and an 8-bit wide parallel bus. Additionally, it provides relevant SMX timing signals from ST-BUS timing signals.

Package Options

MT8980D	C,E	40 pin
	P	44 pin
MT8981D	C,E	40 pin
	P	44 pin
MT8982	C,E	16 pin
	S	16 pin
MT9080	P	84 pin
MT9085	P	68 pin

Note: C=CerDIP D=Sidebraze E=PDIP P=PLCC S=SOIC

NOTES:

PRIMARY RATE INTERFACES

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Primary Rate Interfaces

November 1989

Product Family

T1 (1.544 mb/s)

MH89750	T1 Framer & Interface
MT8976	T1/ESF Framer Circuit
MH89760	T1/ESF Framer & Interface
MH89761	T1 Transmit Equalizer

CEPT (2.048 mb/s)

MT8978	CEPT PCM 30 Framer Circuit
MH89780	CEPT PCM 30 Framer & Interface
MT8979	CEPT PCM 30/CRC-4 Framer
MH89790	CEPT PCM 30 CRC-4 Framer & Interface
MH89791	CEPT PCM 30 Transmit Equalizer

Applications

- T1/CEPT Multiplexor
- PBX
- Central Office Switches
- Digital Loop Carrier
- Primary Rate ISDN

Key Features

- Selectable framing/Line codes
  - MT8976/760 - D3/D4, ESF, SLC96, B8ZS ZCS
  - MT8979/790 - CRC4, HDB3, AMI
- 2 Frame elastic buffer with 32µs jitter buffer
- Insertion/Detection of A,B,C,D signalling bits with optional debounce
- Frame alignment signals, Tx and Rx
- Pin compatibility between T1 and CEPT devices
- Per channel, overall and remote loop around
- Performance monitoring capability

Description

The MT8976 provides a simple interface to a bidirectional DS1 link. All of the formatting and signalling insertion and detection is done by the device. Various programmable options in the device include: ESF, D3/D4, or SLC-96 mode, common channel or robbed bit signalling, zero code suppression, alarms and, local and remote loopback.

The MH89760 is a hybrid module which encompasses the MT8976, plus additional line interface and clock recovery circuitry. The MH89750 provides the same functionality, except for ESF.

The MT8979 is a CEPT digital trunk framing circuit operating at 2048 kb/s. It provides such features as: insertion and detection of synchronization patterns, optional cyclical redundancy check and far end error performance reporting, HDB3 decoding and optional coding, channel associated or common channel signalling, programmable digital attenuation and a 2 frame received elastic buffer.

The MT8978 is a first generation framer, providing similar features to the MT8979, with the exception of the CRC-4 error check.

The MH89790 is a hybrid module which encompasses the MT8979, plus additional line interface and clock recovery circuitry.

The MT8976 and MT8979, as well as the MH89760 and MH89790, are pin compatible with each other, providing considerable flexibility in addressing both North American and CEPT applications.

The MH89761 and MH89791 provide programmable, 120Ω transmit equalization for T1 and CEPT requirements respectively.

Package Options

MT8976	C,E	28 pin
	P	44 pin
MT8978	C	28 pin
MT8979	C,E	28 pin
	P	44 pin
MH89750	DIL Hybrid	40 pin
MH89760	DIL Hybrid	40 pin
MH89761	SIP Hybrid	20 pin
MH89780	DIL Hybrid	40 pin
MH89790	DIL Hybrid	40 pin
MH89791	SIP Hybrid	20 pin

Note: C=CerDIP D=Sidebraze E=PDIP P=PLCC S=SOIC

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NOTES:

BASIC RATE INTERFACES

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Basic Rate Interfaces

November 1990

Product Family

MT8910	Digital Subscriber Line Interface Circuit (DSLIC)
MT8930	Subscriber Network Interface Circuit (SNIC)
MT8971B/72B	MT8971 Digital Subscriber Interface Circuit (DSIC) MT8972 Digital Network Interface Circuit (DNIC)
MT8972A	Digital Network Interface Circuit
MH89726/728	MT8972 Loop Extender Circuits

Applications

- Digital subscriber lines
- PBX digital sets and line cards
- ISDN NT1/NT2
- ISDN LAN's
- Digital multiplexors and concentrators
- Pair gain/line doublers
- High speed, limited distance modems

Key Features

- Common ST-BUS system interface
- Low power CMOS, single 5V supply

MT8910

- Compatible with ISDN U-Interface standard
- Full duplex transmission over twisted pair
- High performance 2B1Q line code
- Over 5.5km loop range at 160kbps
- Full activation state machine

MT8930

- Compatible with ISDN S-Interface standard
- Full duplex 2B+D, 192kbps transmission
- Point-to-point, point-to-multipoint and star configuration
- Selectable NT/TE modes of operation
- On-chip HDLC
- No crystal required (on-chip PLL/VCO)

MT8972

- Full duplex, biphase line code transmission over single twisted pair
- Up to 5km at 80kbps and 4km at 160kbps
- ISDN compatible 2B+D channel format
- Selectable master/slave modes of operation
- Transparent modem capability
- Extended temperature range with MT8972B

MT8971B

- Similar features as the MT8972 but with shorter loop range - up to 3.0km at 80kbps and 160kbps

MH89726/728

- Extends transmission performance of the MT8972
- Over 6km at 80kbps on 24AWG twisted pair

Description

The MT8910 (DSLIC) provides the ISDN basic rate access at the U-Interface. Full duplex digital transmission at 160 kbit/s on single twisted pair is achieved using 2B1Q line code and echo cancellation technology. Complies with all loop length requirements as defined by ANSI T1.601 1988.

The MT8930 (SNIC) is an ISDN Basic Rate S and T interface conforming to CCITT spec I.430. Provides point-to-point and point-to-multipoint 2B + D transmission up to 1km over 2 twisted pairs. Includes a HDLC protocoller and Motorola/Intel compatible microport.

The MT8972 (DNIC) is a full duplex, bi-phase line code transceiver using echo-cancellation technique enabling up to 5km loop performance over ordinary twisted pair. Data rates of 80 and 160 kbit/s are supported in either transparent "modem" operation or ISDN compatible 2B+D transmission format. For even greater flexibility, the MT8972B offers extended temperature range operation and additional control features.

The MT8971 has features similar to the MT8972, but with loop performance of approximately 3.0 km over ordinary twisted pair. A perfect choice for applications with reduced line length demands but still requiring high quality, cost effective, error and noise immune transceiver functions.

The MH89726 (160kbps transmission) and MH89728 (80kbps transmission) are thick film hybrid circuits that may be used to extend the loop range capability of the MT8972. Over 6km can be achieved at 80kbps and over 5km at 160kbps.

Package Options

MT8910	C,D	28 pin
MT8930	C,E	28 pin
MT8971B	E	22 pin
MT8972A/72B	C,E	22 pin
MT8972A/72B	P	28 pin
MH89726/728	SIL Hybrid	10 pin

Note: C=CerDIP D=Sidebraze E=PDIP P=PLCC S=SOIC

NOTES:

RATE ADAPTORS

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Rate Adaptors

November 1990

Product Family

MH89500	R-Interface Module (RIM)
MT8950	Data Codec

Applications

- Featured telephone sets
- Integrated Voice/Data terminals
- Digital PBX/KTS
- Terminal adaptors

Key Features

- ST-BUS compatible
- Low power CMOS
- Single 5 Volt supply
- Loopback and test modes

MH89500

- Implements ISDN R-Interface function
- Rate adapts to basic rate B and D channels
- User selectable synchronous and asynchronous data rates
- V.24, X.20 and X.21 terminal interfaces
- Compatible with V.110 and ECMA 102 recommendations

MT8950

- Transparent coding and decoding of 0 to 8, 9.6 and 19.2 kbps data
- Rate adapts to 56kbps or 64kbps basic rate channel

Description

The MH89500 (RIM) implements the ISDN R-Interface terminal adaptor function. The RIM will rate adapt V.24 (RS-232 type), X.20 and X.21 terminal interfaces to basic rate B and D channels. It is compatible with V.110 and ECMA.102 recommendations and handles both asynchronous and synchronous data rates from 50 bps to 19.2 kbps.

The MT8950 data codec uses the transition encoded modulation technique to transparently encode/decode low speed data to and from a 56kbps or 64kbps channel. It can accept either asynchronous or synchronous data up to 8kbps, 9.6kbps and 19.2kbps. The MT8950 is a low cost solution to interface RS-232C type terminals to basic rate channel in, for example, digital PABX applications.

Package Options

MH89500	DIL Hybrid	40 pin
MT8950	C	24 pin

Note: C=CerDIP D=Sidebraze E=PDIP P=PLCC S=SOIC

NOTES:

CODEC AND DIGITAL PHONE COMPONENTS

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Product Summary

Codec and Digital Phone Components

November 1990

Product Family

MT8960/61/62/ 63/64/65/66/67	Integrated PCM Filter/Codec
MT8992/3B	Digital Telephone with HDLC (H-Phone)
MT8994/5B	Digital Telephone (D-Phone)

Applications

- Basic to fully featured telephone sets
- Integrated Voice/Data terminals
- Cellular radio sets
- Digital PBX/KTS
- Channel banks/multiplexers

Key Features

- ST-BUS compatible
- Low power CMOS
- Loopback and test modes

MT896X

- Integrated single chip transmit/receive filters and PCM Codec
- Meets AT&T D3/D4 and CCITT G.711 and G.712 specifications
  μLaw: MT8960/2/4/6
  A-Law: MT8961/3/5/7
- Digital Coding Options
  MT8964/5/6/7 CCITT Code
  MT8960/1/2/3 Alternative Code
- Programmable filter gains
- ± 5V supplies

MT899X

- Integrated single chip digital telephone circuit
- μ-Law and A-Law versions
- Programmable receive gain
- DTMF/tone generator and tone ringer
- Speakerphone operation
- On-chip transducer interfaces
- X.25 Level 2 HDLC formatting (MT8992/3B only)
- Single 5V supply

Description

The MT896X family consists of A-Law and μ-Law integrated single chip filter/codecs. All are fully compliant with D3/D4 and G.711/712 specifications and offer independently accessible filters with programmable gain adjustments. Up to six uncommitted scan/drive ports are available to simplify system design.

The MT8994/5B (D-Phone) is a highly integrated digital phone IC which combine either an A-Law or μ-Law filter/codec with all basic telephony functions and interfaces to permit the design of a fully featured digital telephone using a minimum of components. To simplify the set design, speakerphone operation, DTMF/tone and ringing generations, and programmable gain control are all included on chip as is a Motorola/Intel compatible microprocessor port. It is also easily interfaceable to any of Mitel's basic rate transceivers (DNIC, DSLIC and SNIC) through the ST-BUS to offer 2B + D connectivity. The D-Phone operates on only a single 5 Volt supply and its low power consumption provides the set designer the option of line power feeding.

The MT8992/3B (H-Phone) is a further enhancement of the D-Phone. In addition to all the features of the MT8994/5B, the H-Phone includes a fully integrated X.25 HDLC data formatter. Digital set design has never been simpler!

Package Options

MT8960/1	E	18 pin
MT8964/5	C,E	18 Pin
MT8962/3	E	20 pin
MT8962/3/6/7	S	20 pin
MT8992/3/4/5B	C	40 pin

Note: C=CerDIP D=Sidebraze E=PDIP P=PLCC S=SOIC

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COMMON CONTROL PRODUCTS

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Product Summary
Common Control Products

November 1990

Product Family

MT8920/ MT8920-1	ST-BUS Parallel Access Circuit
MT8940	T1/CEPT Digital Trunk PLL
MT8941	Advanced T1/CEPT Digital Trunk PLL
MT8952B	HDLC Protocol Converter

Applications

- T1/CEPT multiplexor
- PBX
- Central office
- Digital loop carrier
- ISDN

Key Features

MT8920
- High speed parallel access to ST-BUS
- Access time: 180ns - MT8920
  120ns - MT8920-1
- Flexible interrupts

MT8940
- Supplies 1.544 and 2.048 MHz clock phase-locked to an 8 kHz reference signal

MT8941
- Supplies 1.544, 2.048 and 4.096 MHz clocks phase-locked to an 8 kHz reference signal
- Pin compatible to MT8940
- Typical output jitter 0.07UI from 2 Hz to 40 kHz

MT8942
- Provides 512 kHz, 1.544 MHz, 2.048 MHz, 4.096 MHz and 8.192 MHz clocks phase-locked to an 8 kHz reference signal
- Selectable clock and frame pulse output ST-BUS or GCI mode
- Typical output jitter 0.04 UI from 2 Hz to 40 kHz

MT8952
- Formats as per X.25 level-2 standard
- Send and receive 19 byte FIFO
- ST-BUS and Motorola microprocessor interface

Description

The MT8920 provides a simple interface between Mitel's ST-BUS and parallel system environments.

It can be used to provide parallel data interfaces to various Mitel basic and primary rate components. Additionally, the MT8920 can be used as a parallel control interface to the MT8976/79 instead of using an MT8980 digital switch.

The MT8940 is a dual digital phase-locked loop providing the timing and synchronization signals for the T1 or CEPT transmission links and the ST-BUS. The first PLL provides the T1 clock (1.544 MHz) synchronized to the input frame pulse at 8 kHz. The timing signals for the CEPT transmission link or the ST-BUS are provided by the second PLL locked to an internal or an external 8 kHz reference signal.

The MT8941 is an advanced T1/CEPT digital trunk phase-locked loop that is a pin compatible variant of the MT8940 featuring enhanced jitter performance. The device also provides timing and synchronization signals for T1 or CEPT transmission links and the ST-BUS, all locked to an 8 kHz reference signal.

The MT8952 HDLC Protocol Controller frames and formats data packets according to X.25. This single channel device has a 19 byte FIFO and provides a parallel access to the ISDN D channel, or any other applications requiring HDLC functionality.

Package Options

MT8920/-1	C,E,P	28 pin
MT8940	C, E	24 pin
MT8941	E, P	24, 28 pin
MT8952B	C,E,P	28 pin

Note: C=CerDIP D=Sidebraze E=PDIP P=PLCC S=SOIC

NOTES:

SOFTWARE

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Software

Product Family

MS6000 MS6050	IES ISDN EXPRESS™ Evaluation Software
MS6010 MS6060	ISDN EXPRESS LAPD
MS6020 MS6070	ISDN EXPRESS Call Control

Applications

- ISDN Voice and Data Workstations
- ISDN application software development platform
- ISDN protocol monitoring
- ISDN protocol conversion

Key Features

- Implementation of data link entity as defined by CCITT Q.921
- Written in Kernighan & Ritchie C programming language
- Conformance Testers
- Test Drivers
- Device Drivers
- ISDN Workstation Demonstration
- Demonstrated on Basic Rate and Primary Rate ISDN EXPRESS products
- Operating System Independence

Description

MS6000/MS6050 is the object and source code for the ISDN EXPRESS Evaluation System. An application for this software is test development using the development product hardware.

MS6010/MS6060 Mitel's ISDN EXPRESS LAPD is an ISDN Software Development Tool Kit for Q.921 applications. It is designed to make the implementation of ISDN applications D-Channel processing requirements quick and easy.

MS6020/MS6070 Mitel's ISDN EXPRESS Call Control is an ISDN Development Tool Kit implementing Q.931. It supports protocol control and call control for AT & T and Northern Telecom switches; additional switches will be added.

The ISDN EXPRESS Call Control, LAPD, Physical Entities and Card provide users most of the building blocks for an ISDN system. All that is required is the environment and the application.

Ordering Information

MS6000	IES Object Code
MS6010	ISDN EXPRESS LAPD Object Code
MS6010-EV1.0	ISDN EXPRESS LAPD Evaluation Package
MS6020	ISDN EXPRESS Call Control Object Code
MS6020-EV1.0	ISDN EXPRESS Call Control Evaluation Package
MS6050	IES Source Code
MS6060	ISDN EXPRESS LAPD Source Code
MS6070	ISDN EXPRESS Call Control Source Code

NOTES:

DEVELOPMENT/OEM PRODUCTS

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Development/OEM Products

November 1990

Product Family

MB89000C	The ISDN EXPRESS™ Card
MB89010	ISDN EXPRESS DSLIC Card
MB89050	ISDN EXPRESS RIM Card
MB60XX	The ISDN EXPRESS Ancilliary Components

Applications

- ISDN component evaluation
- ISDN system emulator
- Communications Interface for voice processing systems
- Hardware/Software development system
- Test system

Key Features

- Component evaluation and Hardware/ Software development system
- ISDN system emulation
- Compatible with Multi-Vendor Integration Protocol (MVIP™) PC Interconnection Standard
- IBM PC/XT/AT/386 plug in cards support basic rate, primary rate and support components
- Eases familiarization with standard interfaces
- Menu driven software with full size display window for each component
- Help facility for all major system functions and component registers

Description

MB89000 The ISDN EXPRESS Card is an evaluation platform for a broad range of ISDN components. These include: ISDN EXPRESS LAPD Software, T-1, CEPT, SNIC, DNIC, Digital Phone, Digital Switch, HDLC and DPLL. The ISDN EXPRESS Card has an MVIP compatible interface.

MB89010 The ISDN EXPRESS DSLIC Card is a PC Card that operates as a stand alone card or in conjunction with other ISDN EXPRESS Cards. It provides an evaluation platform for the H-Phone, Digital Switch and the DSLIC which is the "U"-interface device. The MB89010 is MVIP compatible.

MB89050 The ISDN EXPRESS RIM Card operates in conjunction with The ISDN EXPRESS Card. It provides an evaluation platform for the RIM which is the "R"-interface device. The MB89050 is MVIP compatible.

MB60XX ISDN EXPRESS Ancilliary Components are used to assist in evaluating and designing with Mitel products. The Ancilliary Components include handset, speakerphone enclosure, and a variety of transformers, crystals and inductors.

Ordering Information

MB89000C	The ISDN EXPRESS Card
MB89010	ISDN EXPRESS DSLIC Card
MB89050	ISDN EXPRESS RIM Card
MB6000	ISDN EXPRESS Speakerphone
MB6001	ISDN EXPRESS Handset
MB6010	T1/MH89760 Magnetics Kit
MB6012	DNIC Accessory Kit
MB6013	MT8940 Crystal Oscillator Kit
MB6014	RIM Crystal Kit
MB6016	75Ω CEPT/MH89790 Magnetics Kit
MB6017	120Ω CEPT/MH89790 Magnetics Kit
MB6022	MT8941 Crystal Oscillator Kit
MB6024	DSLIC Accessory Kit (Low Inductance)

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APPLICATION NOTES

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Application Note **MSAN-101**

Applications of the MT8804A 8 X 4 Analog Switch Array

ISSUE 1 August 1982

Contents

Introduction

The constant trend in electronic design is towards circuits which minimize power and space requirements while improving on the performance characteristics of the predecessors. The field of analog switching is no exception to this design strategy. The Mitel MT8804A CMOS 8 x 4 Analog Switch Array is a micropower device which replaces several CMOS MSI packages and meets the stringent specifications required in analog switching systems. The 8 x 4 array configuration and minimal interchannel crosstalk make the MT8804A ideal for crosspoint switching applications. This application note provides both functional and parametric details of the device that would normally be required in designing the MT8804A into such systems. A series of application circuits and descriptions is presented to further illustrate the use and versatility of the MT8804A in communications and other more general areas.

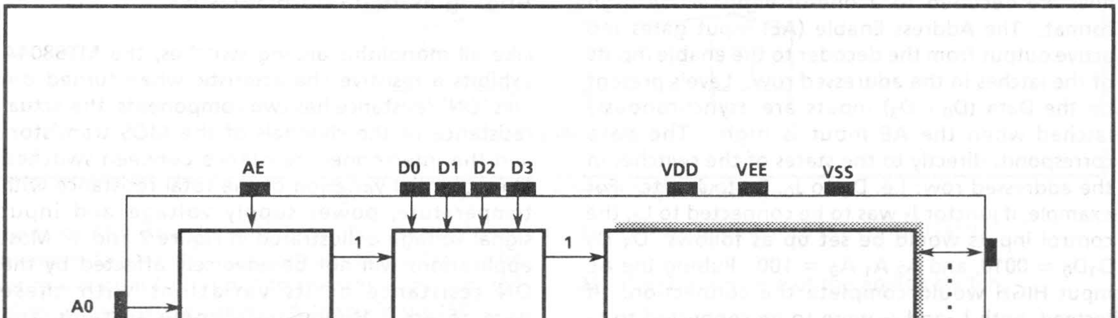


Fig. 1 - Functional Block Diagram

The MT8804A in Detail

Configuration and Control

The 32 analog switches in the MT8804A are configured in an 8 x 4 array as shown in Figure 1. The eight switches in each column are connected to an input/output Junctor (J_0 - J_3), and similarly, the four switches of each row are connected to an input/output Line (L_0 - L_7). Each crosspoint switch provides either isolation or transmission between its associated line and junctor. The states of the switches are controlled by a set of 32 latches arranged in an 8 x 4 array corresponding to the analog switch matrix. A logical HIGH stored in a latch turns the corresponding switch ON, while a LOW level turns the switch OFF. Data is asynchronously written into the control latches whenever the Address Enable (AE) input is HIGH. The latch outputs are directly connected to the control inputs of the analog switches. This direct interconnection results in a "continuous read" of the control memory (latches) by the analog switches.

Writing data into the control memory is done the same as in a standard random access memory. However, since no read control signals are required, the control store can uniquely be treated as a write-only-memory. The eight rows are selected by the three Address (A_0 - A_2) inputs. The signals on these lines are decoded to a one-of-eight active high format. The Address Enable (AE) input gates the active output from the decoder to the enable inputs of the latches in the addressed row. Levels present on the Data (D_0 - D_3) inputs are asynchronously latched when the AE input is high. The data corresponds directly to the states of the switches in the addressed row; i.e. D_0 to J_0, D_1 to J_1, etc. For example, if junctor J_1 was to be connected to L_4, the control inputs would be set up as follows: $D_3\ D_2\ D_1 D_0 = 0010$, and $A_2\ A_1\ A_0 = 100$. Pulsing the AE input HIGH would complete the connection. If instead, both J_1 and J_3 were to be connected to L_4 then the data inputs would be set to $D_3\ D_2\ D_1\ D_0 =$ 1010 and all else would remain the same. Similar connections can be programmed for each of the eight lines (L_0 - L_7). All of the latches in the control memory are asynchronously reset whenever the Master Reset (MR) input is HIGH. This results in all analog switches being turned OFF, isolating all junctors from all lines.

Power Supply Considerations

The MT8804A is equipped with on-chip logic level converters to simplify the interface to logic circuits in an analog switching system. The control inputs of the device are driven from signals between V_{DD} and V_{SS}. All of the control inputs are active HIGH with V_{DD} being a logical HIGH level and V_{SS} a logical LOW. The analog or digital signals switched through the array are allowed to swing between V_{DD} and V_{EE}.

The power supply input voltages are defined as follows:

$5V \leq V_{DD}\ V_{SS} \leq 13V$ Digital
$5V \leq V_{DD}\ V_{EE} \leq 13V$ Analog
$0V \leq V_{SS}\ V_{EE} \leq 8V$ Level Converters

These voltages define the operating power supply ranges of the digital and analog inputs and the logic level converters. While the analog and digital power supplies have identical limits the levels may be different in a given application. For example, a valid power supply configuration is as follows:

$V_{DD} = +5V$, $V_{SS} = 0V$ and $V_{EE} = -6V$. The control inputs are thus driven from a 5V CMOS logic system while the signals on the lines and junctors can swing from +5V to -6V. Caution must be used to meet all three power supply constraints when deciding upon a power supply configuration. The following is an example of invalid power supply voltages: $V_{DD} = +5V$, $V_{SS} = 0V$, and $V_{EE} = -12V$. In this case, $V_{DD} - V_{EE} = 17V$ which exceeds the analog power supply range.

Analog Switch Characteristics

Like all monolithic analog switches, the MT8804A exhibits a resistive characteristic when turned on. This 'ON' resistance has two components, the actual resistance of the channels of the MOS transistors and the interconnect resistance between switches. The potential variation of the total resistance with temperature, power supply voltage and input signal voltage is illustrated in Figure 2 and 3. Most applications will not be adversely affected by the ON resistance or its variations with these parameters. However in some systems and applications with more stringent specifications, special considerations may be required. In cases such as driving through the MT8804A into low impedance loads, or using the device in a gain control circuit, it becomes necessary to consider the switch resistance in design equations.

Timing Measurements

Timing measurements such as propagation delays, set up and hold times, etc. on the control inputs of the MT8804A cannot be made directly as digitial outputs are not available. For this reason, these measurements are made indirectly by observing the effects of changes in the control memory on the

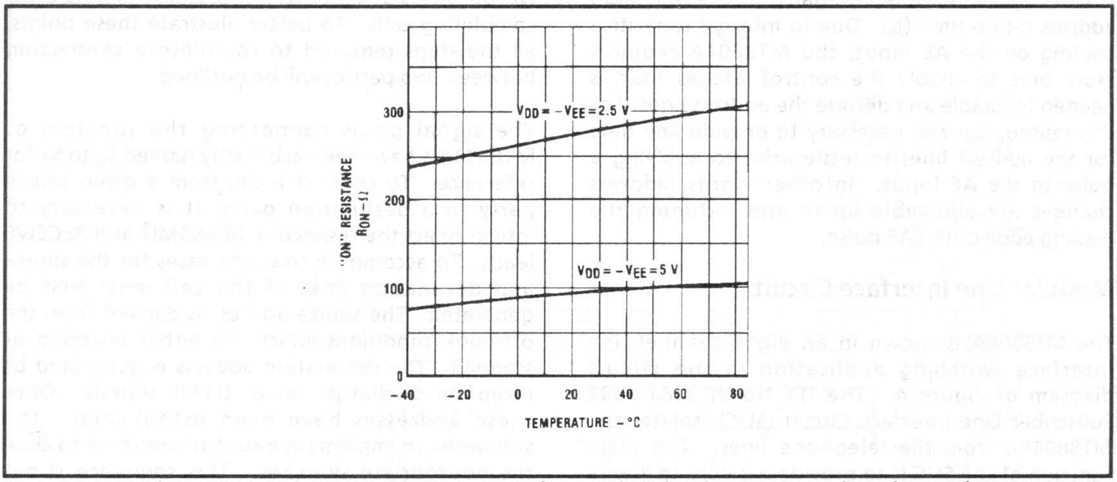


Fig. 2 - On Resistance vs Temperature (Input Signal Voltage = Supply Voltage/2)

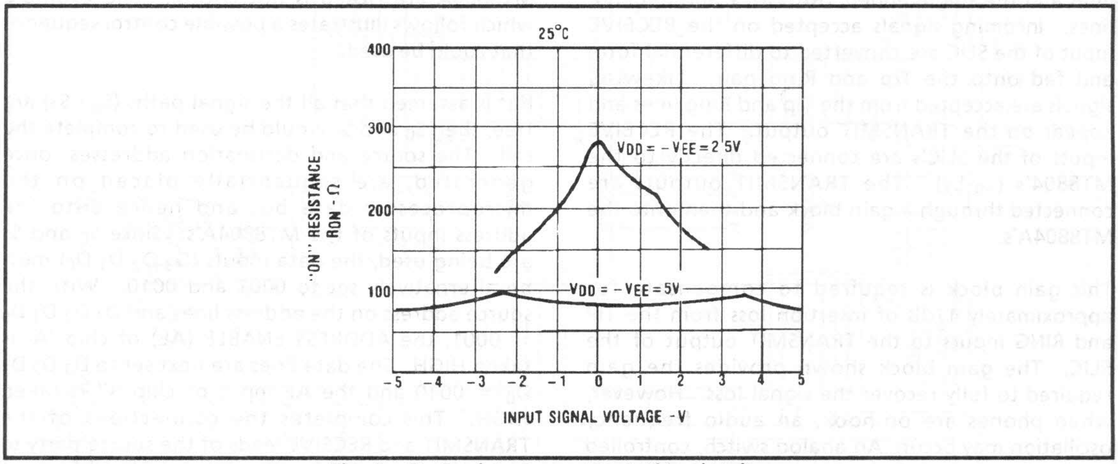


Fig. 3 - On Resistance vs Input Signal Voltage

states of the analog switches. For example, to measure t_{PAE}, the propagation delay from the address enable (AE) input to the signal output, the following steps are taken. A load circuit (50pF in parallel with 10K) is connected from a given junctor to ground (V_{SS}). One of the lines (L_0 - L_7) is connected to V_{DD}. With all switches initially OFF, the control inputs are set up to connect the load circuit to V_{DD} through the appropriate switch. The AE input is pulsed HIGH and the propagation delay time is measured from the 50% voltage point of the resulting signal across the load. In both cases, time is measured from the leading edge of the signal. The actual time measured has three components.

1) The write time into the control latch
2) The turn on time of the analog switch
3) The propagation time through the channel of the switch

In digital switching applications of the MT8804A, it is this total time that is of concern. In general, however, the minimum time needed to write data into the latches is required. This is represented by the first of the three components listed above and is by far, the longest of the three. Therefore, basing system design on the actual measurements of total time will add a small safety margin without sacrificing significant device performance.

A special note is made in regards to the minimum address set up time (t_s). Due to internal capacitive loading on the AE input, the MT8804A requires more time to enable the control latches than is needed to enable and decode the address lines. For this reason, it is not necessary to provide any time for the address lines to settle prior to applying a pulse to the AE input. In other words, address changes are allowable up to and including the leading edge of the AE pulse.

Modular Line Interface Circuit

The MT8804A is shown in an eight channel line interface switching application in the circuit diagram of Figure 4. The ITT North 3081/3082 Subscriber Line Interface Circuit (SLIC) isolates the MT8804A's from the telephone lines. The main function of the SLIC is to provide a 2-wire to 4-wire conversion between the balanced TIP and RING lines and the single ended TRANSMIT and RECEIVE lines. Incoming signals accepted on the RECEIVE input of the SLIC are converted to differential form and fed onto the Tip and Ring pair. Likewise, signals are accepted from the Tip and Ring lines and appear on the TRANSMIT output. The RECEIVE inputs of the SLIC's are connected directly to the MT8804's (L_0-L_7). The TRANSMIT outputs are connected through a gain block and then onto the MT8804A's.

This gain block is required to compensate for approximately 17dB of insertion loss from the TIP and RING inputs to the TRANSMIT output of the SLIC. The gain block shown provides the gain required to fully recover the signal loss. However, when phones are on-hook, an audio frequency oscillation may occur. An analog switch, controlled by the Switchhook Detection output of the SLIC, reduces the ac gain to unity preventing this oscillation. A small capacitor placed around the feed back loop eliminates spurious high frequency oscillation.

Network Control

In general, to complete a telephone call with this system, it is necessary to connect the TRANSMIT output of a calling party to the RECEIVE input of a called party and vice versa. Thus, for each telephone conversation, two speech paths are required. In the configuration shown in Figure 4, four simultaneous conversations are possible. With all of the MT8804A's reset, the junctors (J_0 - J_3) are floating and not assigned to any particular telephone line. Thus, the junctor can be completely controlled by software in a microprocessor system, independent of the particular telephone line being switched. The software must maintain a record of which junctors are in use and which are free for completing calls. To better illustrate these points, all the steps required to complete a connection between two parties will be outlined.

The signal paths connecting the junctors of MT8804A's have been arbitrarily named S_0 to S_7 for reference. To connect a call from a given source party to a destination party, it is necessary to interconnect the respective TRANSMIT and RECEIVE leads. To accomplish this, addresses for the source and destination lines of the call must first be generated. The source address is derived from the off-hook conditions which are either encoded or scanned. The destination address is generated by reception of dial pulses or DTMF signals. Once these addresses have been established, the software can implement a control sequence to close the appropriate switches. This sequence is not unique as the order in which switches in the MT8804A are closed is not critical. The example which follows illustrates a possible control sequence that could be used.

If it is assumed that all the signal paths (S_0 - S_7) are free, then S_0 and S_1 would be used to complete the call. The source and destination addresses, once generated, are sequentially placed on the microprocessor data bus and hence onto the address inputs of the MT8804A's. Since S_0 and S_1 are being used, the data inputs (D_3 D_2 D_1 D_0) must be alternatively set to 0001 and 0010. With the source address on the address lines and D_3 D_2 D_1 D_0 = 0001, the ADDRESS ENABLE (AE) of chip 'A' is taken HIGH. The data lines are next set to D_3 D_2 D_1 D_0 = 0010 and the AE input of chip 'C' is taken HIGH. This completes the connections of the TRANSMIT and RECEIVE leads of the source party to S_0 and S_1 respectively. It remains only to connect the destination TRANSMIT lead to S_1 and RECEIVE lead to S_0 to complete the 2-way interconnection. To do this, the destination address is set on the address inputs of the MT8804A's. The data lines are again set to D_3 D_2 D_1 D_0 = 0010 and the AE input of chip 'A' is taken HIGH.

Lastly, with D_3 D_2 D_1 D_0 = 0001, the AE input of chip 'C' is pulsed high. This connects the TRANSMIT and RECEIVE leads of the destination line to S_1 and S_0 respectively as required. All necessary interconnections are thus complete and the processor become free to service other calls.

To disconnect a telephone call, the following steps are taken. Once a change in off-hook condition is detected, the address from the scanning circuitry is put onto the address lines and the data lines are all

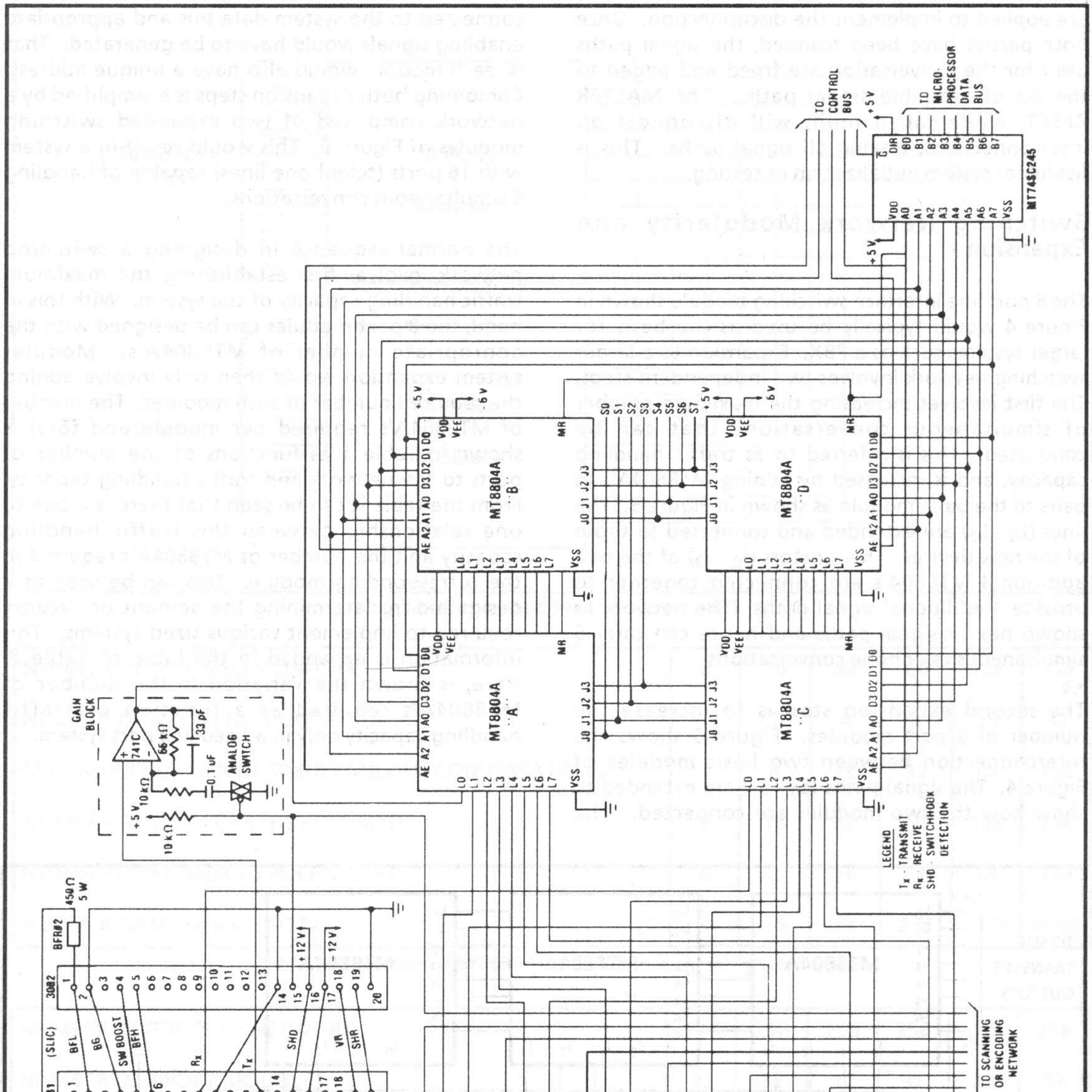


Fig. 4. Line Interface Switching Circuit (8-Port Module)

set to zero. The appropriate Address Enable pulses are applied to implement the disconnection. Once both parties have been scanned, the signal paths used for the conversation are freed and added to the list of available signal paths. The MASTER RESET, when taken high, will disconnect all interconnections, freeing all signal paths. This is useful for system initialization or testing.

Switching Network Modularity and Expansion

The 8 port line interface switching module shown in Figure 4 would typically be used as the basis for larger systems such as a PBX. Expansion to a larger switching network involves two independent steps. The first involves increasing the maximum number of simultaneous conversations that can be conducted. This is referred to as traffic handling capacity, and is increased by adding MT8804A's in pairs to the basic module as shown in Figure 5. The lines (L_0 - L_7) are extended and connected to those of the new devices. The junctors (J_0 - J_3) of the two additional MT8804's are connected together to provide 4 additional signal paths. The network as shown has 12 signal paths and hence can carry 6 simultaneous telephone conversations.

The second expansion step is to increase the number of 8 port modules. Figure 6 shows the interconnection between two basic modules of Figure 4. The signal paths (S_0 - S_7) are extended to show how the two modules are connected. The control lines of each module (not shown) would be connected to the system data bus and appropriate enabling signals would have to be generated. That is, each module would also have a unique address. Combining both expansion steps is exemplified by a network comprised of two expanded switching modules of Figure 5. This would result in a system with 16 ports (telephone lines) capable of handling 6 simultaneous conversations.

The normal sequence in designing a switching network involves first establishing the maximum traffic handling capacity of the system. With this in hand, the 8 port modules can be designed with the appropriate number of MT8804A's. Modular system expansion would then only involve adding the required number of such modules. The number of MT8804A's required per module and total is shown in Table 1 as functions of the number of ports to the network and traffic handling capacity. From the table it can be seen that there is a one to one relationship between this traffic handling capacity and the number of MT8804A's required in the corresponding module. This can be used as a design aid in determining the amount of circuitry required to implement various sized systems. This information is expanded in the table of Table 2. Here, is shown the variation in the number of MT8804A's required as a function of traffic handling capacity only in a fixed 256 port system.

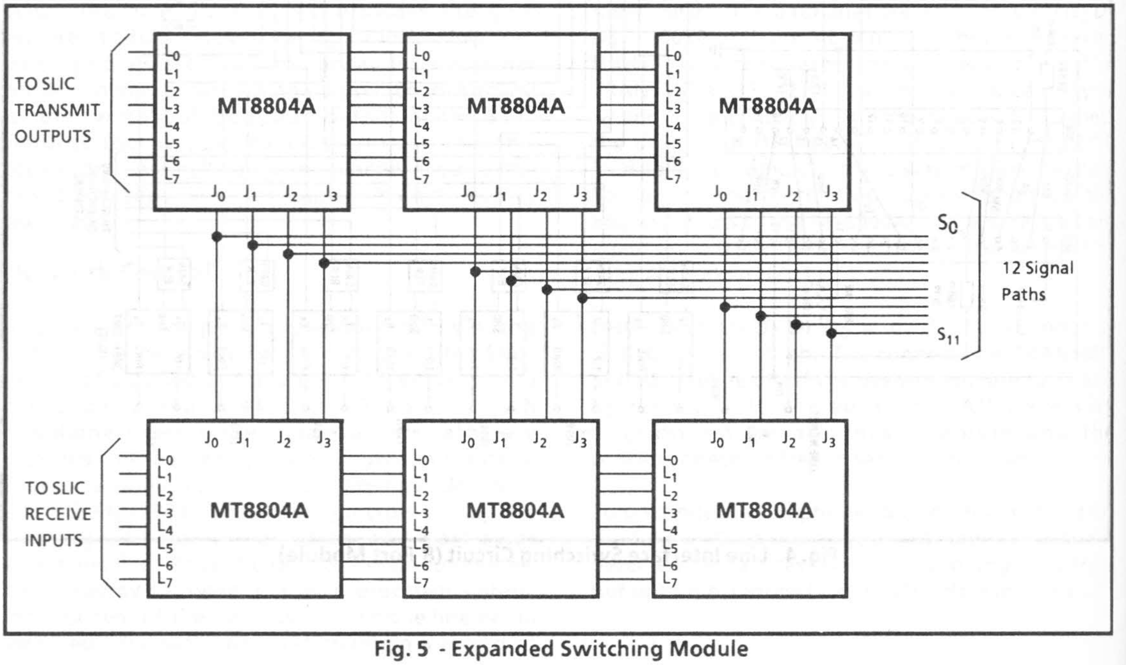


Fig. 5 - Expanded Switching Module

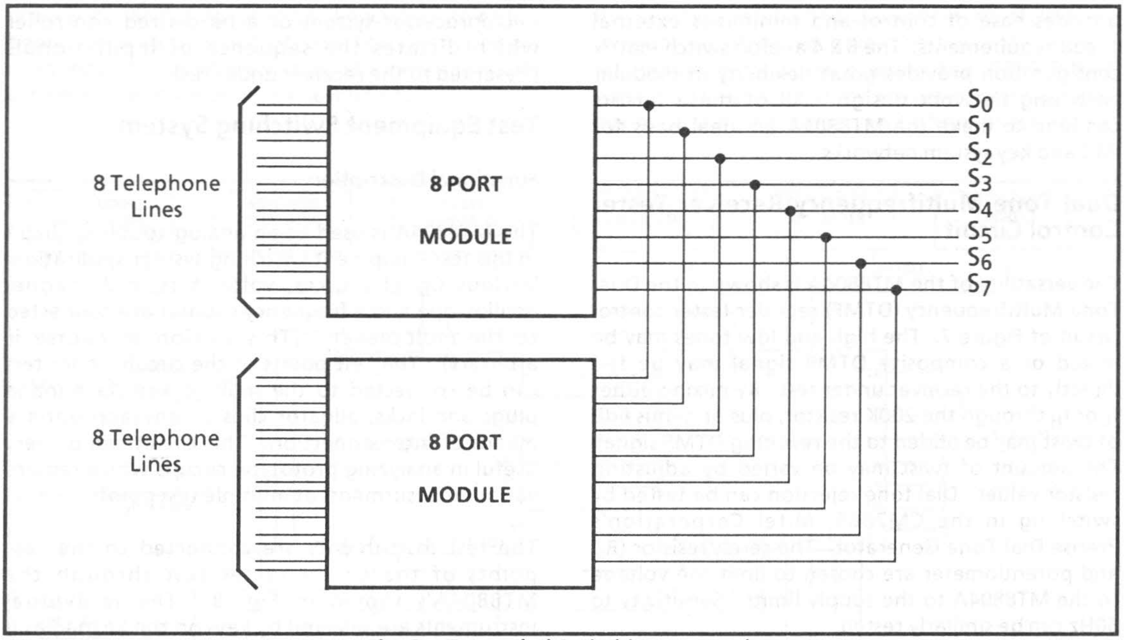


Fig. 6 - Expanded Switching Network

NUMBER OF PORTS TO NETWORK	8	16	32	64	128	256
NUMBER OF 8 PORT MODULES	1	2	4	8	16	32
MAXIMUM NUMBER OF SIMULTANEOUS CONVERSATIONS	4	8	16	32	64	128
NUMBER OF SIGNAL PATHS REQUIRED	8	16	32	64	128	256
NUMBER OF MT8804A'S PER MODULE	4	8	16	32	64	128
NUMBER OF MT8804A'S TOTAL	4	16	64	256	1024	4096

Table 1 - Number of MT8804A's as a Function of System Size

NUMBER OF PORTS TO NETWORK	256	256	256	256	256	256
NUMBER OF 8 PORT MODULES	32	32	32	32	32	32
MAXIMUM NUMBER OF SIMULTANEOUS CONVERSATIONS	4	8	16	32	64	128
NUMBER OF SIGNAL PATHS REQUIRED	8	16	32	64	128	256
NUMBER OF MT8804A'S PER MODULE	4	8	16	32	64	128
NUMBER OF MT8804A'S TOTAL	128	256	512	1024	2048	4096

Table 2 - Number of MT8804A's as a Function of Traffic Density for a 256 Port Network

Summary

Using the MT8804A in line interface switching systems offers many advantages over conventional circuit elements. Replacing relays or smaller analog switch packages with this device results in great reductions in size and power consumption. Simultaneously, a low level of interchannel crosstalk is maintained. The on-chip control memory with microprocessor compatible inputs

provides ease of control and minimizes external circuit requirements. The 8 x 4 analog switch matrix configuration provides great flexibility in modular switching network design. All of these factors combine to make the MT8804A an ideal basis for PBX and key system networks.

Dual Tone Multifrequency Receiver Tester Control Circuit

The versatility of the MT8804A is shown in the Dual Tone Multifrequency (DTMF) receiver tester control circuit of Figure 7. The high and low tones may be mixed or a composite DTMF signal may be fed directly to the receiver under test. By mixing either f_L or f_H through the 200K resistor, plus or minus 6dB of twist may be added to the resulting DTMF signal. The amount of twist may be varied by adjusting resistor values. Dial tone rejection can be tested by switching in the CM7065, Mitel Corporation's Precise Dial Tone Generator. The series resistor (R_S) and potentiometer are chosen to limit the voltage to the MT8804A to the supply limits. Sensitivity to 60Hz can be similarly tested.

If the receiver under test has the facility to accept dial pulses, these may be generated by switching the power supplies in and out at the required rates. A single pole double throw relay R1, is added to provide a switchable output impedance to simulate long line conditions. The relay drive is also switched by the MT8804A. The control of the MT8804A is provided by a stored test program in a microprocessor system or a hardwired controller which dictates the sequence of input signals presented to the receiver under test.

Test Equipment Switching System

Functional Description

The MT8804A is used as an analog coupling circuit in this test equipment switching system application. Various signal sources, voltmeters, a 2-channel oscilloscope and a frequency counter are connected to the multiplexer. (This section of course is arbitrary). The test points of the circuit under test can be connected to the multiplexer via banana plugs and jacks, aligator clips or any appropriate means of interconnection. This circuit can be very useful in analyzing prototype circuits which require various measurments at multiple test points.

The test instruments are connected to the test points of the circuit under test through the MT8804A's shown in Fig. 8. The individual instruments are selected by keys on the keypad as is the particular test point to which this equipment is connected. The system is operated as follows. First the 'TEST POINT' switch is pressed, followed by one of the numbered keys on the keypad. These correspond to the test points. Next, a sequence of keys designated the same as the test equipment is pressed. Finally the 'CONNECT' button is pressed. This completes the connection of the test equipment keyed in to the selected test point. This

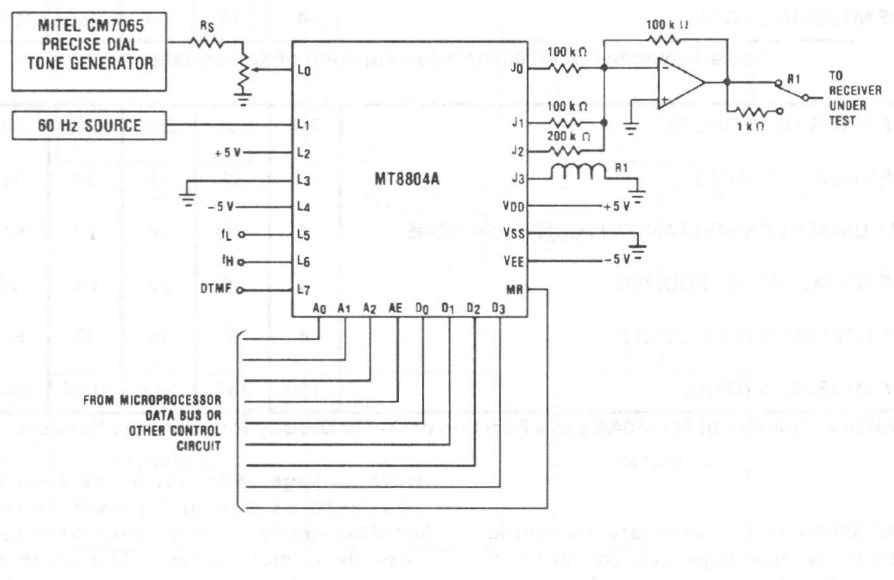


Fig. 7 - DTMF Receiver Tester Control Circuit

procedure can be repeated until each test point has been connected or all of the test instruments assigned. The signal sources may be simultaneously connected to more than one test point.

It is a simple matter to disconnect all of the test instruments from a given test point. This is accomplished by again pressing the 'TEST POINT' switch, keying in the number corresponding to the appropriate test point and then pressing the

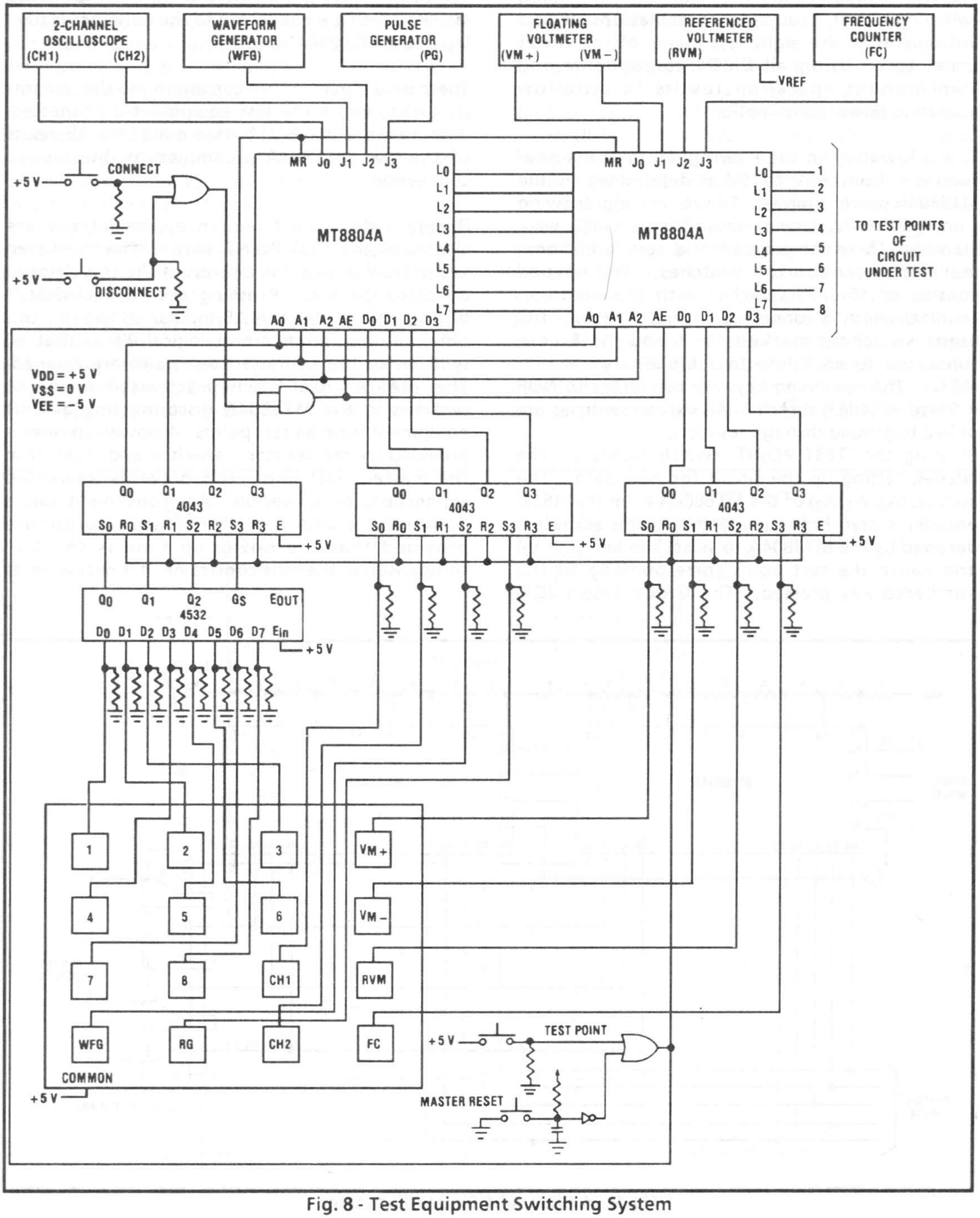


Fig. 8 - Test Equipment Switching System

'DISCONNECT' button. Pressing the 'MASTER RESET' switch at any time disconnects all test instruments from all test points.

Circuit Operation

The two MT8804A's are the heart of this analog switching circuit, coupling combinations of test instruments to the eight test points of the circuit under test. Using all CMOS components and asynchronous operation results in ultra-low operating power consumption.

The allowable voltage swing from the signal sources is from +5V to -5V as determined by the MT8804A power supplies. The control inputs swing from +5V to 0V. User control of the circuit is via a standard 16 switch keypad and four additional momentary pushbutton switches. The keypad consists of 16 SPST switches with one common terminal which is connected to V_{DD} = +5V. The eight switches, marked '1' through '8' are connected to an 8 line to 3 bit binary encoder (4532). The remaining keys are connected to NOR R-S latches (4043) directly. All sixteen switches are pulled to ground through resistors.
Pressing the 'TEST POINT' switch clears all the latches, setting up the circuit for new data. The address (A_0, A_1, A_2) of the MT8804A from the '4532' encoder is asynchronously latched. This address is decoded by the MT8804A to select the line (L_0 - L_7) and hence the test point corresponding to the numbered key pressed. The Group Select (GS) output of the '4532' goes high whenever one of its eight data inputs goes high. This signal is also latched and used to gate the AE pulse to the MT8804A. This ensures that a test point number has been entered and hence prevents unwanted or accidental connections. A series of designated test equipment keys is pressed setting corresponding latches which are connected to the data inputs (D_0 - D_3) of the MT8804A's.

These data inputs in turn correspond to the junctors (J_0 - J_3) to which the test equipment is connected. Pushing the 'CONNECT' button pulses the AE inputs of the two MT8804A's, completing the desired connection.

During a disconnect sequence, the latches are cleared by the 'TEST POINT' switch. The numbered key pressed sets up the address of the test point to be disconnected. Pressing the 'DISCONNECT' button next pulses the AE inputs. However, this time, all data inputs are at logical 0's so that all switches to the addressed test point are opened. The 'MASTER RESET' when activated opens all switches in the MT8804A disconnecting all test equipment from all test points. A power-up reset is provided by the resistor, capacitor and inverter in the master reset line. This prevents unwanted connections on power-up. Any convenient values of resistance and capacitance are appropriate provided that the power-up time is short in comparison to the time constraint. It is necessary, at

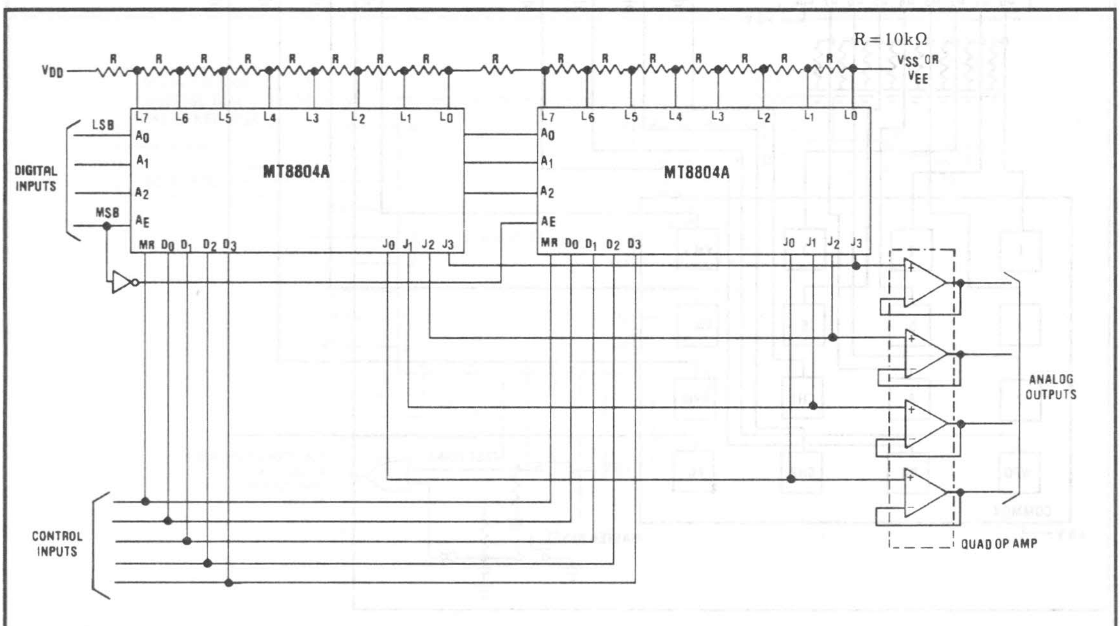


Fig. 9 - 4-Channel 4-Bit D/A Converter

all times, to supply power to the switching circuit prior to energizing signal sources.

4-Channel 4-Bit D/A Converter

The circuit of Figure 9 can be used to implement a low resolution (4-Bit), multichannel D/A converter. The digital signals are input on the address lines (A_0 - A1, AE) and the analog signals are switched from the resistive divider to the lines of the MT8804A (L_0 - L_7) and onto the junctors as selected by the data inputs. Any voltage profile can be programmed be it linear, logarithmic etc. by selecting the appropriate resistors for the divider network. The linearity and monotonicity of the converter are determined by the matching of resistors used. The temperature stability of the converter is dependent upon the relative tracking of the resistors in the network with temperature. The resistor network is shown with one end connected to V_{DD} and the other to V_{SS} or V_{EE}. By setting $V_{EE} = -V_{DD}$, the converter outputs will swing from V_{DD} to $V_{SS} = 0V$ in one mode and symetrically about 0V from $\pm V_{DD}$ in the other. The op amp buffers are used to reduce the effects of the ON resistance of the MT8804A.

The four analog outputs can simultaneously provide four independent voltages or any combination of outputs may be at the same voltage. The converter can be expanded to more digital inputs by extending the resistive ladder and adding MT8804's.

Programmable Attenuator

The programmable attenuator shown in Figure 10 is capable of providing up to 61dB of attenuation or 20dB of gain. Selecting the input attenuation is accomplished via the address inputs (A_0, A_1, A_2) and can be chosen in 3dB steps. The range is selected in 20dB steps by gating an attenuated input signal onto the appropriate junctor (J_0 -J_3) via the data inputs (D_0 - D_3). The attenuated input signal is buffered after passing through the MT8804A to provide constant input impedance to the attenuator circuit. The resistor multipliers shown provide a logarithmic profile of attenuation, calibrated in dB. A linear profile for use in control system applications is accomplished easily by appropriate choice of resistors. The attenuation accuracy is purely a function of resistor tolerances.

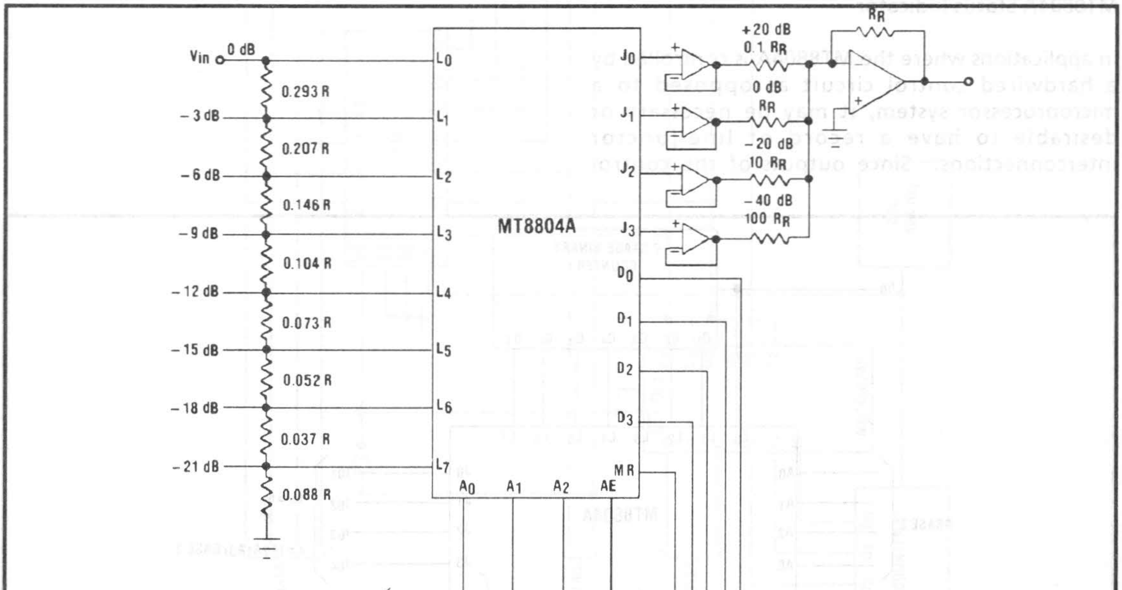


Fig. 10 - Programmable Attenuator

The circuit attenuation can be expressed as follows:

FOR ADDRESS $(A_0 A_1 A_2)_2 = N10$

$A_{dB} = -(V_0/V_i)\ dB = (3 \times N_{10} + A_R)\ dB$

Where $(A_2 A_1 A_0)_2$ Address expressed as binary number

A_R Attenuation in dB of range attenuator

Multi-Output 2^n Programmable Frequency Divider

The circuit of Figure 11 provides up to 4 independent output frequencies each of which is a binary weighted multiple of a given input frequency. The frequency division factor is represented by the binary coded number of the address inputs of the MT8804A. The division range for the circuit shown is from 2^0 to 2^7. This range can be increased by adding counters for frequency division and MT8804A's to do the switching. The four data inputs (D_0 to D_3) control which output line or lines are switched to a particular frequency. The master reset (MR) when taken high turns all switches off.

MT8804A Status Indicator

In applications where the MT8804A is controlled by a hardwired control circuit as opposed to a microprocessor system, it may be necessary or desirable to have a record of line-junctor interconnections. Since outputs of the control latches are not available, a duplicate memory map is required. An 8 x 4 array of light emitting diodes is used to provide visual output of the information (See Fig. 12). Control data written into the MT8804A is copied into a Random Access Memory. The RAM shown, the Fairchild 4710BX, is a CMOS device organized as 16 four bit words. As such, 2 MT8804A's could be mapped with one device. The RAM outputs can be used for control purposes as well as visual outputs as shown in the diagram.

A scanning oscillator and counter (negative edge triggered) are used to continuously read data out of the RAM and refresh the LED matrix. The address provided by this binary counter is decoded to a one of eight active low output format by the MD74SC138. Drive current is provided by two 74367 hex 3-state TTL buffers. A variable duty cycle waveform may be applied to the output enables to provide intensity modulation. When data is written into the MT8804A and RAM, the address is provided by the control circuit. This address is isolated from the scanning counter by the octal three state buffer, MD74SC241.

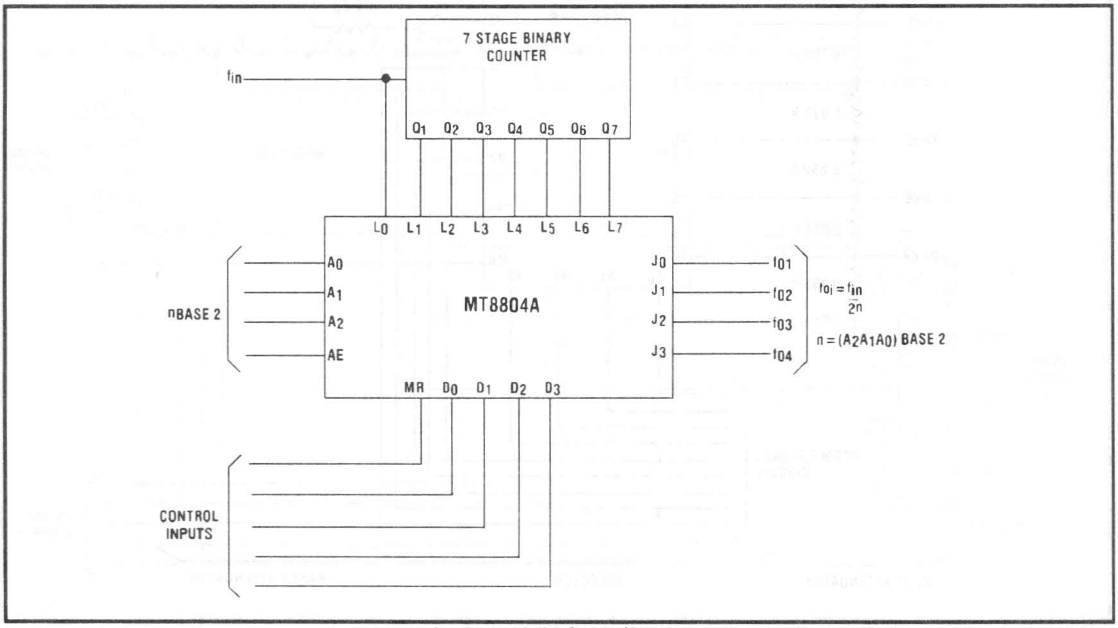


Fig. 11 - Digital Application

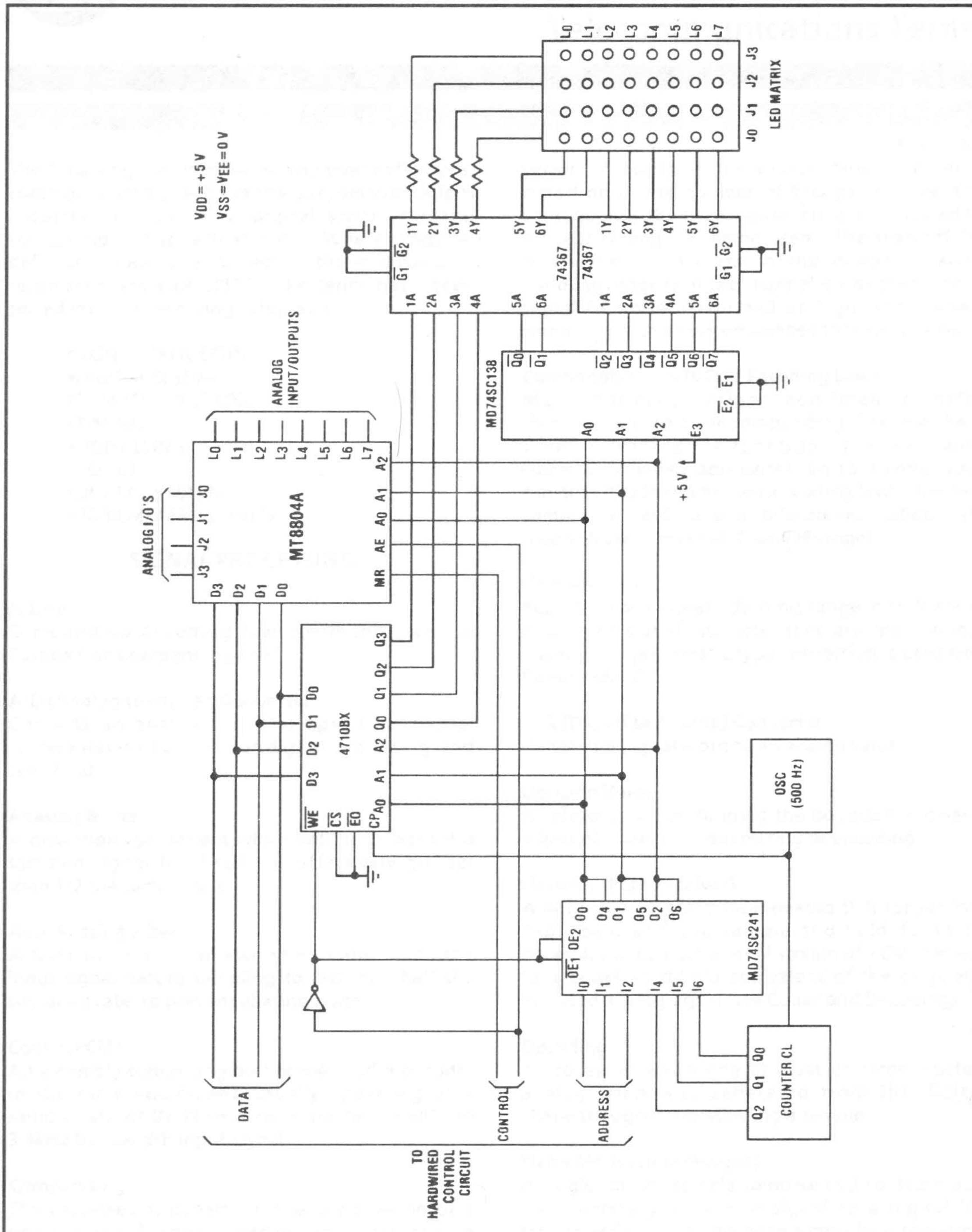


Fig. 12. Memory Map and Visual Indication of MT8804A Control Memory Status

NOTES:

Application Note **MSAN-102**

Glossary of Digital Telecommunications Terms

August 1986

The following is a list of terms, and their definitions, commonly encountered in the telecommunications industry in relation to digital switching and transmission of speech signals. Where possible, definitions have been based on the international recommendation of CCITT. The terms have been sorted into the following categories:

- •SIGNAL PROCESSING
- •DIGITAL SIGNALS
- •PCM MULTIPLEXING
- •TIMING
- •SIGNALLING
- •CODES
- •DIGITAL SYSTEMS
- •PARAMETERS & UNITS

SIGNAL PROCESSING

A-Law
Companding/encoding law commonly used in Europe (see Companding Law).

A/D (Analog to Digital) Converter
Converts an analog signal sample to a digital representation suitable for digital processing and switching.

Aliasing Noise
A distortion component which will be created if a sampled signal bandwidth is effectively greater than 1/2 the sample rate.

Anti-Aliasing Filter
A filter (normally lowpass) which band limits the input signal before sampling to less than half the sampling rate, to prevent aliasing noise.

Codec (PCM)
An assembly comprising an encoder and a decoder in the same equipment, usually operating at a sample rate of 8kHz to accommodate a 300Hz to 3.4kHz bandwidth input signal.

Companding
The processes of dynamic range compression of a signal and subsequent expansion in accordance with a given non-linear transfer characteristic (companding law) which is usually logarithmic. The purpose of companding is to allow transmission of the signal via a channel incapable of carrying the uncompressed dynamic range of the signal. In terms of digital transmission this involves a reduction in the number of bits per sample and consequently the transmission bit rate compared to a linear coding law being used. The tradeoff for this effective increase in the dynamic range handling capacity of the channel is a degradation in signal to noise performed at high signal levels compared with an uncompanded (linear) systems.

Companding Law (CCITT Encoding Law)
Mathematically defined non-linear transfer characteristic used for companding. This may be a smooth continuous function or a piecewise (commonly linear) approximation to a continuous function (CCITT segmented encoding law). The two commonly used laws in telecommunications are µ-Law (North America), A-Law (Europe).

Compression
Reduction of a signal's dynamic range in such a way that small signal characteristics are maintained. Usually a logarithmatic type conversion is used (see Companding).

D/A (Digital to Analog) Converter
Converts a digital word to an analog value.

Decision Value
A reference value defining the boundary between adjacent intervals in quantizing or encoding.

Decoder (PCM Receiver)
A device which performs repeated D/A conversion, expansion and the sample-and-hold function necessary to convert a serial stream of PCM samples to a sample-and-hold equivalent of the originally encoded analog signal (see Codec and Decoding).

Decoding
A process in which one of a set of reconstructed analog samples is generated from the digital character signal representing a sample.

Delta Modulation (Simple)
A single bit per sample iterative coding technique for converting an analog signal to a digital bit stream which can be decoded simply by integrating the digital bit stream and lowpass filtering. To obtain telephony quality transmission requires a sample rate of approximately 8kHz.

15

Delta-Sigma Modulation (Simple)
A single bit per sample iterative coding technique for converting an analog signal to a digital bit stream. The resulting bit stream is a pulse density function of the original analog signal which can be recovered simply by low pass filtering the bit stream. To obtain telephony quality transmission requires a sample rate of approximately 8kHz.

Dynamic Range
The dynamic range of a converter is a measure of its ability to handle a wide range of input amplitude and is defined as the ratio of the largest resolvable signal to the smallest signal that can be handled.

Encoder (PCM)
A device which performs repeated sampling, compression and A/D conversion to convert an analog signal to a serial stream of PCM samples representing the analog signal (see Codec and Encoding).

Encoding
Coding
The generation of digital character signals to represent quantized analog samples.

Encoding Law (see Companding Law)
The law defining the relative values of the quantum steps used in quantizing and encoding.

Error Ratio
A measure for the distortion of a digital signal is the error ratio which is defined as number of wrongly received bits divided by the total number of received bits.

Expansion
Expansion of a compressed signal back to its original dynamic range (see Companding).

HIDM (High Information Delta Modulation)
One of many companded delta modulation schemes. Operates at lower sample rates than simple delta modulation for equivalent performance.

Instantaneously Companded Delta-Sigma Modulation
As its name implies - an equivalent scheme in delta-sigma modulation to the HIDM scheme.

Linear Quantizing
Quantizing in which all the intervals are equal, i.e., linear A/D converter.

Non-Linear Quantizing
Quantizing in which the intervals are not all equal. This keeps the quantizing distortion as low as possible.

Pulse Code Modulation (PCM)
A process in which an analog signal is sampled, and the magnitude of each sample with respect to a fixed reference is quantized and converted by coding to a digital signal. This is the prevalent technique for digital transmission in communications systems.

Quantizing
A process in which samples are classified into a number of adjacent intervals (amplitude steps) each interval step being represented by a single value called the quantized value.

Quantizing Distortion
Due to the restriction of a finite number of produced amplitude steps, a difference inevitably occurs between the information which can be transmitted and the original information. This difference is called quantizing distortion.

S&H (Sample and Hold)
A circuit which samples a signal and holds the sample value until the next sample is taken. In A/D conversion, S/H is usually an analog function. In D/A conversion, the S/H may be performed digitally, making continuous use of the D/A convertor or the D/A convertor may be shared by other functions and its output signal held by an analog sample and hold circuit.

Sample
The value of a particular characteristic of a signal at a chosen instant.

Sampled Data System
A system that operates on samples of the analog input signals. Can be either analog (e.g., switched capacitor filter) or digital (speech coding/digital filter) processing or both.

Sampling
The process of taking samples, usually at equal time intervals.

Sampling Rate
The number of samples per unit time.

Segmented Encoding Law
An encoding law which an approximation to a smooth law is obtained by a number of linear segments.

Single Channel Codec
Codec which is designated to operate on a single signal source and *not* in a multiplexed mode performing the codec functions for more than one signal source.

Single Chip Codec
A single integrated circuit capable of performing all codec functions and in some cases providing an auxiliary signalling interface. It may be either single channel or multiplexable.

Smoothing (Decode or Reconstruction) Filter
Usually lowpass. Restores the desired analog signal at the S&H, D/A or decoder output by blocking high frequency components produced by sampling.

Working Range
The permitted range of values of an analogue signal over which a transmission or other processing equipment can operate.

Virtual Decision Value
Two hypothetical decision values, used in quantizing or encoding. Located at the ends of the working range used, and obtained by extrapolation from the real decision values. Effectively specify the maximum input signal amplitude.

μ-Law
Companding/encoding law commonly used in North America (see Companding Law).

DIGITAL SIGNALS

ADI
Alternate digit inversion. Used with A-Law to ensure sufficient 1-0/0-1 transitions for clock extraction (timing recovery) in PCM multiplex transmission equipment.

Asynchronous Transmission
A mode of communication characterized by start/stop transmissions with undefined time intervals between transmissions.

Binary Digit
A member selected from a binary set, e.g., 1,0; V+, V-; H,L.

Note: Bit is in abbreviation for binary digit.

Character Signal
A set of signal elements representing a character, or in PCM representing the quantizing value of a sample.

Note: In PCM, the term "PCM word" may be used in this sense.

Digit
A member selected from a finite set.

Note 1: In digital transmission, a digit may be represented by a signal element, being characterized by the dynamic nature, discrete condition and discrete timing of the element, e.g., it may be represented as a pulse of specified amplitude and duration.

Note 2: In equipment used in digital transmission, a digit may be represented by a stored condition being characterized by a special physical condition, e.g., it may be represented as a binary magnetic condition of a ferrite core or voltage condition in a semiconductor memory cell.

Note 3: The context of the use of the term should be as such as to indicate the radix of notation. (The meaning of "digit" in Notes 1, 2, and 3 translates into French as "élément numérique".)

Note 4: In telephone subscriber numbering, a digit is any of the numbers 1, 2, 3...9 or 0 forming the elements of a telephone number (Recommendation Q.10). (This meaning of "digit" translates into French as "chiffre".)

Digital Signal
A signal constrained to have a discontinuous characteristic in time and a set of permitted discrete values.

Equivalent Bit Rate
In a line coded signal, the number of binary digits that can be transmitted in a unit of time.

Note: The point which the equivalent bit rate is referred may be either real or hypothetical.

Intersymbol Interference
Interference in a digital (or any Time Division) transmission system caused by a symbol in one signalling interval being spread out and overlapping the sample time of a symbol in another signal interval.

Jitter
Short-term variations of the significant instants of a digital signal from their ideal positions in time.

Regardless of the stability of clocks at both ends of a digital transmission system, certain amounts of instability occur in the received signal because of external electrical disturbances and changing physical parameters of the transmission link. The resulting instability in the line clock is referred as "jitter".

Regeneration
The process of recognizing and reconstructing a digital signal so that the amplitude, waveform and timing are constrained within stated limits.

Synchronous Transmission
A mode of digital transmission in which discrete signal elements (symbols) are transmitted at a fixed and continuous rate.

PCM MULTIPLEXING

Channel Bank
Terminal equipment for a transmission system used to multiplex individual channels using FDM or TDM techniques.

Digital Multiplex Equipment
Equipment for combining, by time division multiplexing (multiplexer) a defined integral number of digital input signals into a single digital signal at a defined digit rate and also for carrying out the inverse function (demultiplexer).

Frame
A set of consecutive digit timeslots in which the position of each digit slot can be identified by reference to a frame alignment. The frame alignment signal does not necessarily occur, in whole or in part, in each frame.

Highway
A common path or a set of parallel paths over which signals from a number of channels pass with separation achieved by time division.

Justification (Pulse Stuffing)
A process of changing the rate of a digital signal in a controlled manner so that it can accord with a rate different from its own inherent rate, usually without loss of information.

Multiframe
A set of consecutive frames in which the position of each frame can be identified by reference to a multiframe alignment signal. The multiframe signal does not necessarily occur, in whole or in part, in each multiframe.

Multiplexing
The process of combining the multiple signals into a single channel for transmission over common facilities.

PCM Multiplex Equipment
Equipment for deriving a single digital signal at a defined digit rate from two or more analogue channels by a combination of pulse code modulation and time division multiplexing (multiplexer) and also for carrying out the inverse function (demultiplexer). The description should be preceded by the relevant equivalent binary digit rate, e.g., 2048 kbit/s PCM multiplex equipment.

Primary Block
(American: Digroup)
A basic group of PCM channels assembled by time division multiplexing.

Note: The following conventions could be useful:

Primary block μ- a basic group of channels derived from 1544 kbit/s PCM multiplex equipment.

Primary block A- a basic group of PCM channels derived from 2048 kbit/s PCM multiplex equipment.

Time Division Multiplexing
Several information channels are multiplexed (time shared) over a single communication circuit by sampling each channel periodically and allocating each sample an assigned timeslot in the circuit.

T1 Carrier System (North America)
PCM multiplex equipment using 8 digit μ-Law, 24 channels (timeslot).

30 Channel Mux (U.K. & Europe)
CCITT recommended form PCM multiplex equipment. 8 digit A Law, 30 speech channels + 2 utility channels (32 timeslots in all) transmission rate 2,048 kbit/s.

Transmultiplexer
An equipment which transforms signals derived from frequency division multiplex equipment to time division multiplexed signals having the same structure as those derived from PCM multiplex equipment and vice versa.

24 Channel Mux (U.K.)
Early PCM multiplex equipment: 7 digit A-Law, 1 signalling bit associated with each timeslot, 24 channels (timeslots), transmission rate 1536 kbit/s.

TIMING

Channel Timeslot
A timeslot starting at a particular phase in a frame and allocated to a channel for transmitting a character signal and possibly in-slot signalling or other information.

Digit Timeslot
A timeslot allocated to a single digit.

Frame Alignment
The state in which the frame of the receiving equipment is correctly phased with respect to that of the received signal.

Frame Alignment Signal
The distinctive signal used to enable frame alignment to be secured.

Frame Alignment Timeslot
A timeslot starting at a particular phase in each frame and allocated to the transmission of a frame alignment signal.

Master Clock
A clock which generates accurate timing signals for the control of other clocks and possibly other equipments.

Mesochronous
Two signals are mesochronous if their corresponding significant instants occur at the same average rate.

Non-Synchronous Network (Asynchronous Network)
A network in which the clocks need not be synchronous or mesochronous.

Signalling Timeslot
A timeslot starting at a particular phase in each frame and allocated to the transmission of signalling.

Synchronous
Two signals are synchronous if their corresponding significant instants have a desired phase relationship.

Synchronous Network
A network in which the clocks are controlled so as to run, ideally, at identical rates, or at the same mean rate with limited relative phase displacement.

Timeslot
Any cyclic time interval which can be recognized and defined uniquely.

Timing Recovery (Timing Extraction)
The derivation of a timing signal from a received signal.

Timing Signal
A cyclic signal used to control the timing of operations.

SIGNALLING

CCIS
Common channel interoffice signalling.

Common Channel Signalling
A signalling method using a link common to a number of channels for the transmission of signals necessary for the traffic via these channels.

Signalling
The exchange of electrical information (other than by speech) specifically concerned with establishment and control of connections, and management, in a communication network. May be transmitted by independent link, designed timeslots, designation bit positions in a timeslot or by "bit stealing" specific speech bit positions in the PCM codeword. In a transmission, system signalling may carry equipment status, routing, billing and testing data.

When referred to the line card of a digital switch, signalling includes-on hook/off hook status, ring trip, applying ringing, dialed digit information, test signals. Where ON CARD timeslot assignment is performed, signalling also includes timeslot identification.

Speech Digit Signalling (sometimes called Bit Stealing)
Signalling in which digit timeslots primarily used for the transmission of encoded speech are periodically used for signalling.

CODES

A-Law/or μ-Law Companded
8 bit PCM Binary code. The codes almost universally used for PCM digital switching and transmission. When a reference is made to PCM, it is almost invariably these codes which are being referred to (A-Law version in Europe and μ-Law version in North America).

Alternate-Mark Inversion Signal (AMI) (Bipolar Signal)
A pseudo-ternary signal, conveying binary digits, in which successive "marks" are normally of alternate, positive and negative, polarity but equal in amplitude and in which "space" is of zero amplitude.

HDB-3 Code - High Density Bipolar 3 Code
Here two consecutive ones of the same polarity are permitted (interrupting a zero sequence which is too long).These violation bits, moreover, are arranged to form an AMI sequence in itself. (See modified AMI).

Line Code
A code chosen to suit the transmission medium and giving the equivalence between a set of digits generated in a terminal of other processing equipment and the pulses chosen to represent that set of digits for the line transmission.

Modified Alternate Mark Inversion
An AMI signal which does not strictly conform with alternate mark inversion but includes violations in accordance with a defined set of rules.

PCM Binary Code
A pulse code in which the quantized values are identified by binary numbers taken in order.

Note: This term should not be used for line transmission.

Pulse Code
A code giving the equivalence between the quantized value of a sample and the corresponding character signal.

DIGITAL SYSTEMS

'Blocking' System
There are more telephones than through connection paths so dynamic channel allocation is needed on a demand basis. If all channels are busy, new calls are are blocked from completion or are delayed until a channel becomes available.

Connection
The circuits and equipment which together provide a communication path between two subscriber stations.

Digital Switching
A process in which analog signals are converted to digital signals and connections are established by operations on the digital signals. Alternatively, digitally transmitted signals are routed by operating on the digital signals directly without converting to analog.

'Non-Blocking' System
Each telephone has a guaranteed through connection when needed. This may be in the form of dedicated channels (fixed channel asignment) which guarantees any phone the same communication channel at any time.

STS Switch
Space Time Space Switch - large switch consisting of a time switch block between two space switch blocks.

Space Division
Use of different physical paths to transmit two or more channels (N.B. 'space division multiplex' is a contradiction in terms).

Space Switch (Abbrev.) Space Division Switch
Multiport switch in which ports are interconnected by use of different physical paths.

TST Switch
Time Space Time Switch - large switch consisting of a space block between two time switch blocks.

Time Switch (Abbrev.) Time Division Multiplex Switch
Multiport switch in which all ports have access to the same physical path on which transmitted data from individual ports are allocated unique timeslots. Send and receive paths are connected by both accessing the same timeslot. The path may be a serial data or parallel data highway.

PARAMETERS & UNITS

dB
Decibel - unit of measure of relative power level defined as $10\log_{10}(P_1/P_2)$ assuming R1=R2 where P_1 and P_2 are the power levels.

dBm
Power in dB relative to 1 mW.

dBm0
dBm referred to or measured at a point of zero transmission level.

dBmp
dBm psophometrically weighed. Unit of power in dBm measured with psophometric weighting. Conversion is as follows:

dBmp = $10 \log_{10}$pWp − 90
= dBa − 84
= dBm − 2.5 (for flat noise 300-3400 Hz)

dBm0p
Circuit noise in dBm0 measured on a line with a noise measuring set having psophometric weighting.

dBr
dB relative to point of zero transmission level.

dBrn
(decibels above reference noise). Weighted circuit noise power in dB referred to 1 picowatt (−90 dBm) which is defined as 0dBrn. Type of weighting is indicated by next letter (see dBrnc).

Note: With 'C' message weighting, a 1mW 1 kHz tone will read +90 dBrn, but the same power with the noise randomly distributed over a 3 kHz band (300-3400 cps) will read +88dBrn.

dBrnc
Weighted circuit noise power in dBrn, measured on a line by noise measuring set with 'C' message weighting.

dBrnc0
Noise measured in dBrnc referred to zero transmission level point (0TLP).

$$dBrnc0 = dBrnc - 20 \log_{10} R_{LOAD}/600$$

Gain Level Linearity (U.K.)
See Gain Tracking Error.

Gain Tracking Error (N.A)
Gain Level Linearity
A measurement of the dependence of a device gain on signal level. The output signal is compared to the input signal (assuming unity gain) over a range of input signals. The variation of gain from a constant gain (determined at 0dBm input level) is the gain tracking error.

Idle Channel Noise
The total signal energy measured at the output of the device when the input of the device is grounded. Unless otherwise specified, this is a wideband noise measurement.

Load Capacity
(Overload Point)
In PCM, the level expressed in dBm0, of a sinusoidal signal the positive and negative peaks of which coincide with the positive and negative virtual decision values of the encoder.

Peak Limiting
In PCM, the effect caused by the application to an encoder of an input signal whose value exceeds the virtual decision values of the encoder.

Quantizing Distortion
The distortion resulting from the process of quantizing.

Quantizing Distortion Power
The power of the distortion component of the output signal resulting from the process of quantizing.

Signal to Distortion Ratio (S/D)
The ratio between the input signal level, and the level of all components that are present when the input signal (usually a 1.020 kHz sinusoid) is eliminated from the output signal (by filtering for example).

Weighting Filters
Several different filters have been used to represent the transmission passband characteristics of different communication networks. The two most frequently used are C-message (N.A) and Psophometric (Europe) weighting filters.

NOTES:

MITEL®

Application Note MSAN-106
An Introduction to Mitel DTMF Receivers

November 1981

Dual-tone multi-frequency (DTMF) receivers have been built using various filtering techniques. The most recent relies on MOS/LSI for higher quality and reduced cost. LSI DTMF detection relies on algorithms developed both empirically and analytically. New generations of receivers are just emerging: miniature hybrid receivers are already available in volume production. General acceptance in the marketplace has resulted in an acceleration of the innovation and the pricing trends made possible by the latest advances in LSI technology.

DTMF Signalling

Introduced over 25 years ago, DTMF signalling (also known as Touch-Tone*, Tel-Touch, etc.) has been steadily gaining ground at the expense of dial-pulse signalling. Not only is a Touch-Tone telephone more convenient and more efficient to use, but it offers a higher reliability in the transmission of signals. As a result, signalling is no longer confined to telephony but has seen its domain expanded to various fields such as answering machines, radio communications, data transmissions and remote control.

The telephone handset generates a composite audio signal made of the superposition of two tones selected by line-and-column addressing of a keyboard. This scheme is shown in Figure 1.

These frequencies were chosen in such a way that neither their harmonics nor their intermodulation products fall in one of the tone bands. Separation between tones is typically 10%.

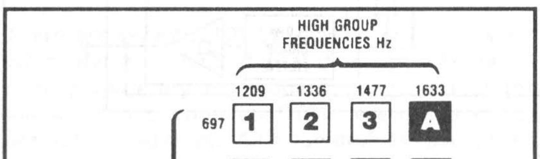


Fig. 1 - DTMF Keypad Encoding

The fourth column of buttons (1633 Hz tone) is not usually present in today's telephone sets. However, it is available for future use. A 4 x 4 matrix of buttons is presently used in some military phones and is suitable for implementation in telephone sets intended for multiple functions such as financial transaction terminals, credit checking machines and some PBX or CBX systems.

The dual-tone signal is heard in the ear-piece and is sent over the telephone lines to the private branch exchange (PBX) or directly to the central office, where it must be decoded into the digit that it represents. The decoder circuitry - or receiver - will convert the DTMF signal to a binary format or to a 2-of-8 format. For the traditional dial-pulse equipment, a further conversion is needed to achieve a complete Touch-Tone to dial-pulse interface, allowing telephone companies to offer subscribers Touch-Tone service in areas where the equipment is not compatible. Such an application is termed a tone-to-pulse converter.

Before 1974, a number of techniques were used to achieve DTMF detection. Passive filters, using LC networks for each frequency, can still be found in some installations. When integrated operational amplifiers became more readily available, the designers switched to active filters using IC's and RC networks. With the advent of the phase-lock-loop in IC form, new designs were introduced embodying this approach.

Every solution outlined so far had technical or cost-related disadvantages. Advances in MOS/LSI technology have made it possible to solve the problem of DTMF decoding at considerable cost savings.

Digital DTMF Detection

The basic method of discriminating various frequencies from each other using digital logic is to relate the number of cycles of some reference clock signal to each period of the unknown frequency. Typically, the DTMF signal is sent first through a band-splitting filter which separates the high- and

* Touch-Tone is a registered service mark of AT&T

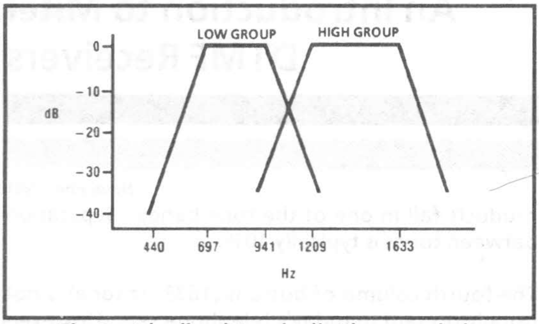


Fig. 2 - Idealized Bandsplit Characteristic

low-band frequencies (Figure 2). Each frequency is then square-shaped and processed separately. The problem consists of establishing whether a frequency is recognizable as a DTMF tone, considering that this is within a certain frequency tolerance, or that it is a mere simulation of a true DTMF tone, such as produced by speech. As a result, the designer is faced by a dilemma: if the "accept" criteria are too relaxed, DTMF tone-pairs are quickly recognized as valid, and so are speech segments which simulate a real DTMF signal. This is referred to as "talk-off". Now, if the "accept" criteria are too strict, detection time is inordinately stretched and the receiver is no longer in compliance with timing requirements. In other words, if detection time is fixed this becomes a compromise between:

A. Tolerance to received-tone imperfections and noise.

B. Immunity to tones simulated by speech (talk-off).

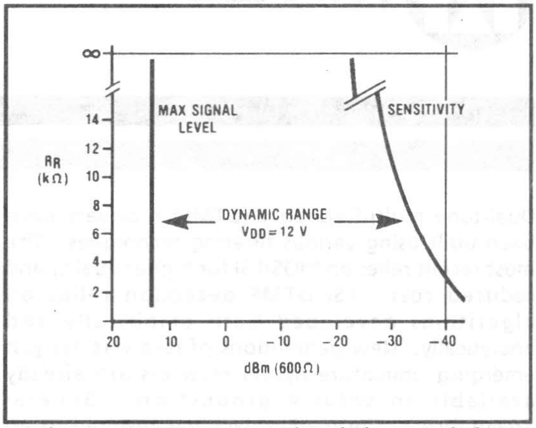


Fig. 4 - MH88305 Input Signal Characteristics

Modern receiver design can successfully deal with this problem by optimizing both the front-end filtering and the digital detection algorithm. Such a product - the MH88305 - has been developed by Mitel to serve the most exacting requirements of DTMF reception, as seen in central office applications. The MH88305 is a self-contained hybrid DTMF receiver measuring 1.5x2.5x0.25 inch (3.8x6.3x0.63cm).

No external components are needed to operate this receiver (even the time-base crystal is enclosed), although the addition in each case of a single resistor or capacitor allows the designer to modify three of the device parameters: detect time (time to detect the presence of a valid tone-pair); sensitivity (minimum acceptable signal level); and twist acceptance (degree of mismatch between the

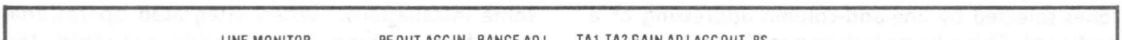


Fig. 3 - MH88305 Functional Block Diagram

amplitudes of the two tones of a pair). The unit connects directly to the telephone line. Talk-off immunity is excellent: less than five "hits" on the Mitel test tape CM7291. Error rate is typically better than 1 error in 100,000 applied tones and third-tone tolerance meets the CEPT recommendation of (A-16) dBm for a swept in-band tone applied simultaneously with undeviated signal frequencies. Power consumption at 5V is a mere 50 mW and input sensitivity can be adjusted down to -42 dBm giving a maximum dynamic range of 55 dB as illustrated in Figure 4.

DTMF Receiver Specifications

The worst case specifications of a DTMF receiver are typical of Central Office requirements:

Input Dynamic range : -26 dBm to + 6 dBm

Twist (V_{FH}/V_{FL}) : -8 dB to + 4 dB

Dial Tone : 350 Hz mixed with 440 Hz

Tone Burst (min.) : 40 ms ON, 40 ms OFF

Repetition rate (max.) : 12 pps

Valid tone accept : ± 1.5%

Invalid tone reject : ± 3.5%

Signal-to-noise ratio : 16 dB

Silence gap bridging : 15 ms

For other applications, such as keyphone systems, the specifications are less stringent. No dial tone is used. Little twist exists on the line. In this case, some circuitry - such as the dial tone rejection filter - can be omitted.

Digital Detection Algorithm

There are several MOS/LSI devices on the market which perform DTMF digital detection. Some are even proprietary to companies involved in the manufacture of complete DTMF receivers, and thus are not sold as chips. All these devices have a basic tenet in common: digital period-counting relying on a zero-crossing detector. Little difference exists in the choice of tone bandwidths. The main divergences lie in the choice of criteria leading to accept or reject a tone-pair. It is instructive to discuss one of the more general techniques.

In order to reduce the overall system cost, the designer tries to shift the design complexity to the contents of the LSI device rather than the front-end filtering which is typically costlier. Thus, when the band-splitting filters have less-than-ideal attenuation, the separated tones will carry a residue from the other band. This, in addition to random noise, results in jitter of the zero crossings (Figure 5).

Averaging several pulses eliminates most of the jitter effects. However, it also allows easier speech simulation of tone-pairs. In order to improve speech rejection, single-period counting is made to concur with the counting of several periods. Such a technique is used in the Mitel MT8860 decoder and its variants, the MT8862 and MT8863. The Mitel MH88305, which uses the MT8863 digital decoder, also uses the LSI bandsplit filter, the MT8865. This device uses switched-capacitor filters implemented in Mitel's double-poly ISO²-CMOS™ technology.

The MT8860/8865 chip pair integrates an entire functional receiver, the external circuitry required being dependent on the user's system environment and specification. Typical enhancements might be a differential input amplifier for line interfacing; prefiltering for extra dial-tone rejection; agc circuitry for extended dynamic range. All of these enhancements are incorporated into the MH88305 hybrid.

In addition to the digital detection algorithm, Mitel tone receivers incorporate a further validation check during a period termed the guard-time. This time is user-accessible since it is set by an external RC time constant and it offers the designer further flexibility in optimizing receiver performance while complying with his particular system timing requirements. Use of the guard-time feature is fully described in the data sheets of the devices referenced here; Figure 6 tabulates the four main system timing parameters which may be adjusted.

Future LSI Receivers

Work is being conducted at Mitel to develop still smaller and more cost-effective receivers. The first of the new generation monolithic receivers now under development is the MT8870, which combines the filter and decoder functions in one chip contained in a compact 18-pin package. Gains in performance as well as reductions in cost and size are expected from this ISO²-CMOS device, making

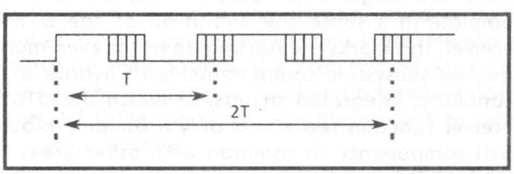


Fig. 5 - Zero-Crossing Jitter

Tone-Pair Recognition	Timing Condition*
SHALL EXIST	$T_P > t_{REC}$
MAY EXIST	$\overline{t_{REC}} \le T_P \le t_{REC}$
SHALL NOT EXIST	$T_P < \overline{t_{REC}}$
SHALL CEASE	$T_A > t_{ID}$
MAY CEASE	$T_{DO} \le T_A \le t_{ID}$
SHALL NOT CEASE	$T_A < t_{DO}$

Typical Values of System Parameters
t_{REC} < 38ms
$\overline{t_{REC}}$ > 30ms
t_{ID} < 38ms
t_{DO} > 20ms

*T_P = The continuous presence of a valid tone pair.
T_A = The continuous absence of a valid tone pair.

Fig. 6 - Typical System Timing Constraints

possible the use of DTMF receiver technology in many new application areas.

The analog functions implemented in today's hybrids (e.g. differential front end with sensitivity control; agc for wide dynamic range) are also susceptible to integration using the analog capabilities of the ISO²-CMOS technology. Future developments will therefore be able to place more and more of this analog circuitry onto the chip, for an even more compact receiver solution.

This development constitutes the last of five DTMF receiver generations:

I. LC, PLL and active filter receivers.

II. MOS/LSI detector chip receivers.

III. Hybrid self-contained receivers.

IV. Two-chip CMOS receivers.

V. Single-chip CMOS receivers.

The dividends of this progression are well-known today:

- better performance;
- higher reliability;
- smaller system size;
- lower system cost.

While the single-chip receiver may be said to complete in a sense the evolution of the DTMF receiver, this marks the starting point for even more complex subsystem components, both hybrids and monolithic integrated circuits, of which the DTMF receiver function represents only a building-block. Such components, in common with other areas in which VLSI is used to its limits, will necessarily be

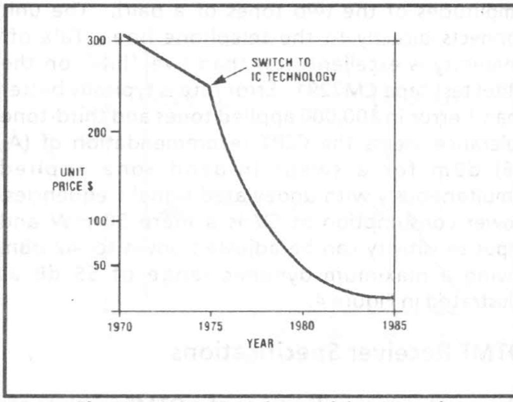


Fig. 7 - DTMF Receiver Pricing Trends

highly specialized to the intended application (e.g. mobile radio, remote control receivers, data receivers, etc.).

Pricing Trends

The telephone operating companies have accelerated the conversion of their equipment to tone dialing. The reason for this is that, apart from the added reliability and convenience of DTMF signalling, the cost of DTMF installation is quickly amortized by the additional revenue available on a DTMF line. Advances in design and the adoption of MOS/LSI has driven the price lower every year. Actual numbers have been used to generate the price curve shown in Figure 7. Future pricing is predicated on advances in technology and pricing trends in both the telecommunications and the semiconductor industries.

According to this curve, a sub-$10 receiver is already projected for 1985, even though inflation is working in the opposite direction. And to stress the point, we are referring to a finished and testing product in a single compact package.

Four main factors account for this phenomenon:

1. Increase in competition between DTMF receiver manufacturers.

2. Switch to MOS/LSI technology, thus taking advantage of semiconductor pricing curves.

3. Acceptance by the telephone companies of newer technologies and reduction of the procurement cycle.

4. Emergence of new applications for DTMF signalling.

An Alternative to Modems?

The emerging new application areas for DTMF signalling deserve some special consideration, as it is these applications which are today being stimulated by the cost-effectiveness of the DTMF approach, and which will in turn benefit as growing volume pushes receivers further down the pricing curve.

Today, DTMF receivers are found primarily in central office and PABX equipment, where the two primary applications are in the receiver proper and in tone-to-pulse converters (Figure 8). Diminishing costs are now permitting the use of receivers at the subscriber end of the installation, transforming the standard voice channel into an economical means of data transmission. The attractiveness of this approach lies in the fact that data may be entered through any standard (DTMF) telephone keypad, eliminating the need for modems, acoustic couplers and other specialized interfacing equipment. Without specialized subscriber equipment, DTMF data transmission is one-way only, and has limited transmission speed and character-set compared to modem solutions, but many applications exist where these shortcomings do not impose a limitation on system performance. Such applications would be characterized as requiring only numeric data (plus possibly the 2 to 6 extra codes embodied in the DTMF specification); as requiring only a moderate data rate (e.g. when data entry speed is limited by speed of operator input); and as being either 'one-way' or else susceptible to some alternative means of data reception (such as achieved by voice synthesis). Many applications of this sort are emerging in fields extending well beyond the telecommunications industry itself.

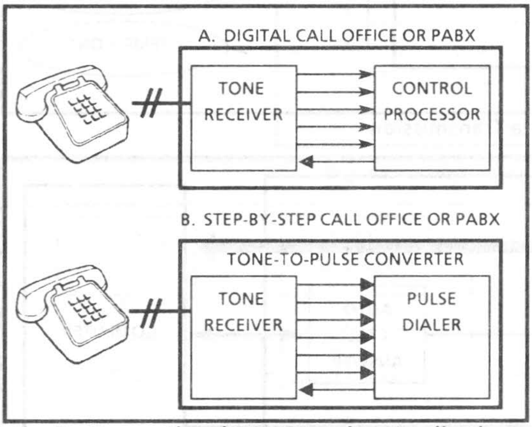


Fig. 8 - Conventional DTMF Receiver Applications

New DTMF Receiver Applications

DTMF technology lends itself to a variety of remote-control applications, in the home (control of heating, appliances, pay-television, etc.) and in industry (control of remotely located installations such as data-loggers, radio transmitters, pumping stations, etc.). The only added expense is at the controlled location (auto-answer, receiver, security logic and controller); the controlling location may be any DTMF telephone, including call-boxes and radiotelephones. Certain of these remote-control applications also benefit from the low power consumption of CMOS technology.Remote data-entry is an application which benefits from the concept of data input through any telephone. For example, a salesman on the road may enter his orders directly into a central computer from any remote location without specialized portable equipment, eliminating equipment and maintenance costs and enhancing user convenience. All that is required is a DTMF receiver installation at the central computer, with the appropriate interface software. A similar application might allow an individual to order goods via his telephone keypad.

Remote-control and data-entry are both applications requiring essentially 'one-way' data transmission (Figure 9), although some audible response would normally be implemented to confirm to the user that correct data has been entered. A more sophisticated approach (Figure 10) must be taken where the called location is required to give a more detailed response. This concept is typified by an application such as credit card verification, where a central computer must provide a confirmation number in response to a keyed-in card number. The obvious solution is voice-synthesis, which maintains the cost and convenience advantage of eliminating specialized equipment at the point of sale. This technology may also bring some of the functions of today's 'electronic bank tellers' directly into the home, again without adding subscriber equipment.

One of the installations which may conveniently be controlled from a remote telephone is the answering machine. The user may command replay of messages and update his own recorded message at will. The machine may also be programmed to store messages intended for specific callers only and activated by a pre-arranged code keyed in by the caller. An economical all-solid-state answering machine may follow the concept of storing a 'follow-me' telephone number updated remotely through DTMF signalling and played back to callers via voice synthesis.

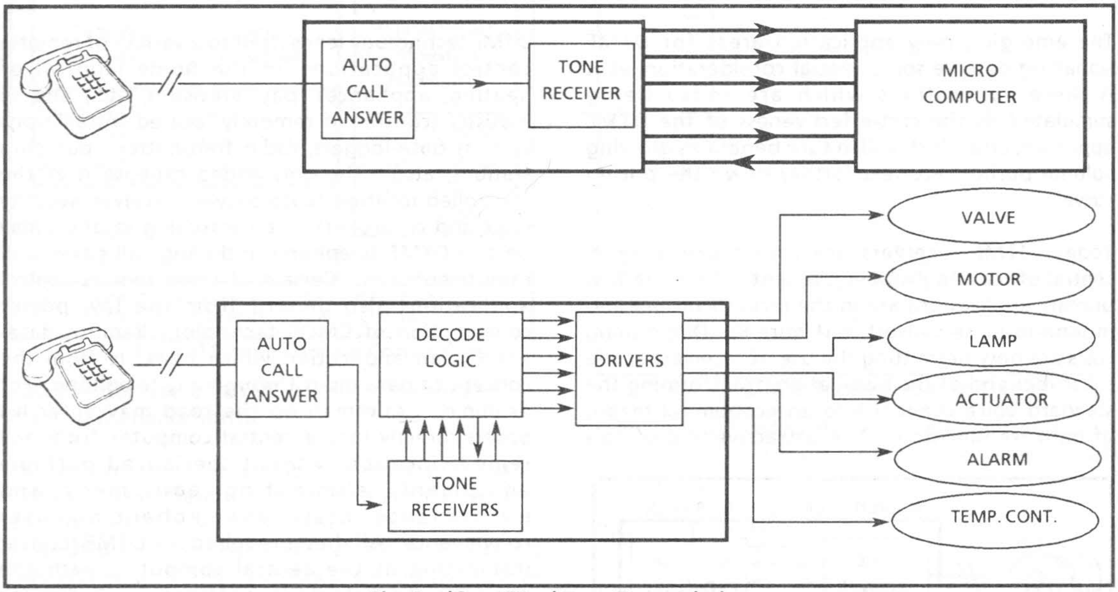


Fig. 9 - 'One-Way' Data Transmission

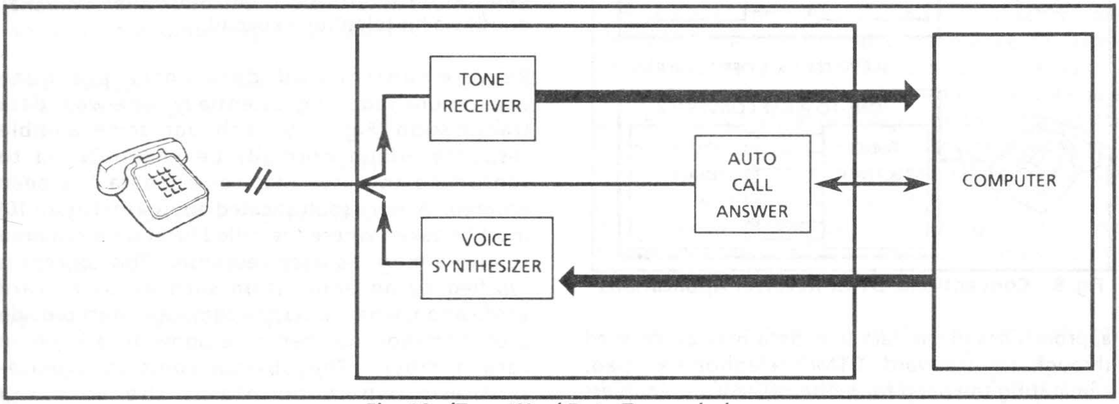


Fig. 10 - 'Two-Way' Data Transmission

One of the more exciting of domestic applications is the home communications system, which brings together telephones, intercom, appliance control, answering machine and home computer in one integrated network. Accessing such a system from any remote telephone clearly adds flexibility to the concept, and might even be applicable to two-way communication between home-computers.

Although some of the major benefits of DTMF signalling stem from an extension of the utility of existing telephone installations, its proven reliability and low cost allow it to be used in any multiple-location signalling network (Figure 11) such as might be found in industrial control systems. The system does not necessarily have any interface to the telephone network but has similar requirements in that it must operate reliably over long distances in the presence of noise and other disturbances. In such an off-line network, the designer has the flexibility to adjust signalling parameters such as tone durations and amplitudes, to conform to his specific application needs.

DTMF signalling is also being extended into mobile-radiotelephone applications (Figure 12). This allows the radio link to 'plug-in' transparently to the telephone network, simplifying the interface, and the same DTMF encoding may be used to transmit channel and other information to and from the mobile installation. Noise and talk-off considerations are rather different in radiotelephone networks, and adjustment of timing parameters can be made to optimize performance in this environment.

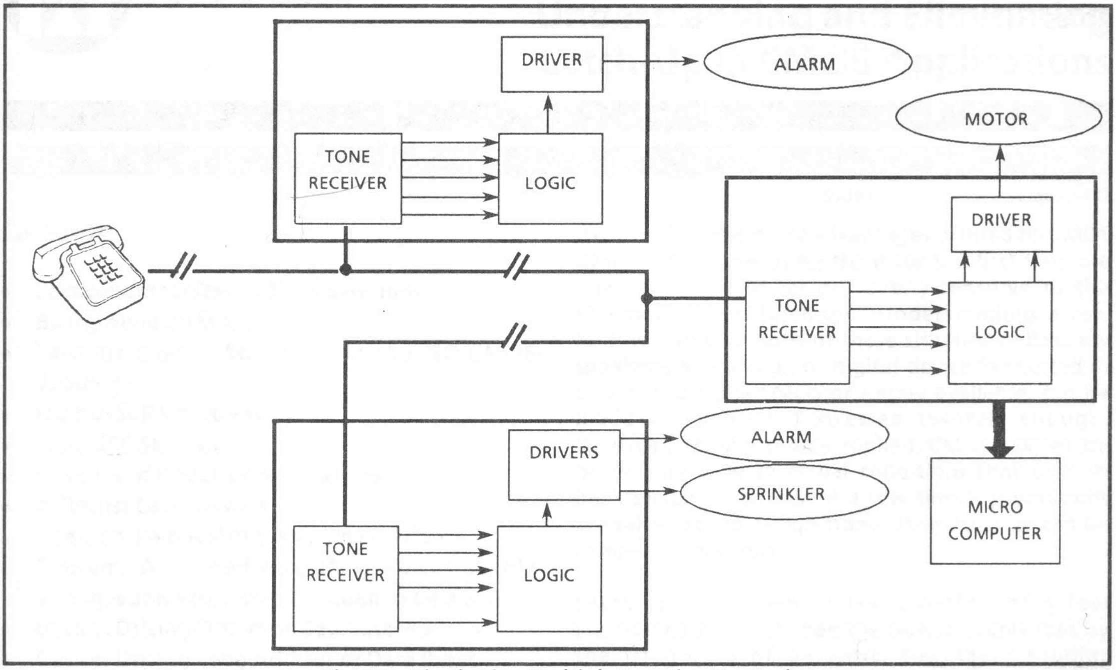


Fig. 11 - Single Line Multiple Location Control

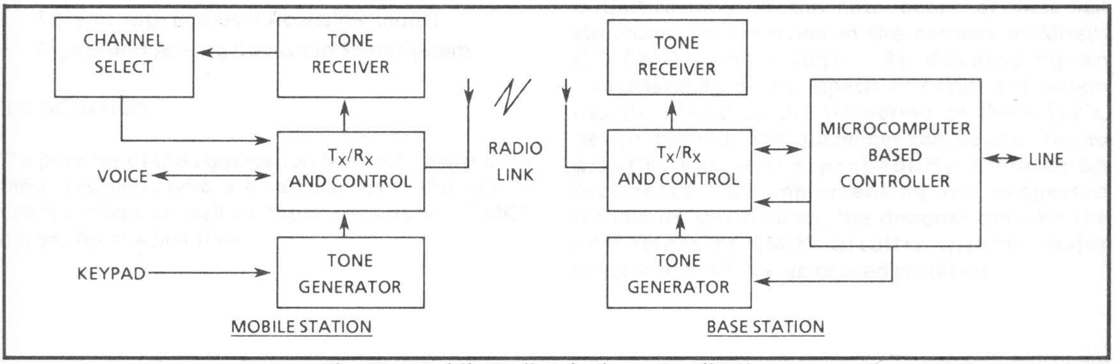


Fig. 12 - Mobile Radiotelephone Applications

Conclusion

A description of the DTMF signalling medium has illustrated its main features both for conventional dialing applications and for certain data transmission and remote control applications. An overview of the "state-of-the-art" as illustrated by the Mitel DTMF receivers has shown the benefits of performance, cost and size which are now available.

Usage of DTMF signalling is enjoying an explosive growth driven primarily by three interacting factors:

1. Increased cost-effectiveness due to LSI implementation.

2. General availability of an input medium (the subscribers telephone).

3. Existence of complementary technologies (such as voice-synthesis).

It remains to be seen what other new applications will be stimulated by the availability of the DTMF signalling medium.

NOTES:

MITEL®

Application Note MSAN-107

Understanding and Eliminating Latch-Up in CMOS Applications

ISSUE 1 August 1982

Contents

Introduction

The purpose of this Application Note is to assist both those designers who are familiar with the use of CMOS devices as well as those considering CMOS designs for the first time.

Attracted by the many advantages offered by CMOS devices, designers using them for the first time are often unaware of, or are overly sensitive to the phenomenom of latch-up. Understanding a few facts will resolve both of these situations. Basically speaking, any analog or digital device fabricated in one of the many CMOS processes available, can be made to latch-up if stressed severely enough. However, when properly applied, CMOS devices are quite insensitive to actual conditions that exist in most systems. Further, if a few simple precautions are taken at the design stage, then latch-up can be completely avoided.

Latch-up is defined as the creation of a low impedance path between the power supply rails by the triggering of parasitic, four-layer bipolar structures (SCR's) inherent in CMOS input and output circuitry. In this note, details of these SCR structures are examined in the context of Mitel's ISO-CMOS technology. By developing an understanding of the aspects of circuit and system design related to the triggering of these SCR's, design methods and guidelines can be acquired to greatly reduce the probability of latch-up occurrence. By implementing the suggested techniques and circuitry, the designer can gain the advantages of CMOS circuitry without major concern about latch-up related problems.

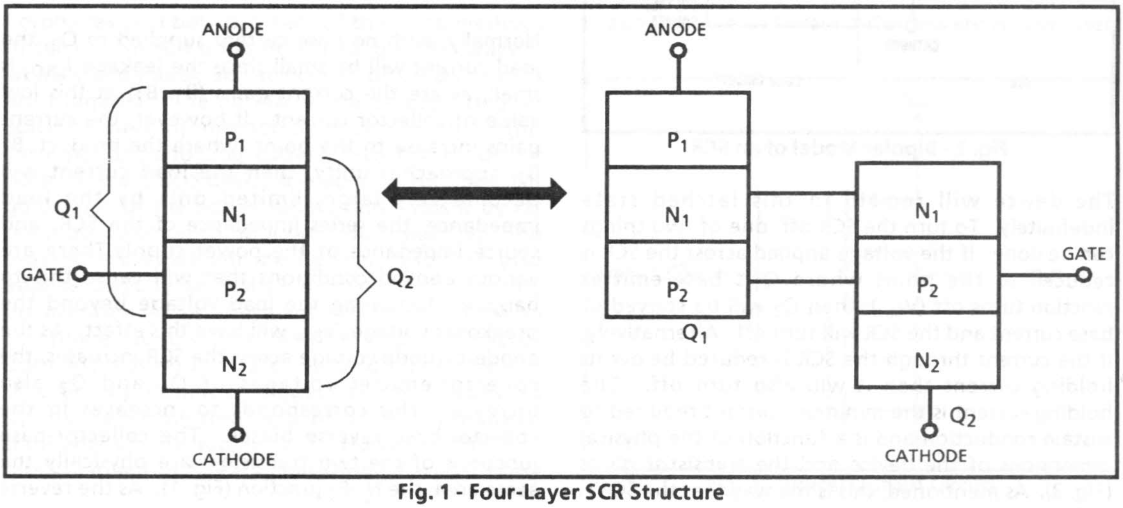


Fig. 1 - Four-Layer SCR Structure

Semiconductor Device Considerations

Background on SCR's

Prior to discussing latch-up in CMOS devices, it is advantageous to briefly review the basic theory of SCR operation. This will be helpful in developing an understanding of the relationships between external circuit and system conditions and the resultant triggerng of latch-up in CMOS devices. The basic SCR structure is that of a four-layer device as shown in Fig. 1. The device has three terminals: Anode, Cathode and Gate. Fig. 2 shows how the SCR can be modelled with two bipolar transistors, one NPN and one PNP. In the normal mode of operation, the SCR is turned on by injecting sufficient current into the base of Q_2 to turn this transistor on. When this is done, Q_2 begins to draw collector current via the base-emitter junction of Q_1. As a result Q_1 also turns on, injecting additional current into Q_2's base. This in turn causes Q_2 to turn on harder, supplying more base current to Q_1. This positive feedback arrangement sustains conduction, and ensures that the SCR continues to conduct even if the gate current is interrupted.

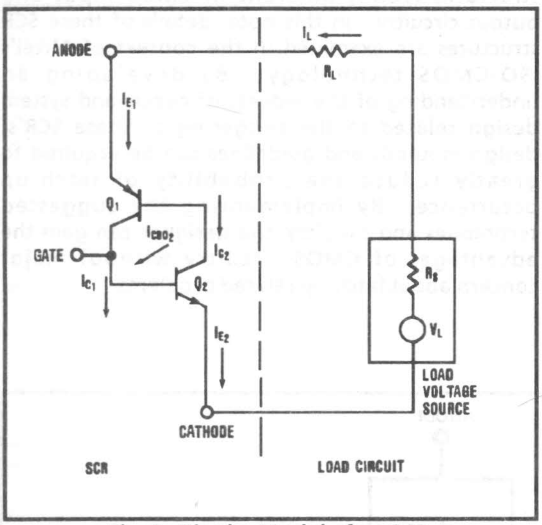


Fig. 2 - Bipolar Model of an SCR

The device will remain in this latched state indefinitely. To turn the SCR off, one of two things can be done. If the voltage applied across the SCR is reduced to the point where Q_1's base-emitter junction turns off (V_{Sus}), then Q_2 will be starved of base current and the SCR will turn off. Alternatively, if the current through the SCR is reduced below its holding current then it will also turn off. The holding current is the minimum current required to sustain conduction and is a function of the physical dimensions of the device and the transistor gains (Fig. 3). As mentioned, this is the way that the SCR is controlled in normal applications. There are various other ways that an SCR may be triggered. These must be examined as they are directly related to latch-up problems.

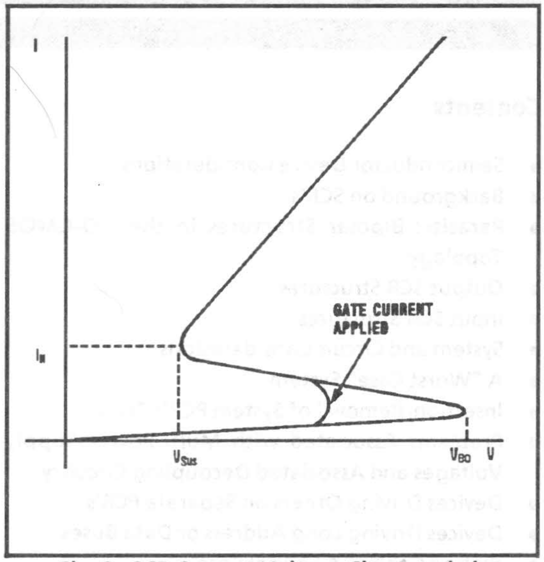


Fig. 3 - SCR Current-Voltage Characteristic

Looking at Fig. 2, it can be seen that the load current and the two emitter currents of Q_1 and Q_2 are all equal. Also the load current is equal to the sums of the two collector currents and a leakage current from Q_2's collector to its base (I_{CBO_2}). It can be shown (refer to Appendix) that:

$$I_L = I_{CBO_2}\left[\frac{(1+B_1)(1+B_2)}{(1-B_1B_2)}\right] \quad (1)$$

Where B_1 and B_2 are the current gains of Q_1 and Q_2 respectively.

Normally, with no base current supplied to Q_2, the load current will be small since the leakage I_{CBO_2} is small, as are the current gains (B_1, B_2) at this low value of collector current. If however, the current gains increase to the point where the product, $B_1 B_2$, approaches unity, then the load current will become very large, limited only by the load impedance, the series impedance of the SCR, and source impedance of the power supply.There are various applied conditions that will cause this to happen. Increasing the load voltage beyond the breakover voltage, V_{BO}, will have this effect. As the anode-cathode voltage across the SCR increases, the collector-emitter voltages of Q_1 and Q_2 also increase. This corresponds to increases in the collector-base reverse biases. The collector-base junctions of the two transistors are physically the same area, the N_1-P_2 junction (Fig. 1). As the reverse

bias increases, the energy of the minority carriers increases causing more carriers to be dislodged, which in turn pick up energy. This continues until the junction undergoes an avalanche breakdown resulting in an increase in the collector currents of Q_1 and Q_2. The resulting increase in B_1 and B_2 cause the SCR to latch on.

A very rapid change in the anode to cathode voltage of an SCR can also cause it to trigger. This is known as the "dV/dt" effect. The N_1-P_2 junction, being reversed biased, exhibits a capacitance. This capacitance varies with the reverse bias voltage applied across the junction. Hence the current through the capacitor is described by:

$$\frac{d(C_j V_{AK})}{dt} \quad (2)$$

$$= \frac{C_j \, dV_{AK}}{dt} + \frac{V_{AK} \, dC_j}{dt} \quad (3)$$

The junction capacitance, C_j decreases with increasing reverse bias and hence the second term of equation (3) is negative. If, however, the rate of change of applied voltage is large enough, the first term of equation (3) will dominate and the current through the SCR will increase. If the current increases sufficiently to cause the B_1B_2 product to approach unity, then the SCR will latch on.

The effects of temperature must also be noted at this point. Increasing temperature will cause an increase in both the leakage current through the SCR and in the current gains B_1 B_2 of the two bipolar transistors. As such, the magnitude of the driving force required to turn the SCR on will decrease with increasing temperature. In other words, the SCR will be more easily triggered as temperature increases for any of the triggering mechanisms described.

Corollaries exist between each of the three methods of turning an SCR on as described, and the ways in which the parasitic SCR structures of CMOS devices are triggered. The normal mode of triggering an SCR is by injecting current into its gate terminal. This corresponds to forcing current into the inputs or outputs of a CMOS device by applying voltages that go outside of the power supply rails. This is by far the most common form of latch-up triggering. The avalanche breakdown mechanism described also applies directly to CMOS devices, although its occurrence is far less prevelant. Excessive voltage on the power supply pins, whether continuous or transient, may result in latch-up occurrence. It is also theoretically possible to trigger parasitic SCR devices by the dV/dt method as a result of high speed transients on the supply rails. However, this will rarely happen in a real application. Each of these triggering methods will be examined in the next section in the context of the ISO-CMOS topology for both the output and input structures.

Parasitic Bipolar Structures in the ISO-CMOS Topology

As with any CMOS technology, ISO-CMOS contains certain parasitic bipolar structures associated with its output devices and input protection circuitry. These parasitic transistors are interconnected in such a way as to form four-layer devices. As such, SCR devices are present at both the inputs and outputs of ISO-CMOS circuits. These devices are normally in their off state and will remain off as long as the absolute maximum ratings of the devices are not exceeded.

Output SCR Structures

A typical ISO-CMOS output driver contains one N-channel MOSFET with its source tied to V_{SS} and one P-channel MOSFET with its source tied to V_{DD}. The drains of the two transistors are connected together to form the output and the gates are commoned to form the input (Fig. 4). The fabrication of these transistors in close proximity results in the formation of a parasitic SCR connected directly across the power supply rails. When triggered, this SCR presents a low impedance to the power supply causing excessive current to flow. This situation is potentially destructive, resulting in damage to bond wires or metal supply tracks on the die due to localized overheating. The SCR is formed as follows. A vertical NPN transistor results from the fabrication of the N-channel device. The N- substrate serves as the collector and is biased at V_{DD}. The P- well acts as the base and the source and drain N- diffusions are the emitters of the transistor. One emitter is tied to V_{SS} and the other to the output. A wide base lateral PNP transistor is formed when a P-channel device is located close to a N-channel transistor. The P-channel source and drain diffusions are two emitters

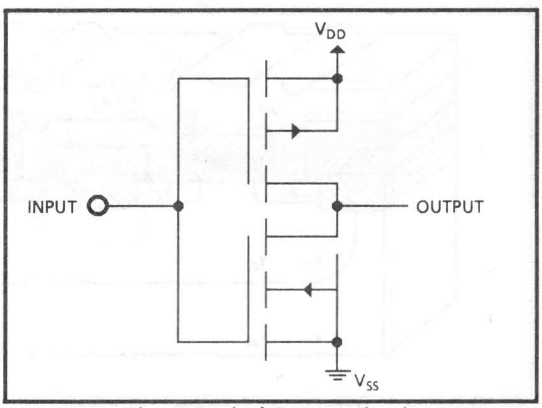


Fig. 4 -Typical Output Circuit

of the transistor: one tied to V_{DD} and the other to the output. The N- substrate acts as the base and hence, is in common with the collector of the vertical NPN. The P- well is the collector of the PNP which is also base of the NPN. Due to the shared diffusions, the vertical NPN and lateral PNP transistors are effectively connected as an SCR (Fig. 5). This parasitic SCR is connected directly across the supply rails. Hence, when triggered, it can cause excessive current to flow. The SCR is normally turned off for nominal operating supply voltages and with all output voltages within the power supply limits. This SCR may be externally triggered causing the output structure to latch-up. The triggering mechanism can be any one of those mentioned in the previous section.

Output voltages being forced outside of the power supply limits is the most common cause of output latch-up. Two parameters are defined at this point for use in subsequent discussions. These are I_{LU} and V_{LU}. I_{LU} is the current which must flow through the output structure to cause latch-up to occur. V_{LU} is the voltage excursion outside of the power supply rails at the output pin that results in I_{LU} flowing through the output structure. In other words I_{LU} and V_{LU} are the conditions at the output pin that will result in latch-up triggering. These same parameters also apply to input latch-up (see next section). Consider first an output voltage which goes below V_{SS} by more than V_{LU}. This causes the P-well to output base-emitter junction of the vertical NPN transistor to become forward biased. Since this acts as the SCR gate, triggering occurs. Current is pulled from V_{DD} through the lateral PNP and is injected into the P- well, causing a localized drop across this diffusion. This voltage drop will forward bias the base-emitter junction of the NPN which is referenced to V_{SS}. Once this occurs, latch-up will be sustained and a low impedance path is created from V_{DD} to V_{SS}.

A note must be taken here in regard to the amount of over-voltage required to trigger latch-up. In the above paragraph, it was mentioned that voltages exceeding the supply rails by more than V_{LU} will cause a current I_{LU} to flow and hence trigger latch-up. The guaranteed values quoted in the data sheet are 0.3V and 10mA respectively for these parameters. These limits are used in production testing and hence, appear in the Absolute Maximum Ratings for MITEL devices. In practice, it is more likely to require from 0.6V to 2V of over-voltage and from 50 to several hundred milliamps of current to cause output latch-up to occur. For input latch-up to occur, it can take several volts of over-voltage and similar currents to induce latch-up due to the series resistance of the input protection circuitry (Fig. 6).

When the V_{DD} supply rail is exceeded by a voltage greater than V_{LU}, a similar set of events occurs. In this case, the output to substrate base-emitter junction of the lateral PNP becomes forward biased. Collector current from this transistors injected into the P- well, again causing a lateral voltage drop. This voltage drop causes the P- well to V_{SS} referenced base-emitter junction of the NPN to become forward biased. This transistor's collector current, pulled from the substrate, causes a lateral voltage drop across the substrate. This voltage drop, in turn, will forward bias the V_{DD} to substrate base-emitter junction of the PNP. Thus, latch-up will be sustained even if the output over-voltage condition is removed and a low impedance path again exists between V_{DD} and V_{SS}.

There are two other causes of output latch-up that are less likely to occur, but nonetheless must be noted. The first of these is the result of over-voltages on the power supply pins. Excessive voltage between V_{DD} and V_{SS} (i.e., greater than the absolute maximum rating) can cause an avalanche breakdown of the reverse biased substrate to P- well collector base junction of the bipolar transistors.

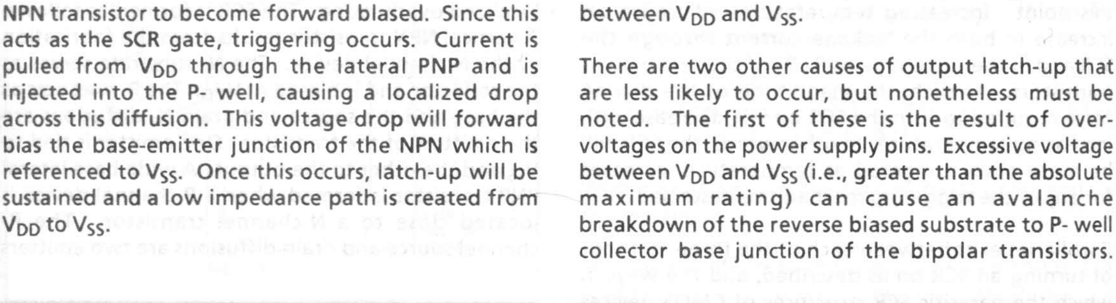


Fig. 5 - Output SCR Structures

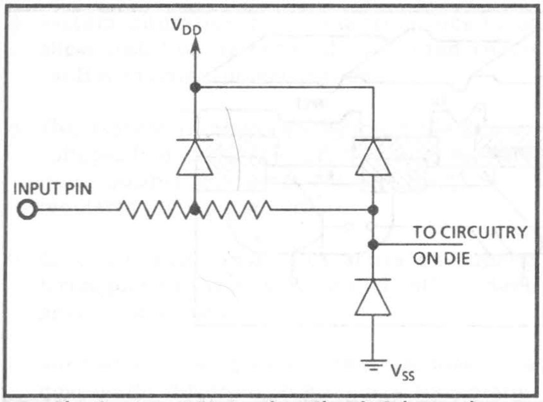


Fig. 6 - Input Protection Circuit Schematic

This will cause the SCR to trigger as outlined in the previous section. The second triggering mechanism will be apparent in very few systems. Very fast voltage spikes on the power supply rails can induce a "dV/dt" triggering of the SCR, also as outlined earlier. This can potentially result in circuit damage by transients which in themselves would not have sufficient energy to cause damage due to localized power dissipation. Once triggered, the SCR may remain latched on until the supply voltage is reduced below its sustaining voltage or if the current is reduced below its holding current.

Input SCR Structures

Parasitic SCR structures can also result due to the fabrication of CMOS input protection circuitry. The ISO-CMOS input protection circuit schematic is shown in Fig. 6. As shown, there is a distributed diode connected to V_{DD} and another diode to V_{SS}. The series resistor is primarily intended for static protection, but also provides latch-up protection. The diodes are connected together at the input node. An SCR structure results when the V_{DD} referenced diode is fabricated in close proximity to an N-channel transistor (Fig. 7) or when the V_{SS} referenced diode is located close to a P-channel device. (Fig. 8).

It is important to note here the difference between input and output SCR structures. The output SCR was connected directly between V_{DD} and V_{SS}, and hence, is more likely to be destructive once triggered. The input SCR structure is connected from the input node to one of the supply rails. Thus, for an input to remain latched, the circuitry driving the input must be capable of supplying the sustaining current of the SCR. For this latch-up to be destructive, the input driver must be capable of supplying large amounts of current. A potentially more dangerous situation occurs when a complimentary transistor, to the one forming the SCR, is located nearby. A secondary SCR structure results from this and it is connected across the supply rails (Figs. 7 and 8).

Consider the V_{SS} referenced diode situation first. The source and drain diffusions of the P-channel transistor form the emitters of a lateral PNP transistor. The substrate acts as the base and the P-diffusion of the diode is the collector. This diode, with the substrate, forms a vertical NPN transistor. The two transistors are interconnected as an SCR due to common diffusion areas. If an applied input voltage is below V_{SS} by more than V_{LU}, then the gate-cathode junction of the SCR will become forward biased and turn the SCR on. This latch-up condition will continue as long as this input condition persists or if the input circuitry can supply the minimum holding current. As mentioned, a potentially more hazardous situation can develop if an N-channel transistor is also located nearby. The P-well of this transistor serves as a second collector of the lateral PNP transistor. When the input voltage goes negative, the gate of the SCR is turned on as mentioned. However, this second collector now injects current into the P- well causing a second

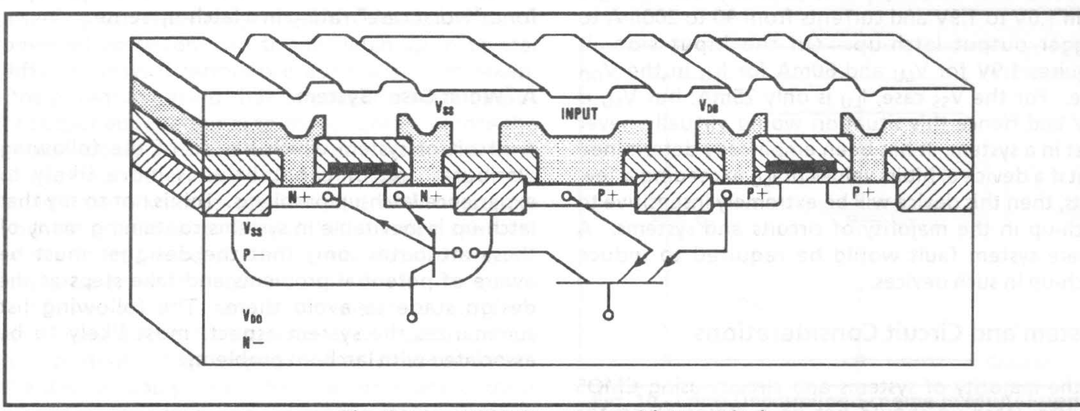


Fig. 7 - Input SCR Structure with V_{DD} Diode

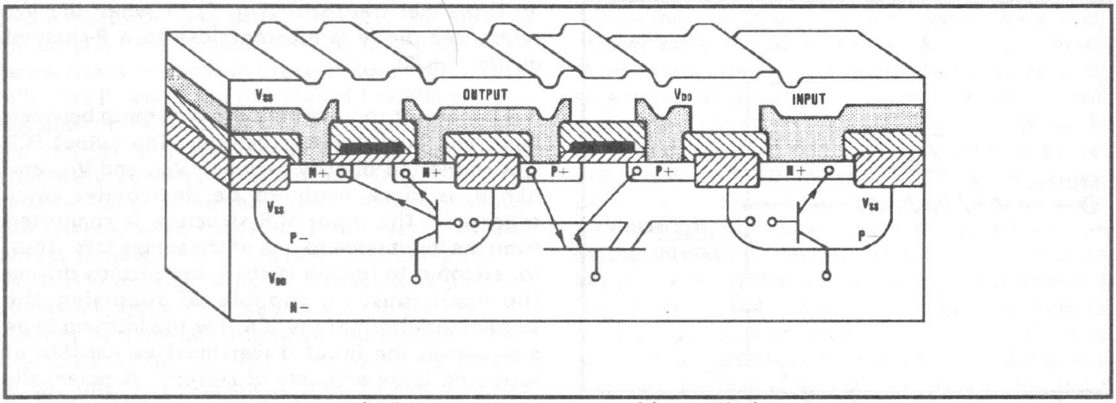


Fig. 8 Input SCR Structure with V_{SS} Diode

Forced I/O Condition	Latch-Up Inducing Conditions	
	V_{LU} (Volts)	I_{LU} (mA)
Outputs above V_{DD}	1.9	200
Outputs below V_{SS}	1.0	90
Inputs above V_{DD}	1.9	80
Inputs below V_{SS}	25.0	25

Table 1 - MD74SC540AC Latch-up Inducing Voltages and Currents

SCR structure to latch on. This device is connected across the power supply rails and hence, can be destructive. This same situation can result with the V_{DD} referenced protection diode. In this case, SCR structures will be triggered by voltages which exceed V_{DD} by more than V_{LU}.

As was mentioned earlier, the actual values of V_{LU} and I_{LU} are typically much greater than the 0.3V and 10mA limits on the data sheets. Table 1 shows some of the numbers pertaining to the current production version of the MD74SC540AC, one of MITEL's Octal Interface devices. As can be seen it requires voltages from 1.0V to 1.9V and currents from 90 to 200mA to trigger output latch-up. On the input side, it requires 1.9V for V_{LU} and 80mA for I_{LU} in the V_{DD} case. For the V_{SS} case, I_{LU} is only 25mA, but V_{LU} is 25V and hence this situation would virtually never exist in a system. It has been empirically determined that if a device exhibits values of I_{LU} exceeding a few volts, then this device will be extremely insensitive to latch-up in the majority of circuits and systems. A severe system fault would be required to induce latch-up in such devices.

System and Circuit Considerations

In the majority of systems and circuits using CMOS devices, latch-up should not be a major cause for concern. Being aware of the sources of latch-up problems will aid the designer in even further reducing the probability of latch-up damage to his circuits. Implementing some of the precautionary measures suggested in the following sections will ensure a trouble-free system.

The aspects of system and circuit design that can result in latch-up occurrence will be examined in the context of a "worst case" system example. In other words, systems containing combinations of the attributes of the example system will be more likely to experience latch-up problems. The relationships between these systems aspects and the resultant latch-up triggering mechanisms will be described. Suggestions will be made intent upon reducing the risk of triggering the parasitic SCR's through careful design techniques. The protection circuits, which will be illustrated, should help in preventing circuit damage in case latch-up occurs. It should be noted at this point, that in systems where the input and output pins of the CMOS devices never go outside of the power supply rails either during power-up or in continuous operation, latch-up is not likely to ever occcur. The first step, then, is to define a system which contains various components that qualify it for a "worst case" rating in a latch-up sense.

A "Worst Case" System

A circuit or system which has all of the following attributes and/or capabilities is more likely to experience latch-up problems. This is not to say that latch-up is inevitable in systems containing many of these attributes, only that the designer must be aware of potential problems and take steps at the design stage to avoid them. The following list summarizes the system aspects most likely to be associated with latch-up problems:

1) System operation/maintenance procedures allow insertion or removal of printed circuit cards with system power applied.

2) The system is powered by multiple supply voltages (e.g. ± 12V, + 5V, and Gnd) or has a multi-supply at same voltage (e.g. +5V regulated, +5V unregulated).

3) Circuits utilize complex capactive decoupling techniques particularly associated with multiple power supply voltages.

4) Integrated circuits on one system PCB drive other devices on different PCB's via a backplane, ribbon cable, etc.

5) Devices drive high capacitive loads such as long data or address busses.

6) System contains high speed address and/or data buses of sufficient length to cause their inductive properties to become significant at the frequencies in question (ribbon cables are a prime example).

7) System has electronic inputs that are directly accessible by the end user of the system.

8) Digital devices are driven from analog devices powered from higher supply voltages, utilizing input diodes for clamping.

Each of the above entries will now be examined in terms of its potential for triggering latch-up. The first four items are very interdependent. While each of these will be given consideration in separate sections, cross referencing will be extensive. The remaining items are relatively independent and thus, will be looked at in relative isolation.

Insertion/Removal of System PBC's "Live"

Inserting or removing printed circuit cards from a powered-up system can trigger latch-up in several different ways if certain precautions are not taken. One potential hazard that can occur is for an input or output edge terminal to make contact before the power supply pins are connected. If driven by a device on another circuit card, this input/output pin could have a voltage applied to it with no supply voltage to the device. Even if this situation exists for only a short period of time, then latch-up may be triggered when the power supply pin is connected. It is important to note that three-state outputs are also vulnerable in this situation. Such output drivers only present a high impedance to voltages within the device supply rails. Voltages on these outputs exceeding the supply can indeed trigger latch-up.

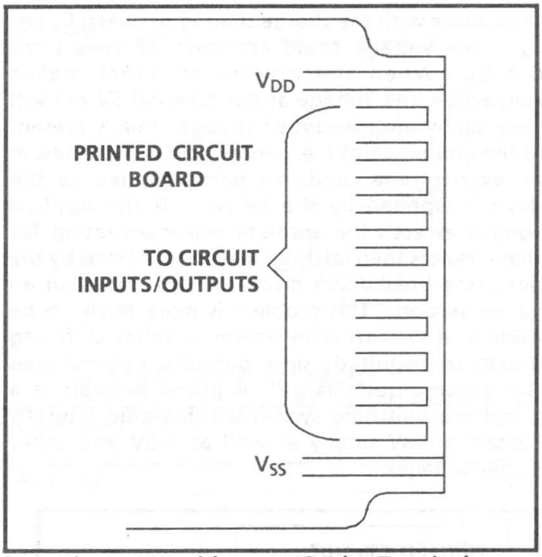


Fig. 9 - PCB with Inset I/O Edge Terminals

One solution to this problem is to slightly extend the power supply terminals with respect to the remaining edge terminals on the PCB (Fig. 9). This will ensure that power supply connections are the first made and last broken on insertion and removal of the PCB respectively.

Plugging a circuit card live into a system with multi-power supply voltages can result in the application of power supply over-voltages to certain devices. Consider the local decoupling scheme shown in Fig. 10. If a PCB containing such decoupling was plugged into a system live, then the following situation could result. Assume that all capacitors are discharged and that C_1 is much greater than C_2. It is possible that when the PCB is inserted, the +12V terminal makes connection first, then the ground, and lastly the +5V connection is made. In this situation, C_1 and C_2 are momentarily connected in series. The +12 volts applied to C_1 causes the voltage at the ground point to increase in

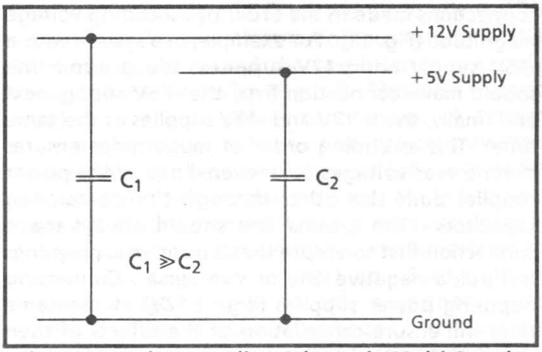


Fig. 10 - Local Decoupling Scheme in Multi-Supply System

accordance with the charge sharing between C_1 anc C_2. This voltage could approach 12 volts since $C_1 \gg C_2$. When the ground terminal makes connection, the voltage at the nominal 5V rail will jump up by the amount of voltage initially present at the ground point (i.e. almost 12V). This results in an over-voltage condition being applied to the devices supplied by the 5V rail. If the applied voltage exceeds the absolute maximum rating for these devices then latch-up may be triggered by the avalanche breakdown mechanism described in an earlier section. This problem is more likely to be evident in systems with power supplies differing greatly in magnitude since potential over-voltages can become quite large. A prime example is a telephone switching system which would typically contain a -48V supply as well as +5V and other supply voltages.

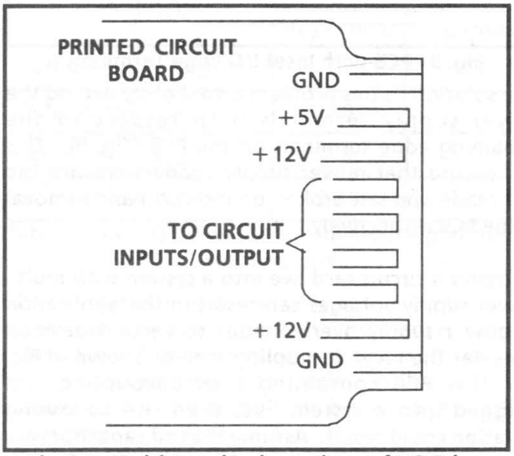


Fig. 11 - Multi-Level Indentations of I/O Edge Terminals

This problem can also be overcome by indenting the edge terminals on PCB's. In this case, there must be more than one level of indentation to ensure that the power supply connections are made in a sequence that will alleviate this problem. The safest way to accomplish this is to have power supply connections made in the order of ascending voltage magnitude (Fig. 11). For example, in a system with a +5V supply and ±12V supplies, the ground line should make connection first, the +5V supply next and finally, the +12V and -12V supplies at the same time. This ascending order of magnitudes ensures that no over-voltages occur even if one of the power supplies pulls the other through the decoupling capacitors. The ground line should always make connection first to ensure that a positive supply does not pull a negative one or vice versa. Connecting opposing power supplies (e.g. ±12V) at the same time will ensure cancellation of the effects of their connection.

In systems which have large number of power supplies to contend with, it may not be feasible to provide the required number of indentations on the PCB. In this case, a careful analysis of the decoupling used must be done to establish potential problem areas. Where possible, decoupling capacitors on different supplies should be of equal magnitude. This will tend to minimize over-voltages dues to equal charge sharing between the capacitors. If after all possible precautions have been taken, there is still a possibility of power supply over-voltages occurring, then it may be necessary to provide some form of current limiting or local regulation to prevent circuit damage.

The simpliest form of protection is to connect a resistor in series with the power supply (V_{DD} or V_{SS}) pin of the devices in question (Fig. 12a). The size of this resistor can be chosen to either prevent latch-up from occurring or to prevent circuit damage when latch-up does occur. If latch-up is to be prevented then the minimum resistor value is chosen as follows:

$$R = \frac{V_{Supply} - V_{DD_{Max}}}{I_{DD_{Max}}}$$

where V_{Supply} = Maximum Supply Voltage Generated

$V_{DD_{Max}}$ = Absolute Maximum Rating for V_{DD}

$I_{DD_{MAX}}$ = Supply Current at $V_{DD_{Max}}$

This will ensure that $V_{DD_{Max}}$ is never exceeded at the device.

To simply prevent damage due to latch-up, the resistor is chosen to limit the supply current to a few hundred milliamps at the maximum applied voltage. There are a few factors which must be taken into consideration when the maximum value for this resistor is selected. The source impedance of the power supply will be increased by the amount of the added resistance. This will result in a decrease in the current sourcing or sinking capacity of the device, depending on whether the resistor is in the V_{DD} or V_{SS} line respectively. There is also a corresponding increase in the output propagation delay, proportional to product of the protection resistor and the load capacitance. Finally there is a decrease in the noise immunity of the device proportional to the product of this resistor and the total instantaneous supply current (including the output currents). For devices such as the MD74SCXXX, it is recommended that this resistor be placed in the V_{DD} line as there is more available noise immunity for

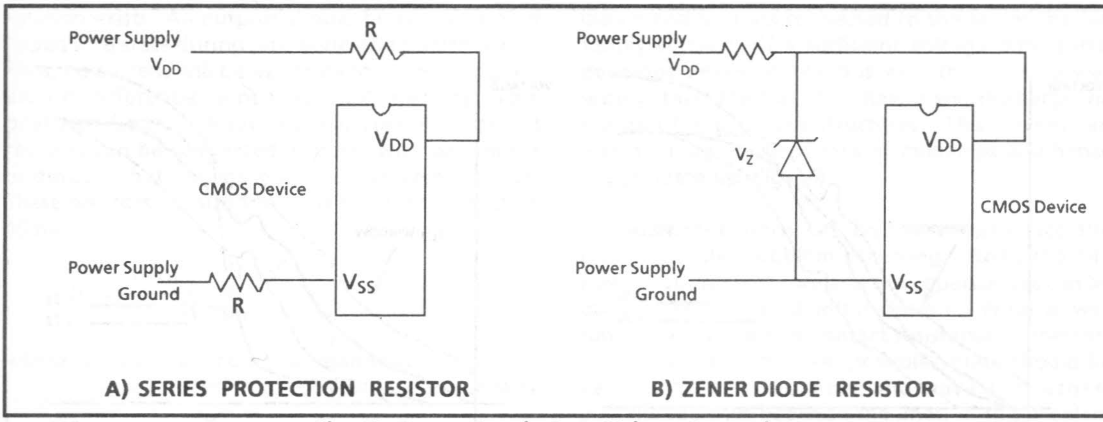


Fig. 12 - Power Supply Over-Voltage Protection

high level outputs (when driving TTL or other MD74SCXXX devices).

If a current-limiting resistor cannot be used due to constraints on output drive, speed or noise immunity, then the alternative is to connect a zener diode between V_{DD} and V_{SS} to prevent over-voltages across the device (Fig. 12b). A current-limiting resistor may still be necessary, but its value can be very small, limited only by the power handling capacity of the zener diode.

There is one last potential hazard that can develop due to "live" insertion of PCB's. On boards with little local decoupling, plugging the card in can result in an extremely fast transient on the power supply leads of devices on the board. These transients could theoretically result in triggering latch-up due to the dV/dt effect described earlier. This problem can be avoided by decoupling the power supply on the board with sufficiently large capacitors to slow down the power supply ramp up when the board is plugged in. These capacitors must be chosen to be compatible with the overall decoupling scheme to prevent the over-voltage problem just described.

Similar transients on the power supply can be generated due to switching of high speed, high current devices such as ECL and Schottky TTL circuits driving heavy DC current loads. Also, back EMF generated by opening of inductive loads such as realys can induce nasty voltage spikes. Adequate high frequency decoupling will usually remedy the problem. A 0.01 to 0.1μF ceramic capacitor connected as close to the device as possible across the power supply pins will shunt most of this high frequency energy to ground (Fig. 13). Connection of flyback diodes around inductive loads is also recommended to limit back EMF surges.

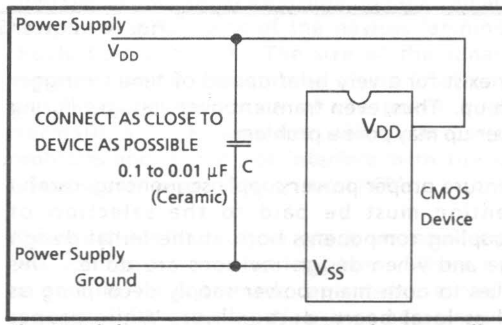


Fig. 13-High Frequency Power Supply Decoupling

Problems Associated with Multi-Power Supply Voltages and Associated Decoupling Circuitry

In systems that have more than one independent power supply, care must be taken to ensure correct sequencing during power-up and power-down cycles. This is required to prevent input and output over-voltage conditions from developing. Consider, for example, a device powered from a +5V supply that has its outputs connected to a device powered from a +7V supply. Under steady state conditions, the output levels from the 5V devices would lie well within the supply voltage of the 7V device. However, if during power-up the 5V supply was to exceed the 7V supply, then the output voltage of the 5V device could exceed the instantaneous supply voltage of the 7V device (Fig. 14). This over-voltage could cause the 7V device to latch-up. A similar situation can occur between two devices powered by separate supplies of equal magnitude such as 5V regulated and 5V unregulated supplies. In this case there is the added concern when three-state outputs are tied together. These outputs are also subject to over-voltage triggering of latch-up. Such outputs present a high impedance only to signals lying within the power supply voltages. It must be stressed that these over-voltage conditions need

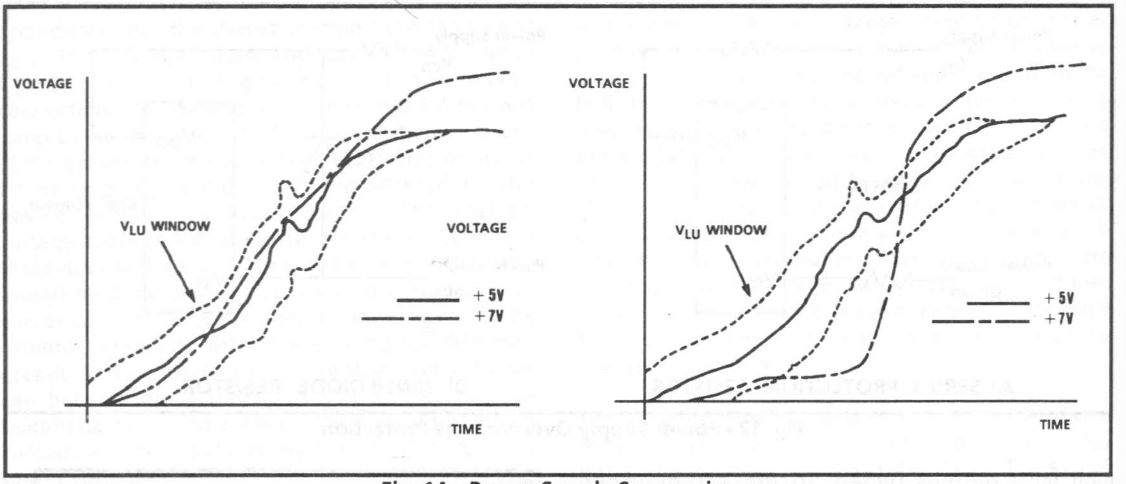


Fig. 14 - Power Supply Sequencing

only exist for a very brief period of time to trigger latch-up. Thus, even transient over-voltages during power-up may pose a problem.

To ensure proper power supply sequencing, careful attention must be paid to the selection of decoupling components both at the initial design stage and when design revisions are done. This applies to both main power supply decoupling as well as local board decoupling. While proper sequencing may be evident at main distribution points, local sequencing can be altered by large capacitors on individual boards. Boards which have a large DC power requirement are likely to have such decoupling and hence, must be looked at carefully.

One way of ensuring that power supplies track when turning on or off is to connect a diode from the lower supply voltage to the higher one in the case of unequal supplies (Fig. 15). This will cause the supplies to track within one diode drop until they attain proper levels. In the case of two equal supplies, two diodes can be connected back to back, forcing supplies to track, independent of which supply comes up first.

Devices Driving Others on Separate PCBs

When integrated circuits in a system drive other devices on separate PCB's (via a backplane for example), then the considerations given in the previous two sections must be applied globally to the system. This was already mentioned in the section on plugging in PCB's "live". That is, when a PCB is plugged into a backplane with the system power applied, there is the danger that an input or output pin will contact an active line on the backplane before the power supply connection is

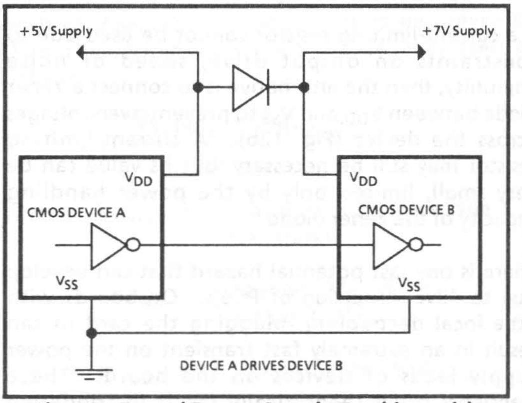


Fig. 15 - Forced Power Supply Tracking with Clamping Diode

made. The solution to this problem, as mentioned, lies in indenting the I/O edge terminations with respect to power supply terminals on the PCB.

Power supply sequencing should be given special attention in systems with devices that drive off-board. The same criteria applies here as was described for multi-supply systems. However, care must also be taken in single supply systems. In this case, large amounts of local decoupling can cause the supply voltages on some boards in the system to ramp up slower than on others. Devices on boards whose power supply ramps up quickly, can impress an over-voltage on devices on other boards. If this over-voltage is large enough, then latch-up may be triggered.

Whenever possible, local decoupling should be equalized on all boards within the system to minimize these effects. In systems where all off-board drivers are three-state devices, a simple

solution exists. All outputs should be kept in a high impedance state during power-up and power-down. Thus, no current will be available to trigger latch-up even if differential supply voltages develop from board to board. Alternatively, current limiting resistors can be connected in series with any inputs or outputs that may be subjected to over-voltages. These resistors are sized to limit current to less than 10mA:

$$R = \frac{(V_{Diff} - 0.3V)}{10mA}$$

where V_{Diff} = maximum instantaneous voltage differential between power supplies

The side effects of connecting these resistors are the same as mentioned previously for power supply over-voltage protection. There will be reductions in current drive from outputs, in speed, and in noise immunity on outputs driving DC loads through these resistors.

Devices Driving Long Address or Data Buses

Long address and data buses can exhibit quite large capacitances. Devices which drive such buses or have their inputs tied to one, can be subjected to over-voltage conditions. This is especially true if large DC current loads are switched on the same PCB (e.g. a group of LED's during a lamp test). Over-voltages can develop as follows. The change in the power supply current causes a localized voltage drop on the supply pins of the devices near to the device drawing the load current. This is a result of the finite resistance of the power supply tracks and contact resistance of any connectors. At the same time, the bus capacitance tends to hold the voltage on the inputs and outputs connected to the bus at the full supply voltage. If a sufficient voltage differential develops between the bus and the local power supply, then the bus capacitance will discharge via the input and output structures. This current can attain a magnitude of tens of milliamps and hence trigger latch-up (Fig. 16).

Various precautions can be taken to reduce the chances of this problem occurring. Reducing the power supply resistance and bus capacitances can be done at the time of inital design. Wide power supply tracks and low contact resistance connectors should be used whenever possible. Buses should be kept as short as possible and have the largest possible spacings between the lines. If this problem still results due to system restraints on PCB layout, then the connection of a decoupling capacitor across the power supply pins of the devices latching-up should help (Fig. 17). The size of the capacitor depends upon the magnitude of the local current and the local resistance of the power supply. Normally a 10µF capacitor will clear up such problems and should not interfere with the local power supply sequencing on most PCB's.

There is one other way in which an input/output over-voltage can occur on long buses. There exists, on such buses, intertrack capacitance as well as capacitance to ground. When two adjacent tracks are at opposite logic levels (one at 5V, the other at ground), this capacitance charges to the full supply voltage. When the track initially at ground potential suddenly goes high, the signal is coupled through the capacitor to the other track. The voltage on this track increases from its initial value of 5V, impressing over-voltages on any devices connected to this track.

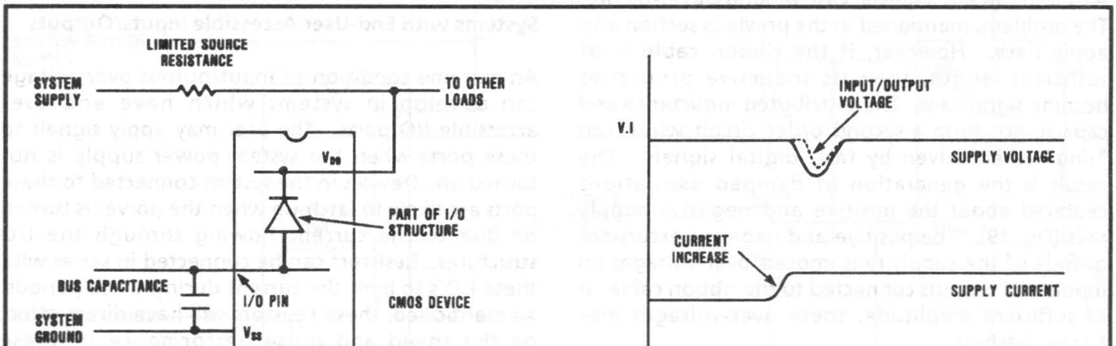


Fig. 16 - Effects of Switching DC Loads Combined with Large Bus Capacitors

Minimizing intertrack capacitance by interleaving signal and ground tracks should be done wherever board space permits. Alternatively, external clamping diodes can be connected on tracks exhibiting these voltage excursions. The diodes may need be Schottky diodes if regular ones do not clamp soon enough toprevent current flow through

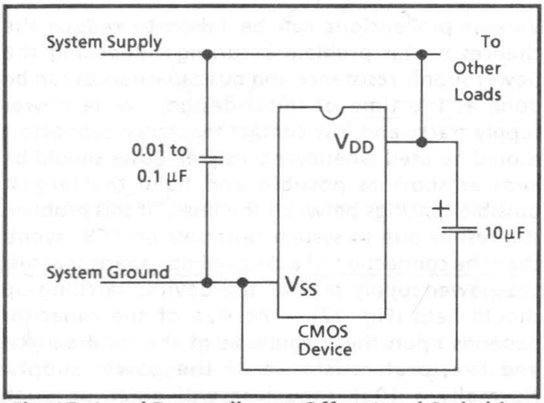


Fig. 17- Local Decoupling to Offset Load Switching Effects

I/O structures. Regular silicon diodes may still be used if they are referenced to voltages inset by 0.7V from the supply rails. The clamping circuit shown in Fig. 18 should be quite effective, but as can be seen, this circuit will dissipate power. This may or may not be a problem depending on the overall system requirements. The decoupling capacitors help to absorb the high frequency energy. The resistor values shown are selected for a 5V supply and should be scaled for other supply voltages.

Ribbon Cables - A Special Case

A ribbon cable is a special case of long bus structure. The problems mentioned in the previous section also apply here. However, if the ribbon cable is of sufficient length, then its inductive properties become significant. The distributed inductance and capacitance form a second order circuit which can "ring" when driven by fast, digital signals. The result is the generation of damped oscillations centered about the positive and negative supply rails (Fig. 19). The positive and negative excursions outside of the supply rails impress over-voltages on inputs and outputs connected to the ribbon cable. If of sufficient amplitude, these over-voltages may trigger latch-up.

Solving the problem can be as simple as terminating each end of such cables with resistors to reduce the ringing voltages. However, these resistors will dissipate extra power. An alternative is to connect external protection diodes as shown in Fig. 20.

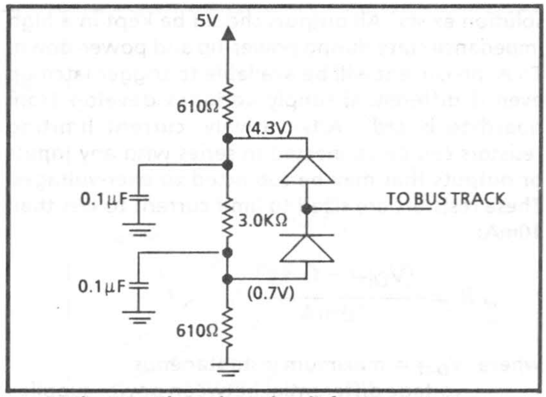


Fig. 18 - Clamping Circuit for Long Buses

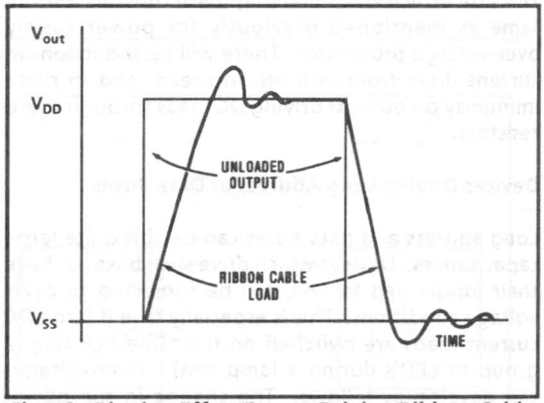


Fig. 19 - Ringing Effect Due to Driving Ribbon Cable

These diodes will clamp any generated over-voltages. If the problem persists, it may be necessary to use Schottky diodes to ensure that the external diodes conduct before the input/output structures do.

Systems with End-User Accessible Inputs/Outputs

An extreme condition of input/output over-voltage can develop in systems which have end user accessible I/O ports. The user may apply signals to these ports when the system power supply is not turned on. Devices in the system connected to these ports are likely to latch-up when the power is turned on due to the current flowing through the I/O structures. Resistors can be connected in series with these I/O's to limit the current during these periods. As mentioned, these resistors will have direct effect on the speed and noise performance of these ports.Latch-up may also be triggered if the end user applies voltages to the I/O ports which exceed the system power supply voltages. The protection resistors suggested above may provide adequate protection against this hazard as well. However, performance constraints on the port may be such

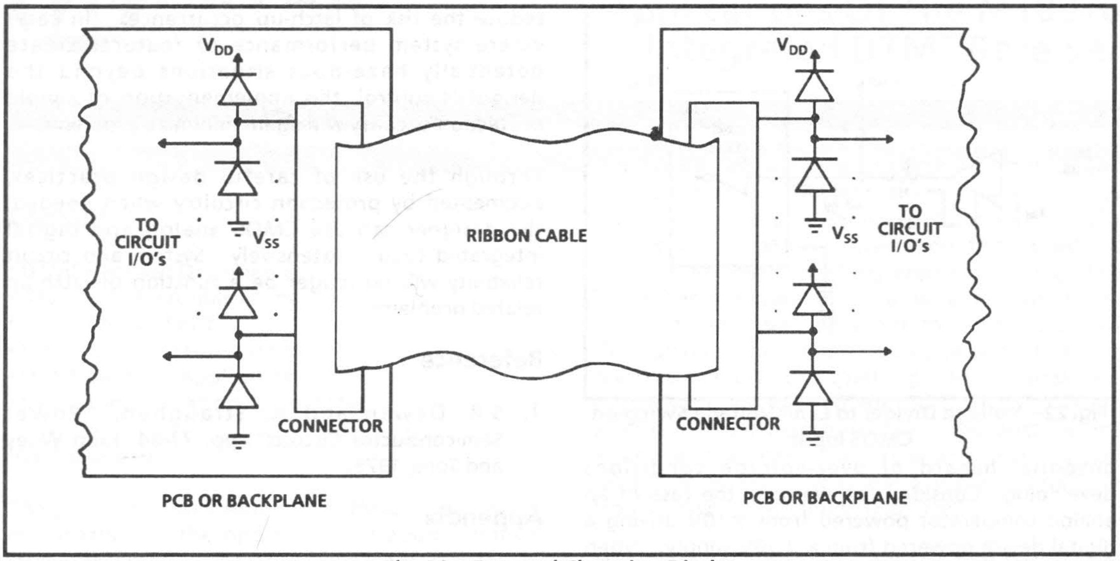


Fig. 20 - External Clamping Diodes

that the current-limiting resistors chosen are too small to protect against severe faults such as accidental connection of the AC mains supply. Protection against such faults can be provided by connection of external clamping diodes in the manner outlined for ribbon cables. Again, Schottky diodes may be required.

If fault conditions are likely to be very severe, it may be necessary to reference external clamping diodes to voltages inset by 0.7V from the power supply (Fig. 21). These diodes will conduct before the input/output structures of the device on the port whenever an over-voltage condition exists. Thus, no current will flow to trigger latch-up. The reference voltages are inset by 0.7V to allow the use of regular, low-cost diodes. Due to the potentially large currents flowing through the protection diodes, a clamping circuit similar to the one in Fig. 18 is not feasible. The output resistance in this case needs to be substantially lower.

Digital and Analog Devices in Same System

In systems which have digital and analog devices powered by different supply voltages, there is the

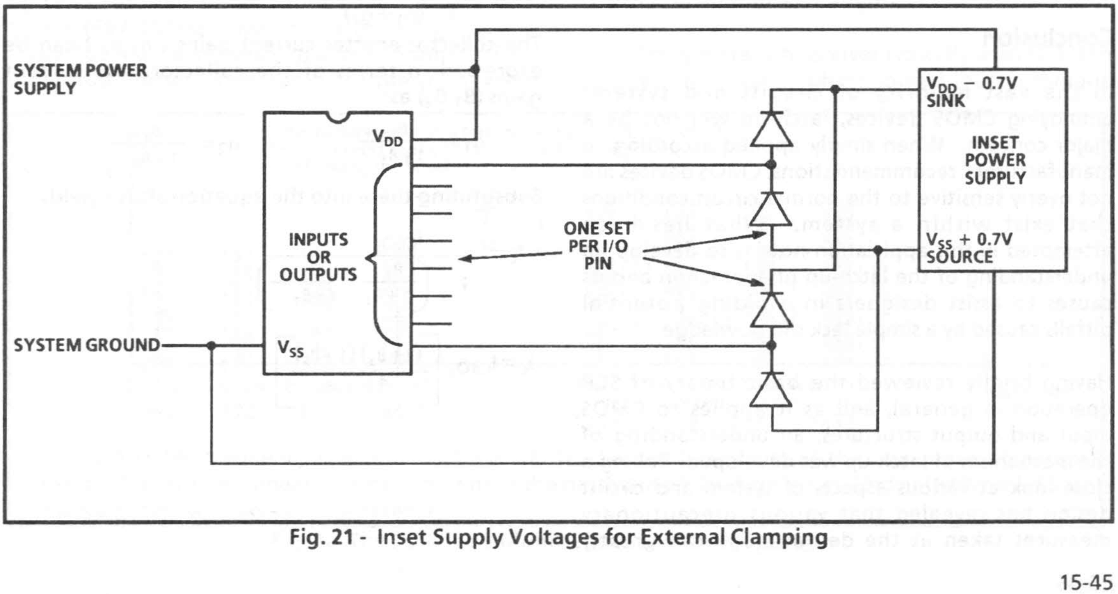


Fig. 21 - Inset Supply Voltages for External Clamping

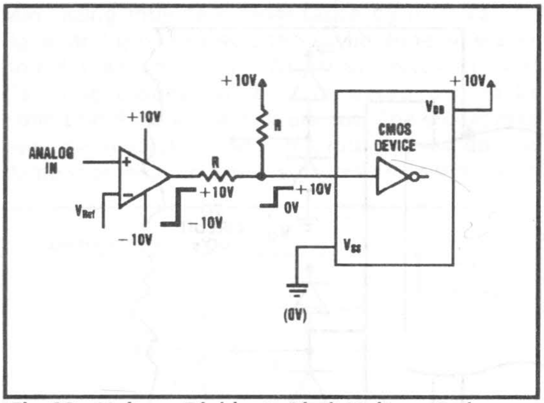


Fig. 22 - Voltage Divider to Limit Voltage Swing on CMOS Input

potential hazard of over-voltage conditions developing. Consider, for example, the case of an analog comparator powered from ±10V driving a digital device powered from a +10V supply. When the comparator output goes low, it will approach -10V and pull the digital input below V_{SS} (0V). If the comparator can pull enough current, then latch-up may be triggered. Putting a resistor in series with the input will limit the current and prevent latch-up. However, it is not a recommended procedure to use the input diodes as clamping circuits. A more advisable solution is to use a resistive divider as shown in Fig. 22. When the comparator output goes low, the divider will have 20V across it. Half of this voltage will be dropped across each resistor so that the digital input sits at 0V. When the comparator output goes high, no current flows through the divider so that the digital input sits at V_{DD}. Since the CMOS input has an extremely high input impedance, the value of these resistors can be very large (>100K) to minimize power consumption.

Conclusion

In the vast majority of circuits and systems employing CMOS devices, latch-up will not be a major concern. When simply applied according to manufacturers' recommendations, CMOS devices are not overly sensitive to the normal circuit conditions that exist within a system. What has been attempted in this application note is to develop an understanding of the latch-up phenomenon and its causes to assist designers in avoiding potential pitfalls caused by a simple lack of knowledge.

Having briefly reviewed the basic theory of SCR operation in general, and as it applies to CMOS input and output structures, an understanding of the mechanism of latch-up was developed. Taking a close look at various aspects of system and circuit design has revealed that various precautionary measures taken at the design stage can greatly reduce the risk of latch-up occurrences. In cases where system performance or features create potentially hazardous situations beyond the designer's control, the implementation of simple protection circuitry will again minimize problems.

Through the use of careful design practices, augmented by protection circuitry when needed, the designer can use CMOS analog and digital integrated circuits extensively. System and circuit reliability will no longer be a function of latch-up related problems.

Reference

1. S.B. Dewan and A. Straughen, "Power Semiconductor Circuits", pp. 77-84, John Wiley and Sons, 1975.

Appendix

The following is a derivation of equation (1) of the main text. Fig. 2 is referenced for this purpose.

The collector and emitter currents of Q_1 and Q_2 are related by:

$$i_{C_1} = \alpha_1 i_{E_1} \qquad i_{C_2} = \alpha_2 i_{E_2}$$

Looking at Fig. 2, it can be seen that the load current and the emitter currents of Q1 and Q2 are all equal. Also the load current is equal to the sums of the two collector currents and a leakage current from Q_2's collector to its base (I_{CBO_2}). Therefore:

$$\begin{aligned} I_L &= i_{C_1} + i_{C_2} + I_{CBO_2} \\ &= \alpha_1 i_{E_1} + \alpha_2 i_{E_2} + I_{CBO_2} \\ &= (\alpha_1 + \alpha_2) I_L + I_{CBO_2} \\ &= \frac{I_{CBO_2}}{1-(\alpha_1+\alpha_2)} \end{aligned}$$

The collector-emitter current gains (α_1, α_2) can be expressed in terms of the collector-base current gains (B_1, B_2) as:

$$\alpha_1 = \frac{B_1}{1+B_1} \qquad \alpha_2 = \frac{B_2}{1+B_2}$$

Substituting these into the equation above yields:

$$I_L = \frac{I_{CBO_2}}{1 - \left(\frac{B_1}{1+B_1} + \frac{B_2}{1+B_2}\right)}$$

$$I_L = I_{CBO_2}\left[\frac{(1+B_1)(1+B_2)}{1-B_1B_2}\right]$$

MITEL®

Application Note MSAN-108
Applications Of The MT8870 Integrated DTMF Receiver

9161-001-002-NA ISSUE 1 JUNE 1983

Contents

Introduction

The purpose of this Application Note is to provide information on the operation and application of DTMF Receivers. The MT8870 Integrated DTMF Receiver will be discussed in detail and its use illustrated in the application examples which follow.

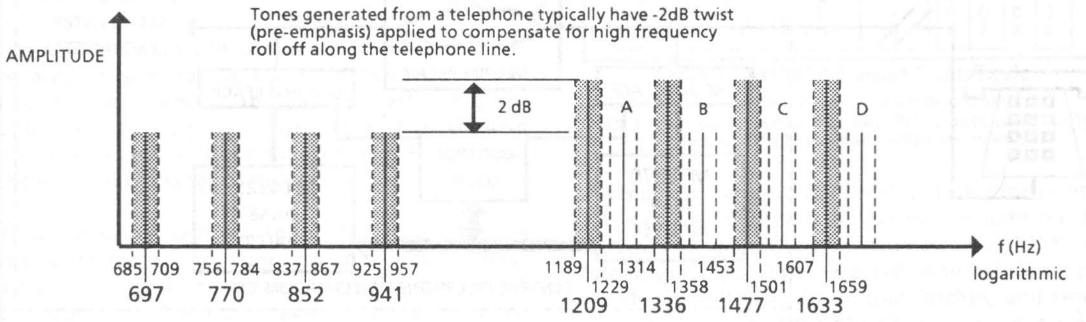
More than 25 years ago the need for an improved method for transferring dialling information through the telephone network was recognized. The traditional method, Dial pulse signalling, was not only slow, suffering severe distortion over long wire loops, but required a DC path through the communications channel. A signalling scheme was developed utilizing voice frequency tones and implemented as a very reliable alternative to pulse dialling. This scheme is known as DTMF (Dual Tone Multi-Frequency), Touch-Tone™ or simply, tone dialling. As its acronym suggests, a valid DTMF signal is the sum of two tones, one from a low group (697-941Hz) and one from a high group (1209-1633Hz) with each group containing four individual tones. The tone frequencies were carefully chosen such that they are not harmonically related and that their intermodulation products result in minimal signalling impairment (Fig. 1a). This scheme allows for 16 unique combinations. Ten of these codes represent the numerals zero through nine, the remaining six (*,#,A,B,C,D) being reserved for special signalling. Most telephone keypads contain ten numeric push buttons plus the asterisk (*) and octothorp (#). The buttons are arranged in a matrix, each selecting its low group tone from its respective row and its high group tone from its respective column (Fig. 1b).

The DTMF coding scheme ensures that each signal contains one and only one component from each of the high and low groups. This significantly simplifies decoding because the composite DTMF signal may be separated with bandpass filters, into its two single frequency components each of which may be handled individually. As a result DTMF coding has proven to provide a flexible signalling scheme of excellent reliability, hence motivating innovative and competitive decoder design.

Development

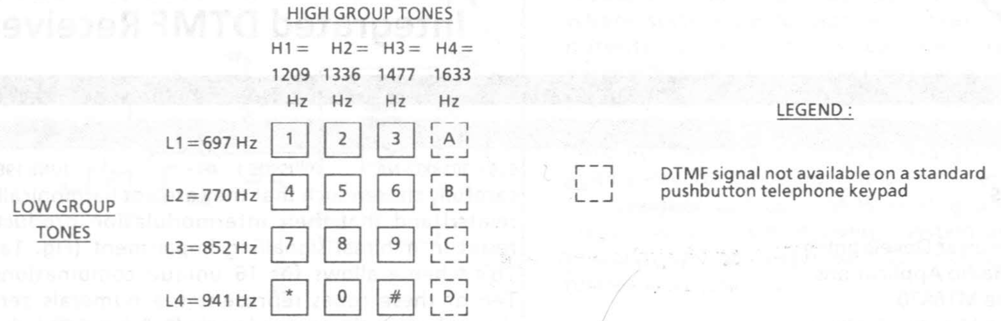
Early DTMF decoders (receivers) utilized banks of bandpass filters making them somewhat cumbersome and expensive to implement. This generally restricted their application to central offices (telephone exchanges).

The first generation receiver typically used LC filters, active filters and/or phase locked loop techniques



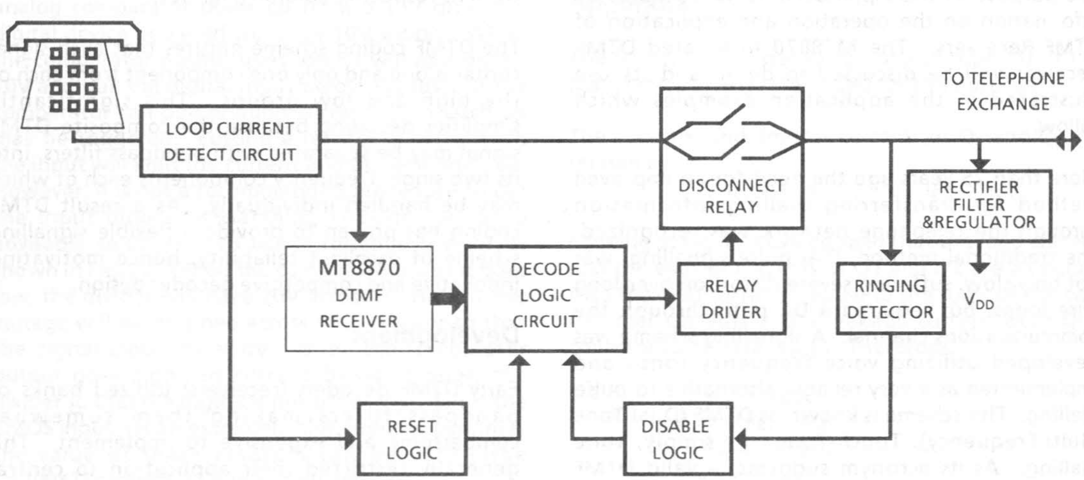
Standard DTMF frequency spectrum ±(1.5% + 2 Hz). Second harmonics of the low group (possibly created due to a non-linear channel) fall within the passband of the high group (Indicated by A,B,C,D). This is a potential source of interference.

Fig. 1a The Dual Tone Multifrequency (DTMF) Spectrum

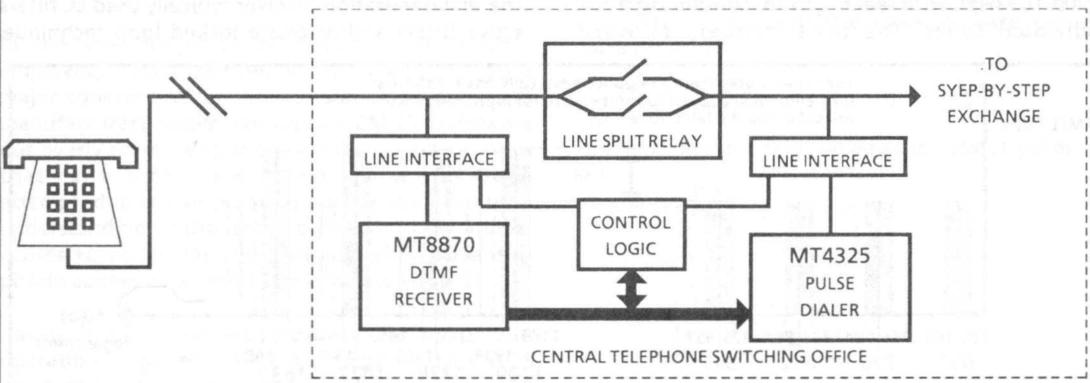


Telephone DTMF keypad matrix. Column H_4 is normally not available on a telephone keypad and is reserved for special signalling.

Fig. 1b The Dual Tone Multifrequency (DTMF) Keypad



(a) Block diagram of a toll call restrictor. This could be implemented on a small pc board and installed in a telephone to disallow long distance calling.



(b) Block diagram of a simple tone to pulse converter to allow TOUCH-TONE™ dialling into a step-by-step or crossbar exchange.

Fig. 2 Typical DTMF Receiver Applications

to receive and decode DTMF tones. Initial functions were, commonly, phone number decoders and toll call restrictors. A DTMF receiver is also frequently used as a building block in a tone-to-pulse converter which allows Touch-Tone™ dialling access to mechanical step-by-step and crossbar exchanges (Fig. 2).

The introduction of MOS/LSI digital techniques brought about the second generation of tone receiver development. These devices were used to digitally decode the two discrete tones that result from decomposition of the composite signal. Two analog bandpass filters were used to perform the decomposition.

Totally self-contained receivers implemented in thick film hybrid technology depicted the start of third generation devices. Typically, they also used analog active filters to bandsplit the composite signal and MOS digital devices to decode the tones.

The development of silicon-implemented switched capacitor sampled filters marked the birth of the fourth and current generation of DTMF receiver technology. Initially single chip bandpass filters were combined with currently available decoders enabling a two chip receiver design. A further advance in integration has merged both functions onto a single chip allowing DTMF receivers to be realized in minimal space at a low cost.

The second and third generation technologies saw a tendency to shift complexity away from the analog circuitry towards the digital LSI circuitry in order to reduce the complexity of analog filters and their inherent problems. Now that the filters themselves can be implemented in silicon, the distribution of complexity becomes more a function of performance and silicon real estate.

Inside The MT8870

P023-13

The MT8870 is a state of the art single chip DTMF receiver incorporating switched capacitor filter technology and an advanced digital counting/averaging algorithm for period measurement. The block diagram (Fig. 3) illustrates the internal workings of this device.

To aid design flexibility, the DTMF input signal is first buffered by an input op-amp which allows adjustment of gain and choice of input configuration. The input stage is followed by a low pass continuous RC active filter which performs an antialiasing function. Dial tone at 350 and 440Hz is then rejected by a third order switched capacitor notch filter. The signal, still in its composite form, is then split into its individual high and low frequency components by two sixth order switched capacitor and pass filters. Each component tone is then smoothed by an output filter and squared up by a hard limiting comparator.

The two resulting rectangular waves are applied to digital circuitry where a counting algorithm measures and averages their periods. An accurate reference clock is derived from an inexpensive external 3.58MHz colourburst crystal.

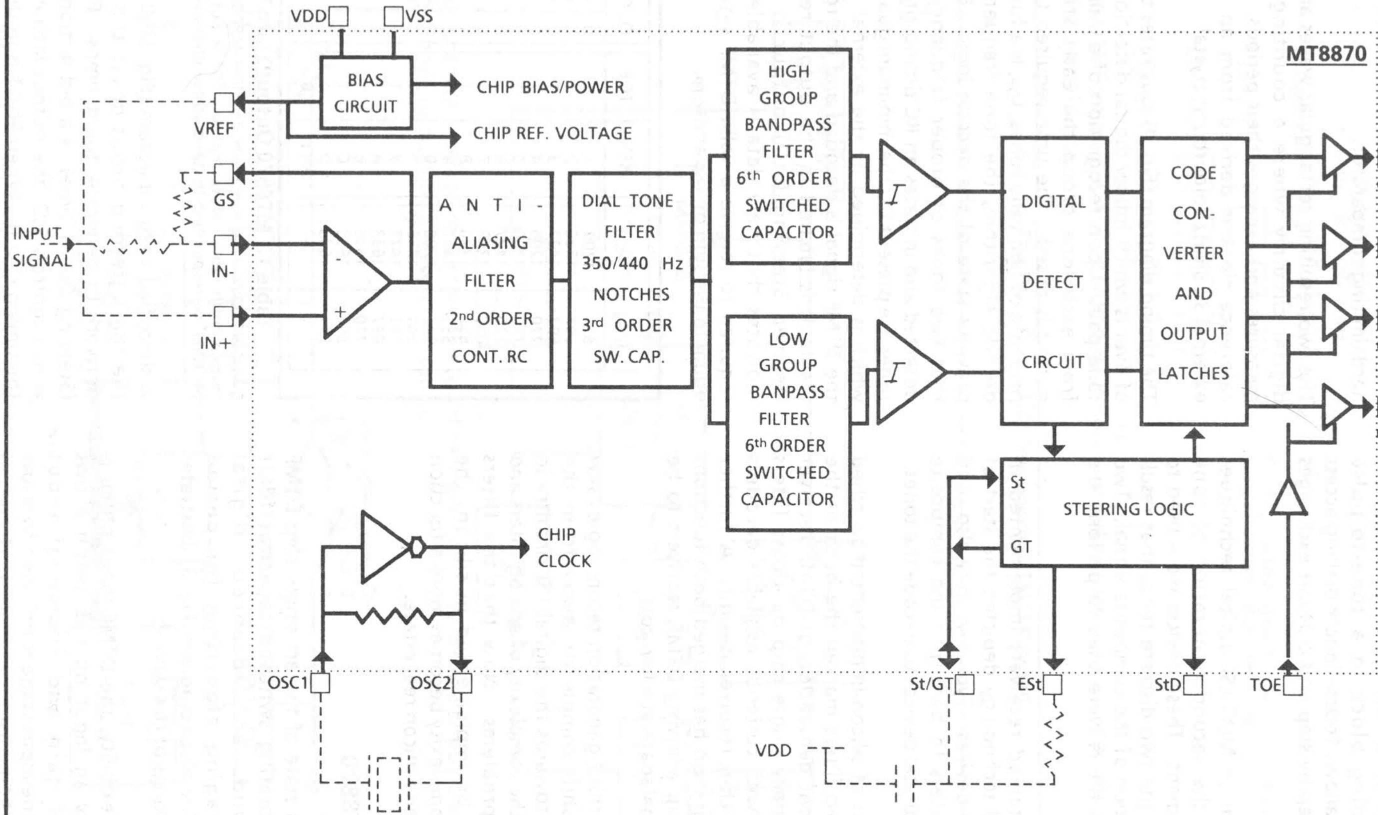
The timing diagram (Fig. 4) illustrates the sequence of events which follow digital detection of a DTMF tone pair. Upon recognition of a valid frequency from each tone group the Early Steering (ESt) output is raised. The time required to detect the presence of two valid tones, t_{DP}, is a function of the decode algorithm, the tone frequency and the previous state of the decode logic. ESt indicates that two tones of proper frequency have been detected and initiates an RC timing circuit. If both tones are present for the minimum guard time, t_{GTP}, which is determined by the external RC network, the DTMF signal is decoded and the resulting data (Table 1) is latched in the output register. The Delayed Steering (StD) output is raised and indicates that new data is available. The time required to receive a valid DTMF signal, t_{REC} , is equal to the sum of t_{DP} andt_{GTP}.

f_{LOW}	f_{HIGH}	KEY	TOE	Q_4	Q_3	Q_2	Q_1
697	1209	1	1	0	0	0	1
697	1336	2	1	0	0	1	0
697	1477	3	1	0	0	1	1
770	1209	4	1	0	1	0	0
770	1336	5	1	0	1	0	1
770	1477	6	1	0	1	1	0
852	1209	7	1	0	1	1	1
852	1336	8	1	1	0	0	0
852	1477	9	1	1	0	0	1
941	1209	0	1	1	0	1	0
941	1336	*	1	1	0	1	1
941	1477	#	1	1	1	0	0
697	1633	A	1	1	1	0	1
770	1633	B	1	1	1	1	0
852	1633	C	1	1	1	1	1
941	1633	D	1	0	0	0	0
-	-	ANY	0	Z	Z	Z	Z

Table 1. MT8870 Output Truth Table

0=LOGIC LOW 1=LOGIC HIGH Z=HIGH IMPEDANCE
Output truth table. Note that key "0" is output as "1010_2 (ie: 10_{10})" corresponding to standard telephony coding.

A simplified circuit diagram (Fig. 5) illustrates how the chip's steering circuit drives the external RC network to generate guard times. Pin 17, St/GT (Steering/Guard Time), is a bidirectional signal pin which controls StD, the output latches, and resets the timing circuit. When St/GT is in its input mode (St function) both Q_1 and Q_2 are turned off and the voltage level at St/GT is compared to the steering threshold voltage V_{TSt}. A transition from below to above V_{TSt} will switch the comparator's output



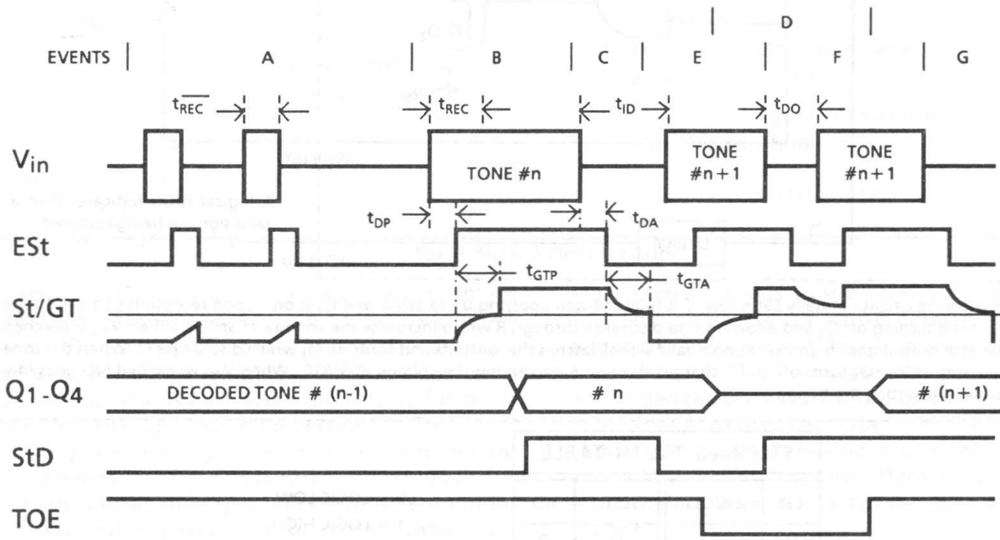
External guard time, input, and clock components (dashed) are included for clarity.

Fig.3 MT8870 Functional Block Diagram

from low to high strobing new data into the output latches, and raising the StD output. As long as an input level above V_{TSt} is maintained StD will remain high indicating the presence of a valid DTMF signal.

Initially, when no valid tone-pairs are present, capacitor C is fully charged applying a low voltage to St/GT. This causes a low at the comparator's output and since ESt is also low, Q_2 turns on ensuring that C is completely charged. In this condition St/GT is in its output mode (GT function). When a valid tone-pair is received ESt is raised turning off Q_2 which puts St/GT in its high impedance input mode and allows C to discharge through R. If this condition persists for the tone-present guard time, t_{GTP}, the voltage at St/GT rises above V_{TSt} raising StD which indicates reception of a valid DTMF signal. If the tone pair drops out before the duration of t_{GTP}, ESt is lowered turning on Q_2 which charges C resetting the tone-present guard time.

Once a DTMF signal is recognized as valid both ESt and the comparator output are high. This turns on Q_1 which discharges C and initializes the tone-absent guard time, t_{GTA}. After the DTMF signal is removed, ESt is lowered, Q_1 turns off placing St/GT in its input mode and C begins to charge through R.



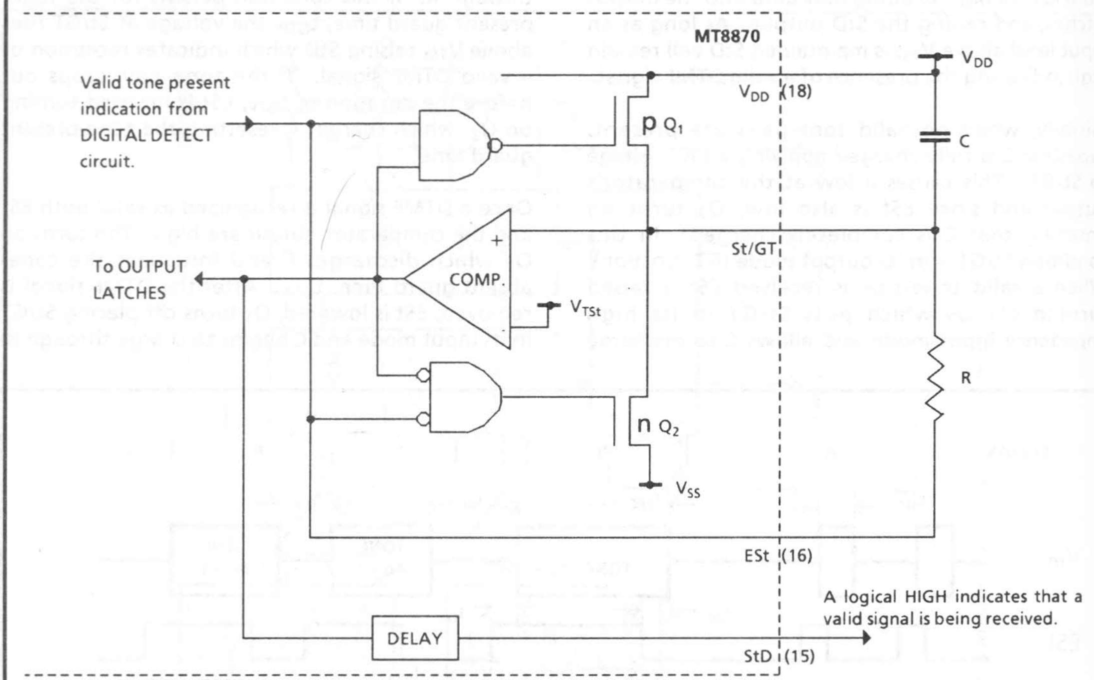
EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED
B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS
C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE
D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE
E) TONE #n+1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE)
F) ACCEPTABLE DROPOUT OF TONE #n+1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED
G) END OF TONE #n+1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL.
ESt	EARLY STEERING OUTPUT. INDICATES DECTECTION OF CORRECT TONE FREQUENCIES.
St/GT	STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
Q_1-Q_4	4-BIT DECODED TONE OUTPUT
StD	DELAYED STEERING OUTPUT. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTE A VALID SIGNAL.
TOE	TONE OUTPUT ENABLE (INPUT). A LOW LEVEL SHIFTS Q_1-Q_4 TO ITS HIGH IMPEDANCE STATE.
$t_{\overline{REC}}$	MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID.
t_{REC}	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.
t_{ID}	MINIMUM TIME BETWEEN VALID SEQUENTIAL DTMF SIGNALS.
t_{DO}	MAXIMUM ALLOWABLE DROPOUT DURING VALID DTMF SIGNAL.
t_{DP}	TIME TO DETECT VALID FREQUENCIES PRESENT.
t_{DA}	TIME TO DETECT VALID FREQUENCIES ABSENT.
t_{GTP}	GUARD TIME, TONE PRESENT.
t_{GTA}	GUARD TIME, TONE ABSENT

Fig. 4 MT8870 Timing Diagram



Simplified steering circuit. Initially ESt is low, C is fully charged applying 0V to St/GT and Q_2 is on. Upon reception of a valid tone pair ESt is raised turning off Q_2 and allowing C to discharge through R which increases the voltage at St/GT. When V_{TSt} is reached the comparator output goes high indicating a valid signal, latches the outputs and turns on Q_1 which discharges C. When the tone pair is lost ESt goes low Q_1 turns off and C charges through R decreasing the voltage at St/GT. When V_{TSt} is reached StD goes low and Q_2 turns on resetting the timing circuit.

STEERING TRUTH TABLE

ESt	St(/GT)	(St/)GT	StD
0	$<V_{TSt}$	0	0
0	$>V_{TSt}$	Z	1
1	$<V_{TSt}$	Z	0
1	$>V_{TSt}$	1	1

0 = LOGIC LOW
1 = LOGIC HIGH
Z = HIGH IMPEDENCE
V_{TSt} = Threshold Voltage (typically 1/2 V_{DD})

Steering circuit truth table. Note that pin 17 (St/GT) acts as both an input and an output depending on the relative states of ESt and the comparator output.

Fig. 5 MT8870 Steering And GuardTime Circuit Operation

If the same valid tone-pair does not reappear before t_{GTA} then the voltage at St/GT falls below V_{TSt} which resets the timing circuit via Q_2 and prepares the device to receive another signal. If the same valid tone-pair reappears before t_{GTA}, ESt is raised turning on Q_1 and discharging C which resets t_{GTA}. In this case StD remains high and the tone dropout is disregarded as noise.

To provide good reliability in a typical telephony environment, a DTMF receiver should be designed to recognize a valid tone-pair greater than 40mS in duration and, to accept as successive digits, tone-pairs that are greater than 40mS apart. However in other environments, such as two-way radio, the optimum tone duration and intra-digit times may differ due to noise considerations.

By adding an extra resistor and steering diode (Fig. 6b, 6c) t_{GTP} and t_{GTA} can be set to different values. Guard time adjustment allows tailoring of noise immunity and talk-off performance to meet specific system needs.

Talk-off is a measure of errors that occur when the receiver falsely detects a tone pair due to speech or background noise simulating a DTMF signal. Increasing t_{GTP} improves talk off performance since

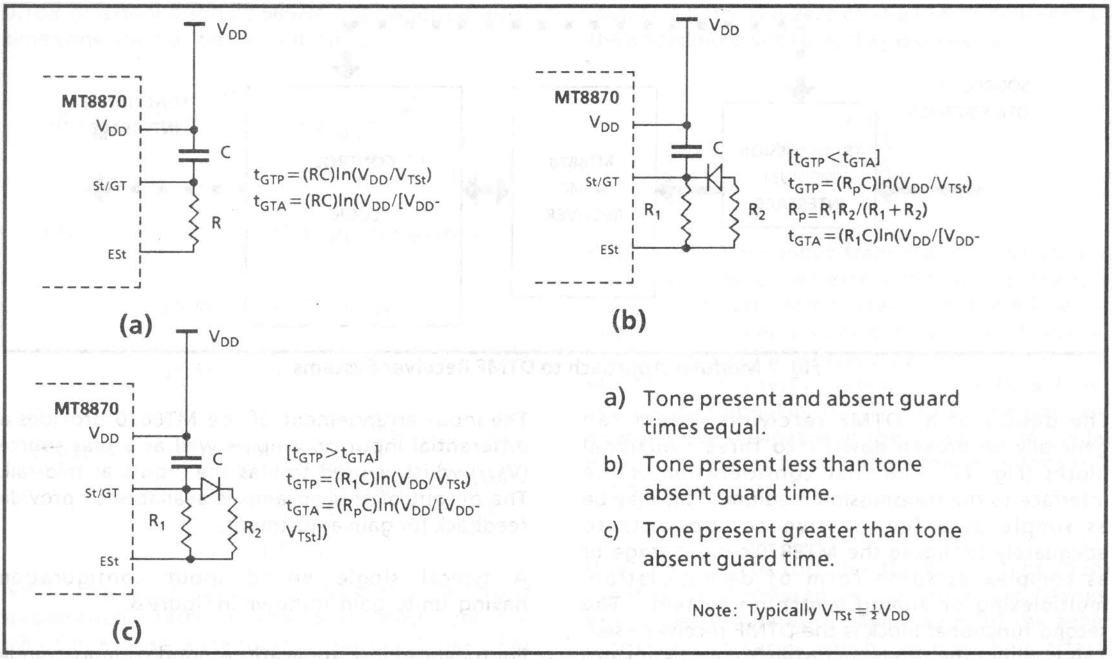


Fig. 6 Guard Time Circuits

it reduces the probability that speech will maintain DTMF simulation long enough to be considered valid. The trade-off here is decreased noise immunity because dropout (longer than t_{DA}) due to noise pulses will restart t_{GTP}. Therefore, for noisy environments, t_{GTP} should be decreased. The signal absent guard time, t_{GTA}, determines the minimum time allowed between successive DTMF signals. A dropout shorter than t_{GTA} will be considered noise and will not register as a successive valid tone detection. This guards against multiple reception of a single character. Therefore, lengthening t_{GTA} will increase noise immunity and tolerance to the presence of an unwanted third tone at the expense of decreasing the maximum signalling rate.

The intricacies of the digital detection algorithm have a significant impact on the overall receiver performance. It is here that the initial decision is made to accept the signal as valid or reject it as speech or noise.

Trade-offs must be made between eliminating talk off errors and eliminating the effects of unwanted third tone signals and noise. These are mutually conflicting events. On one hand valid DTMF signals present in noise must be recognized which requires relaxation of the detection criteria. On the other hand, relaxing the detection criteria increases the probability of receiving "hits" due to talk off errors.

Many considerations must be taken into account in evaluating criteria for noise rejection. In the telephony environment two sources of noise are predominant. These are, third tone interference, which generally comes from dial tone harmonics, and band-limited white noise . In the MT8870 a complex digital averaging algorithm provides excellent immunity to voice, third tone and noise signals which prevail in a typical voice bandwidth channel.

The algorithm used in the MT8870 combines the best features from two previous generations of Mitel digital decoders with improvements resulting from years of practical use within the telephone environment. The algorithm has evolved through a combination of statistical calculations and empirical "tweaks" to result in the realization of an extremely reliable decoder.

Applications

The proven reliability of DTMF signalling has created a vast spectrum of possible applications. Until recently, many of these applications were rendered ineffective due to cost or size considerations. Now that a complete DTMF receiver can be designed with merely a single chip and a few external passive components one can take full advantage of a highly developed signalling scheme as a small, cost-effective signalling solution.

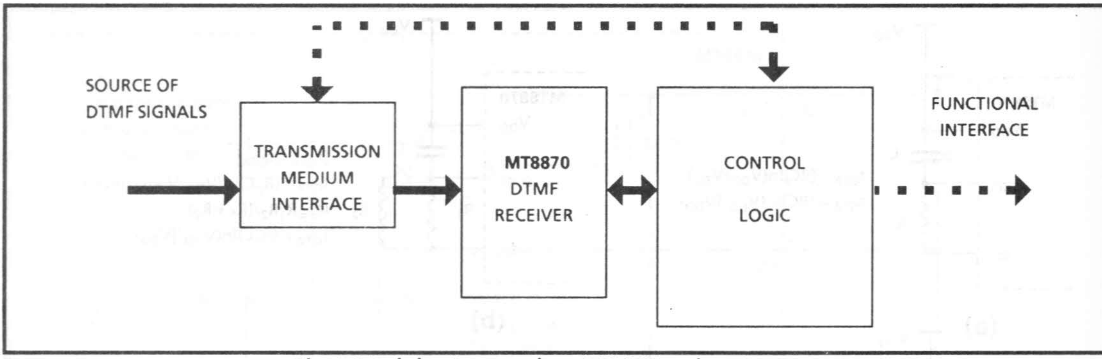


Fig. 7 Modular Approach to DTMF Receiver Systems

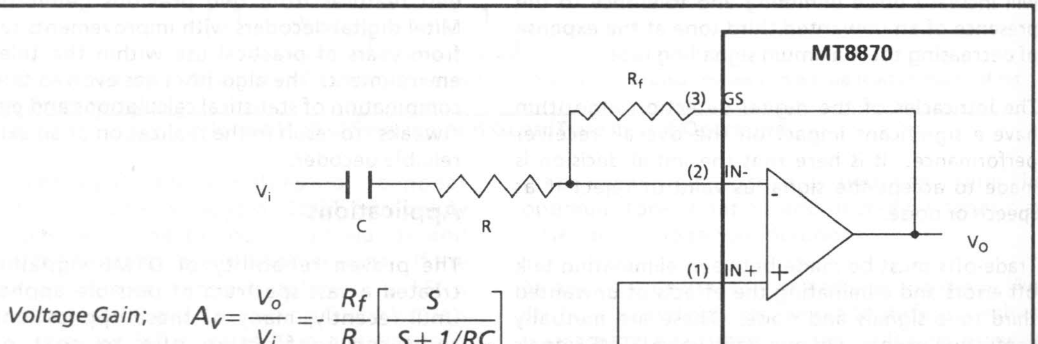
The design of a DTMF receiving system can generally be broken down into three functional blocks (Fig. 7). The first consideration is the interface to the transmission medium. This may be as simple as a few passive components to adequately configure the MT8870's input stage or as complex as some form of demodulation, multiplexing or analog switching system. The second functional block is the DTMF receiver itself. This is where the receiving system's parameters can be optimized for the specific signal conditions delivered from the "front end" interface. The third, and perhaps most widely varying function, is the output control logic. This may be as simple as a 4 to 16 line decoder, controlling a specific function for each DTMF code, or as complex as a full blown computer handling system protocols and adaptively varying the tone receiver's parameters to adjust for changing signal conditions. Several currently applied and conceptually designed applications are described subsequently but first let's consider the design of a typical input stage.

The input arrangement of the MT8870 provides a differential input op amp as well as a bias source (V_{REF}) which is used to bias the inputs at mid-rail. The output of this op amp is available to provide feedback for gain adjustment.

A typical single ended input configuration having unity gain is shown in Figure 8.

For balanced line applications good common mode rejection is offered by the differential configuration (Fig. 9). In both cases, the inputs are biased to 1/2 V_{DD} by V_{Ref}. Consider an input stage which will interface to a 600Ω balanced line. To reject common mode noise signals, a balanced differential amplifier input provides the solution.

With the input configured for unity gain the MT8870 will accept maximum signal levels of +1 dBm (into 600Ω). The lowest DTMF frequency that must be detected is approximately 685Hz. Allowing



Voltage Gain; $$A_V = \frac{V_o}{V_i} = -\frac{R_f}{R}\left[\frac{S}{S+1/RC}\right]$$

Input Impedance; $$\left|Z(\omega)\right| = R\left[1+(1/\omega RC)^2\right]^{\frac{1}{2}}$$

3dB Cutoff Frequency; $$f_c = \frac{1}{2\pi RC}$$

Fig. 8 Single Ended Input Configuration

0.1dB of attenuation at 685Hz, the required input time constant may be derived from;

$$M(\omega)_{dB} = 20log_{10}\frac{R_f}{R} + 20log_{10}\frac{\omega\tau}{\left[(\omega\tau)^2+1\right]^{\frac{1}{2}}}$$

where $M(\omega)_{dB}$ *is the amplifier gain in decibels*

ω *is the radian frequency*

τ *is the input time constant*

$$\textit{Therefore} \quad -0.1 = 20log_{10}\frac{(2\pi)685\tau}{\left[\left[(2\pi)685\tau\right]^2+1\right]^{\frac{1}{2}}}$$

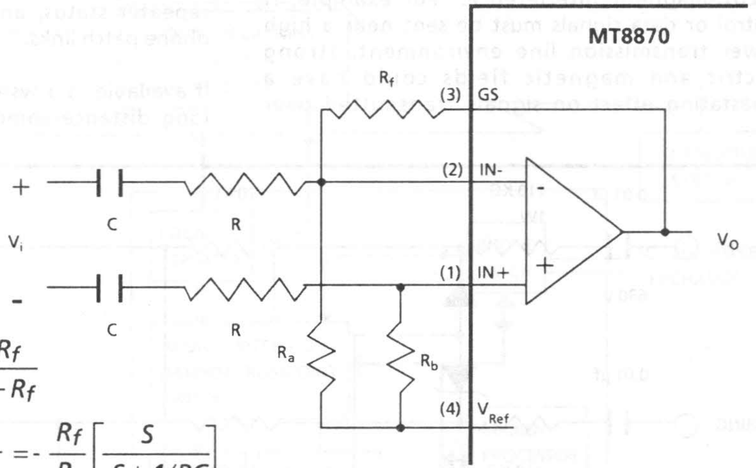
$$or\ \tau = 1.52mS$$

Now, choosing R=220K gives a high input impedance (440K in the passband) and C= τ/R=6.9nF (use a standard value of 10 nF). For unity gain in the passband we choose R_f=R. R_a and R_b are biasing resistors. The choice of R_a is not critical and could be set at, say... 68K. Bias resistor R_a adds a zero to the non-inverting path through the differential amplifier but has no affect on the inverting path. This zero can be exactly cancelled by the added pole due to R_b if R_b is chosen as;

$$R_b = \frac{R_aR_f}{R_a+R_f}.$$

With appropriate input transient protection, this circuit will provide an excellent bridging interface across a properly terminated telephone line for end-to-end or key system applications. Transient protection may be achieved by splitting the input resistors and inserting zener diodes to achieve voltage clamping (Fig. 10). This allows the transient energy to be dissipated in the resistors and diodes and limits the maximum voltage that may appear at the op-amp inputs.

It is important to consider the amount of shunt capacitance introduced by the protection devices. In this case the parasitic capacitances of the zener diodes are in series which reduces their effect. Relatively large shunt capacitances will attenuate the high group frequencies causing the input signal to "twist" which degrades receiver performance.



R_a can be chosen to be a convenient value greater than 50KΩ.

R_b selection; $R_b = \frac{R_aR_f}{R_a+R_f}$

Voltage Gain; $A_V = \frac{V_o}{V_i} = -\frac{R_f}{R}\left[\frac{S}{S+1/RC}\right]$

Input Impedance; $\left|Z(\omega)\right| = 2R\left[1+(1/\omega RC)^2\right]^{\frac{1}{2}}$

3dB Cutoff Frequency; $f_c = \frac{1}{2\pi RC}$

Fig. 9 Differential Input Configuration

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"Twist" is known as the difference in amplitude between the low and high group tones. It is specified in dB as:

$$TWIST = 20\log_{10}\frac{V_L}{V_H}$$

where V_L *is the amplitude of the low frequency tone*

and V_H *is the amplitude of the high frequency tone.*

Twist is usually caused by the frequency response characteristic of the communication channel. Along a telephone line higher frequencies tend to roll off faster than the lower ones so the line response is usually compensated for by applying pre-emphasis (negative twist) to the originating DTMF signal. In extreme cases the receiver may require compensation. This could be realized with a filter arrangement utilizing the input op amp.

Any communication path that can pass the human voice spectrum is eligible for DTMF signalling. Therefore a variety of "front-end" interfaces may be applicable in a given control system. More commonly used media are copper wire and RF channels. An optical fibre could carry a light beam modulated by DTMF. Although this would incur a large overhead in terms of bandwidth utilization, optical fibres do offer isolation from external electro-magnetic interference. For example, if control or data signals must be sent near a high power transmission line environment, strong electric and magnetic fields could have a devastating effect on signals transmitted over wires. DTMF over fibre-optics could easily be employed as a highly reliable communications method in a harsh interference infested environment.

In modern digital switching equipment the MT8870 can easily be interfaced to a digital PCM line by using a codec as an input interface (Fig. 11). Actually, all that is required for the interface is a PCM decoder. In fact, the output filter that normally is associated with PCM decoders is not required since the high group DTMF bandpass filter has an upper cutoff frequency low enough to meet the required roll-off of the PCM filter.

DTMF In Mobile Radio Applications

DTMF signalling plays an important role in distributed communications systems, such as multi-user mobile radio (Fig. 12). It is a "natural" in the two-way radio environment since it slips neatly into the center of the voice spectrum, has excellent noise immunity and highly integrated methods of implementation are currently available. It is also directly compatible with telephone signalling, simplifying automatic phone patch systems.

Several emergency medical service networks currently use DTMF signals to control radio repeaters. Functions are, typically, mobile identification, selection of appropriate repeater links, selection of repeater frequencies, reading of repeater status, and for completing automatic phone patch links.

If available in a system of this type, audio from a long distance communications link (microwave,

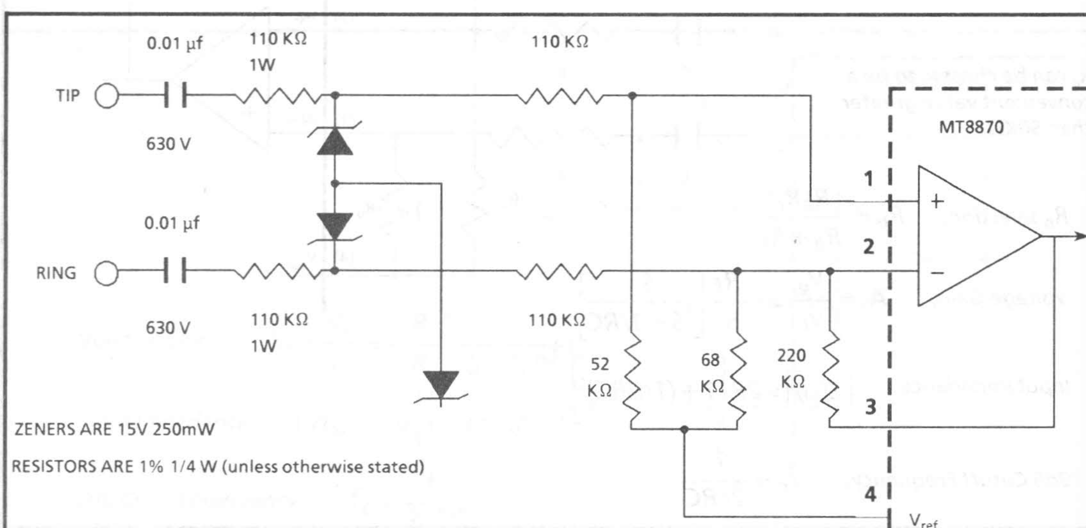


Fig. 10 MT8870 Front End Protection Circuit

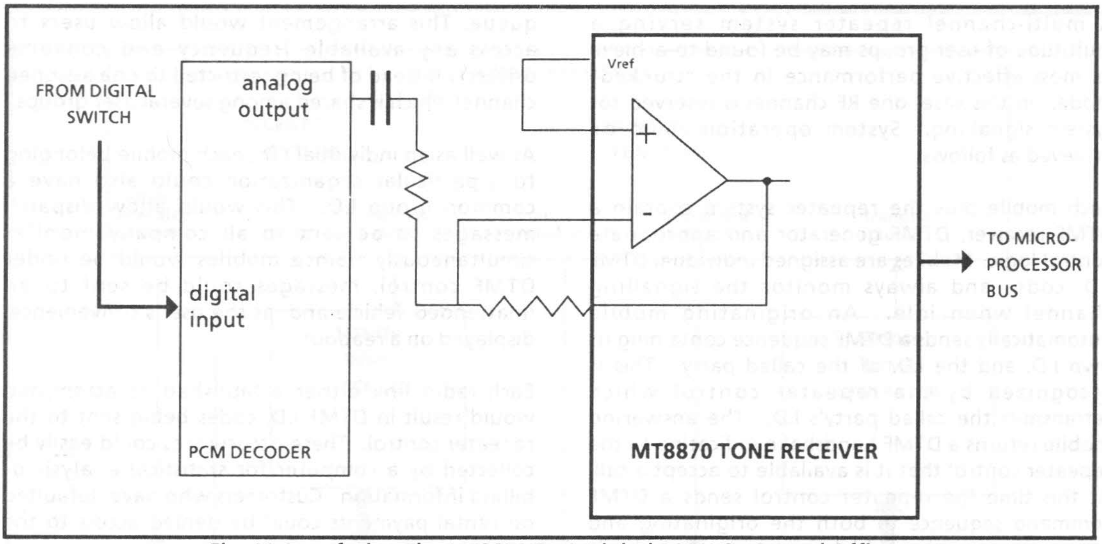
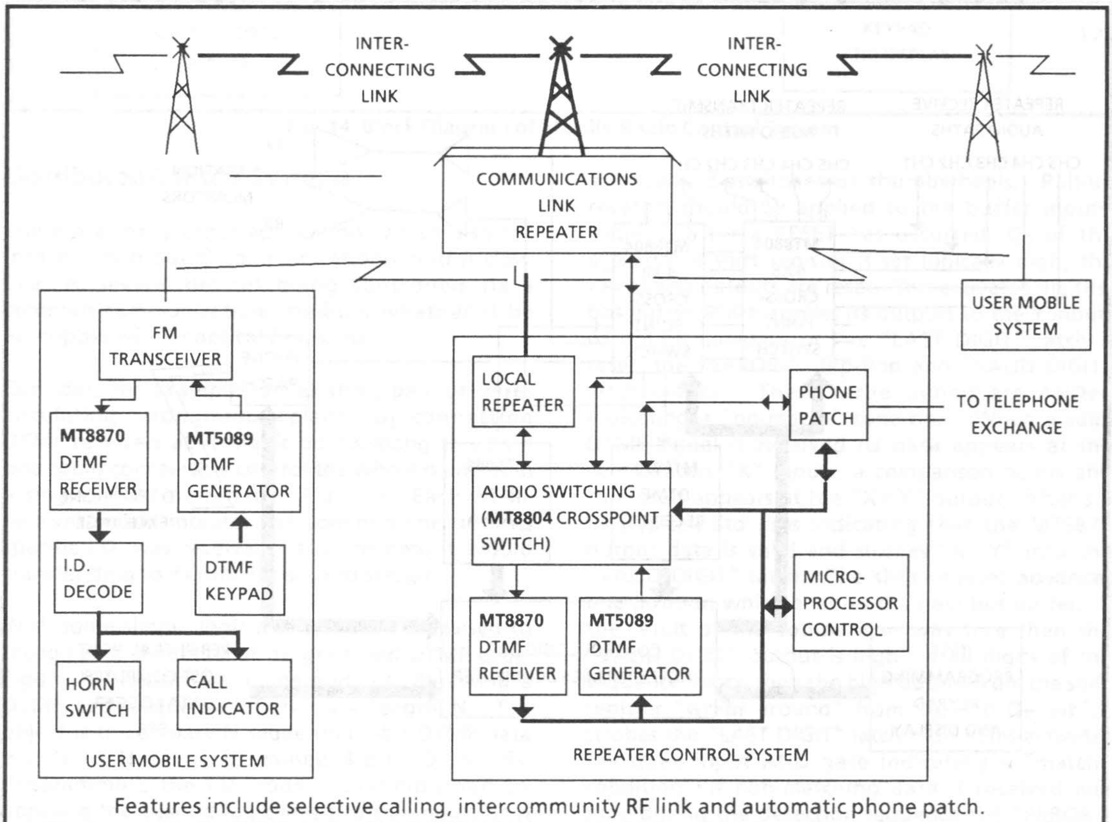


Fig. 11 Interfacing The MT8870 To A Digital PABX Or Central Office

satellite, etc.) could be switched, via commands from the user's DTMF keypad, into the local repeater. This would offer the mobile user a variety of paths for communication without the assistance of a human operator.



Features include selective calling, intercommunity RF link and automatic phone patch.

Fig. 12 DTMF Controlled Radio Repeater

A multi-channel repeater system serving a multitude of user groups may be found to achieve its most effective performance in the "trunked" mode. In this case, one RF channel is reserved for system signalling. System operation could be achieved as follows.

Each mobile plus the repeater system contain a DTMF receiver, DTMF generator and appropriate control logic. Mobiles are assigned individual DTMF I.D. codes and always monitor the signalling channel when idle. An originating mobile automatically sends a DTMF sequence containing its own I.D. and the I.D. of the called party. This is recognized by the repeater control which retransmits the called party's I.D. The answering mobile returns a DTMF handshake indicating to the repeater control that it is available to accept a call. At this time the repeater control sends a DTMF command sequence to both the originating and answering mobiles which instructs their logic circuits to switch to a specific, available channel. If all channels are busy the repeater control could send DTMF sequences to put both mobiles on "hold" and add their I.D.'s to a "channel-request" queue. This arrangement would allow users to access any available frequency and converse privately instead of being restricted to one assigned channel which is shared among several user groups.

As well as an individual I.D., each mobile belonging to a particular organization could also have a common group I.D. This would allow dispatch messages to be sent to all company mobiles simultaneously. Since mobiles would be under DTMF control, messages could be sent to an unattended vehicle and, at the user's convenience, displayed on a readout.

Each radio link either established or attempted would result in DTMF I.D. codes being sent to the repeater control. These occurrences could easily be collected by a computer for statistical analysis or billing information. Customers who have defaulted on rental payments could be denied access to the system.

Simplified block diagrams of the control systems for both the repeater and mobiles are shown in Figures 13 and 14 respectively.

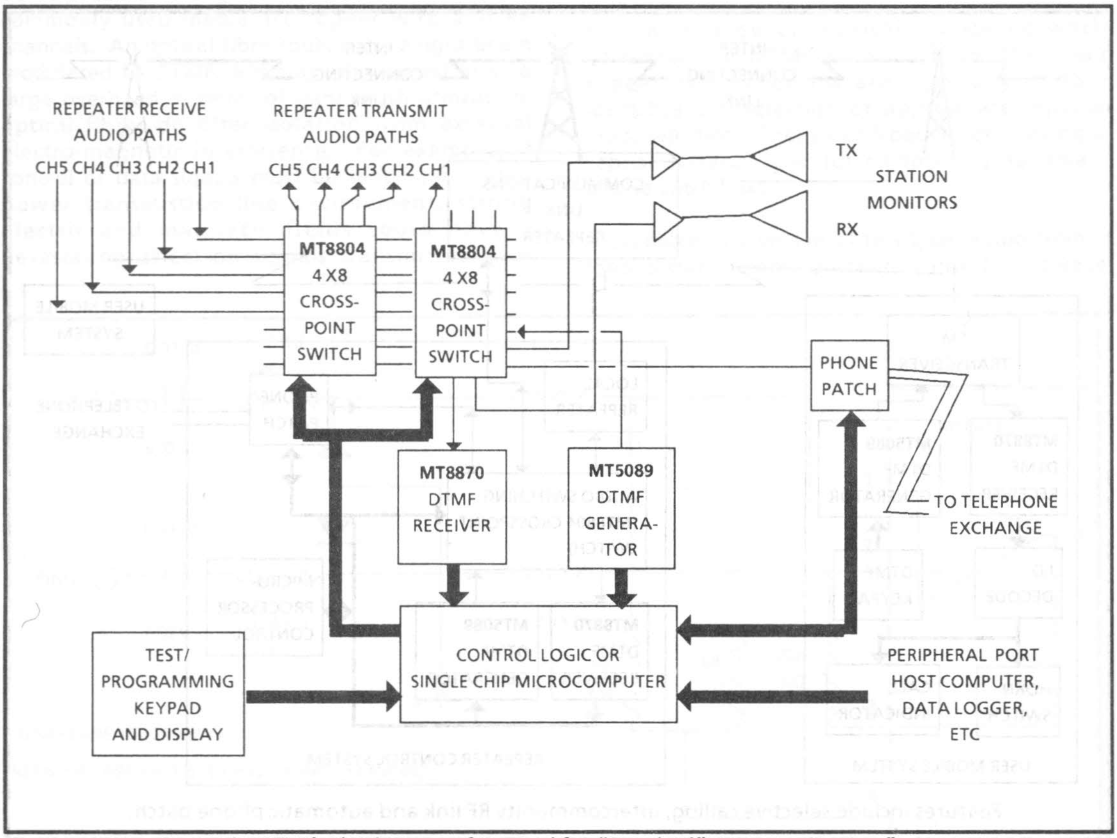


Fig. 13 Block Diagram of Control for "Trunked" Repeater System"

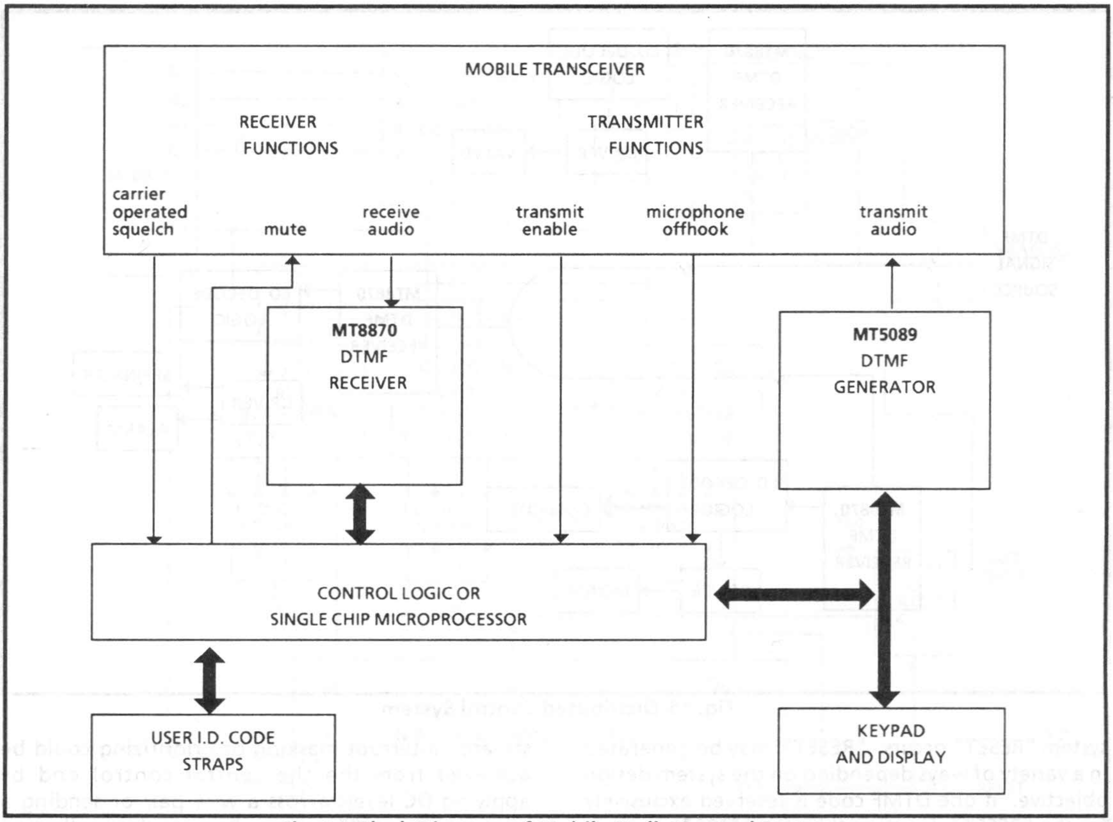


Fig. 14 Block Diagram of Mobile Radio Control System

Distributed Control Systems

There are many other applications which also fall into the distributed communications/control class. That is, several devices being controlled via a common communications medium whether it be RF, copper wire or optical fibres, etc.

Consider, for example, an existing pair of wires circulating throughout a plant. By connecting DTMF receivers at strategic points along this path one could conceivably control the whole plant from a single DTMF transmitter (Fig. 15). Each DTMF receiver would monitor the common line until its specific I.D. was received, at which time it would transfer data to its functional control logic.

With some simple logic a circuit can be devised to recognize a sequence of programmed DTMF code. Figure 16 illustrates a method of detecting a DTMF code sequence of arbitrary length, N. The object is to compare N sequential 4-bit DTMF data words to N preprogrammed 4-bit I.D. words. Programming the I.D. code is accomplished by applying the desired logic levels to the inputs of N 4-bit bus buffers. This may be achieved with straps as shown, dipswitches or thumbwheels. Pull-up resistors should be applied to the buffer inputs. Initially, after a RESET has occurred, Q_0 of the presettable shift register is set logically high, the remaining outputs are reset. This activates the first bus buffer which applies its outputs to the Y inputs of a 4-bit comparator.The "LAST DIGIT" latch is reset, the "ERROR-" flip-flop and "VALID DIGIT" latch are set. These three signals are ANDed indicating a "no-match" condition. When a valid DTMF signal is received its data appears at the comparators "X" inputs, a comparison occurs and the result appears at the "X=Y" output. After 3.4 µS (typical) Std rises indicating that the MT8870 output data is valid and strobes "X=Y" into the "VALID DIGIT" latch. The shift register advances one position which enables the next bus buffer. If the result of the comparison was true then the "VALID DIGIT" output is high. If all digits of the sequence match then the high output from the shift register "wraps around" from Q_{N-1} to Q_0, which strobes the "LAST DIGIT" latch high. This activates the three input AND gate indicating a "match" condition. If non-matching data is received any time during the detection sequence the "ERROR-" flip-flop is reset which disables the AND gate until a

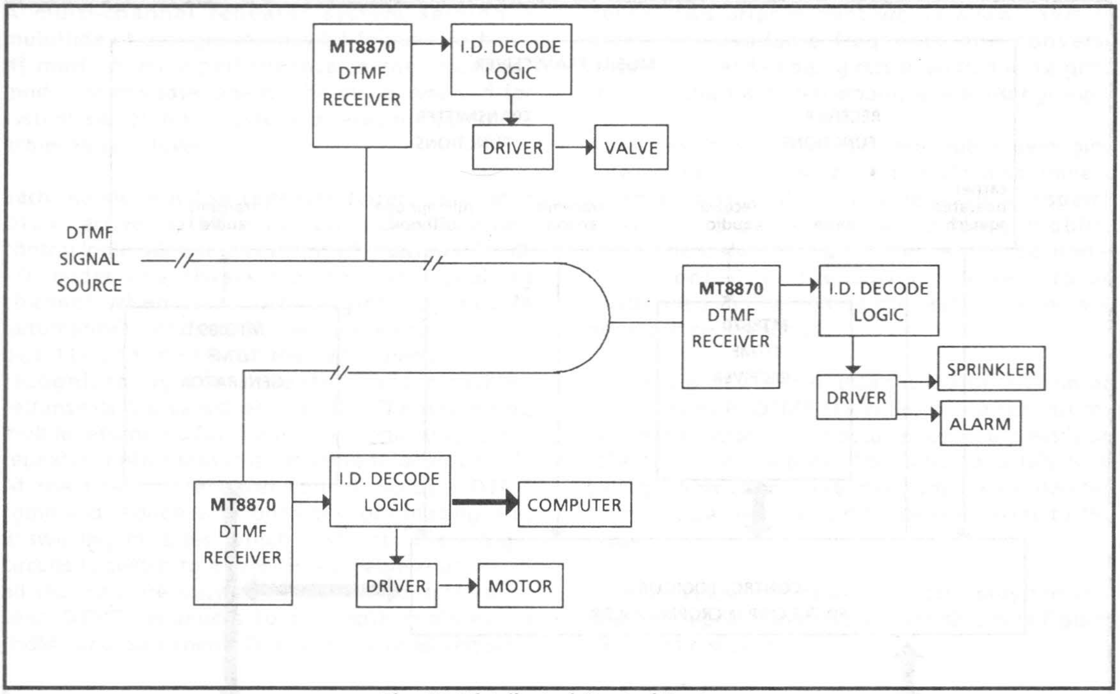


Fig. 15 Distributed Control System

system "RESET" occurs. "RESET" may be generated in a variety of ways depending on the system design objective. If one DTMF code is reserved exclusively for the "RESET" function then the MT8870 outputs can be decoded directly. This requires that the controller send a "RESET" command prior to sending an I.D. sequence. Alternatively a "time-out" timer, triggered by StD, could serve to generate a system reset if a certain time lapse occurs between received signals. This method places time constraints on the system but eliminates the need to consume a DTMF command for the "RESET" function.

The concept of using a common transmission medium for control signalling applies to several possible situations. Plant process control, remote measurement control, selective intercom call systems, institutional intercom systems, two way radio control, pocket pagers and model car or boat remote control, just to mention a few.

Conversely, data could be collected from distributed sources. Implemented on a circulating wire or an RF channel, as illustrated in Figure 17, information could be collected by a central unit which individually polls each monitor to ask for data. Alternatively, the system could be interrupt driven (Fig.18). In this case each monitor, when ready to send data, generates an interrupt request by sending a DTMF I.D. sequence followed by a data stream. Interrupt masking or prioritizing could be achieved from the the central control end by applying DC levels across a wire pair or sending a pilot tone in an RF system. Remote data collection units would monitor this signal to detect when a higher priority interupt is being handled or the communications channel is busy.

Data Communication Using DTMF

There is a vast array of potential applications for DTMF signalling using the existing telephone network. Considering that there are millions of ready-made data sets installed in convenient locations (i.e. the Touch Tone™ telephone) remote control and data entry may be performed by users without requiring them to carry around bulky data modems.

Potential applications include:

- home remote control
- remote data entry from any Touch-Tone keypad
- credit card verification and inquiry
- salesman order entry
- catalogue store (stock/price returned via voice synthesis)
- stock broker buy/sell/inquire -using stock exchange listing mnemonics
- answering machine message retrieval
- automatic switchboard extension forwarding

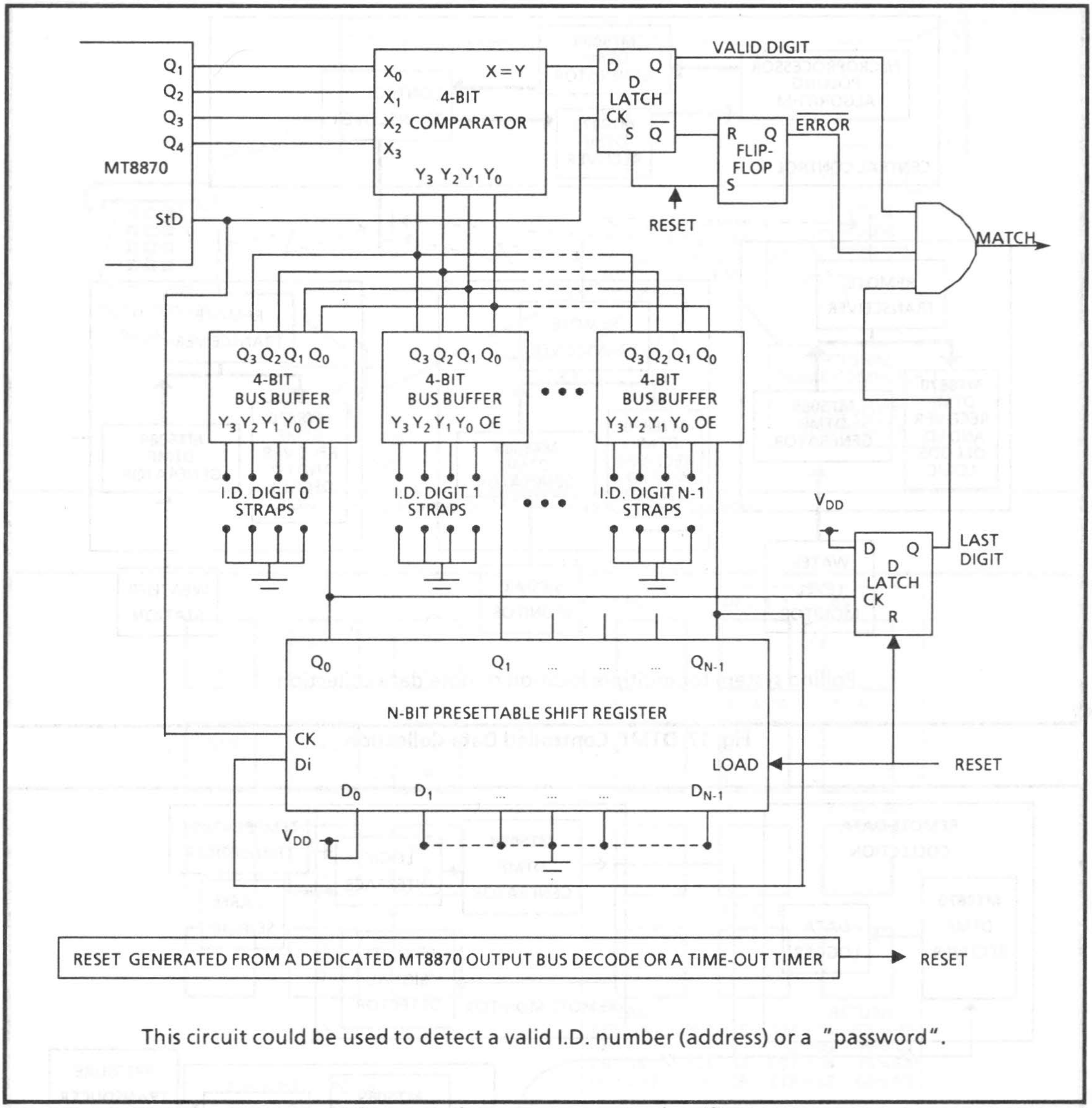
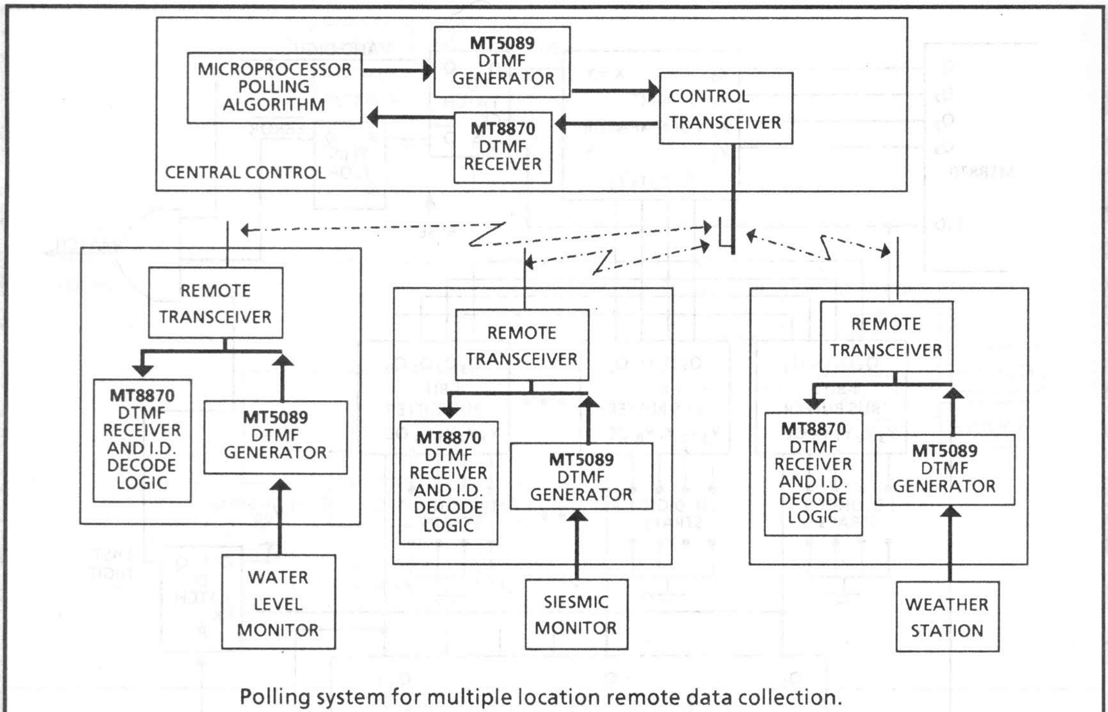


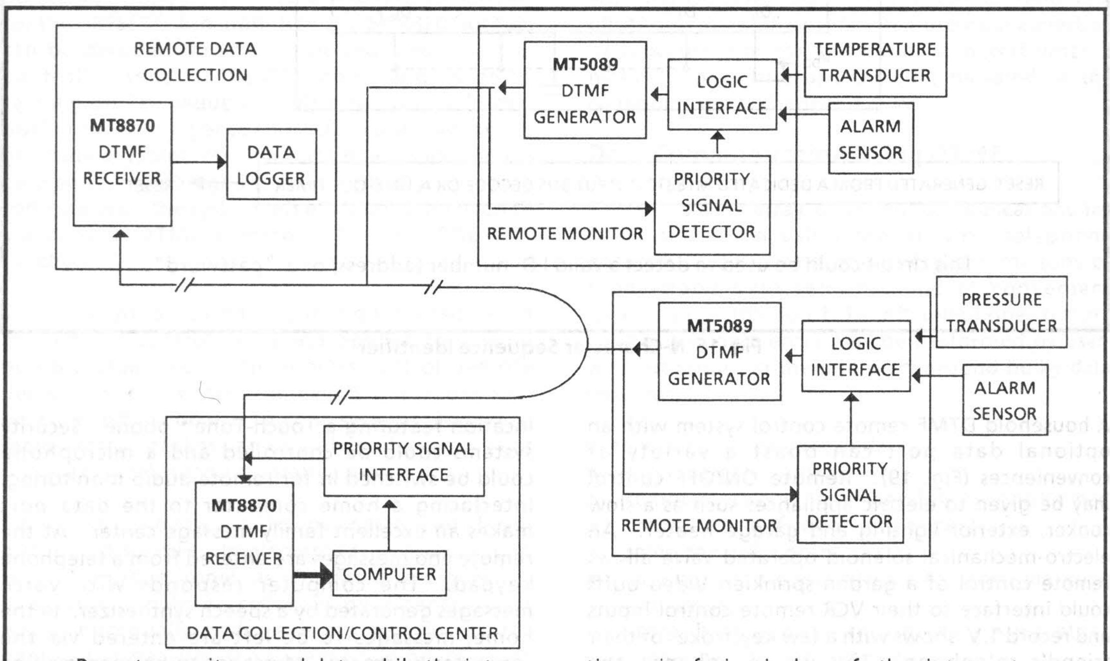
Fig. 16 N-Character Sequence Identifier

A household DTMF remote control system with an optional data port can boast a variety of conveniences (Fig. 19). Remote ON/OFF control may be given to electric appliances such as a slow cooker, exterior lighting and garage heater. An electro-mechanical solenoid operated valve allows remote control of a garden sprinkler. Video buffs could interface to their VCR remote control inputs and record T.V. shows with a few keystrokes of their friend's telephone. This would enhance the function of timers which are currently available on most VCR's. Schedule changes or unexpected broadcasts could be captured from any remote location featuring a Touch-Tone™ phone. Security systems could be controlled and a microphone could be switched in for remote audio monitoring. Interfacing a home computer to the data port makes an excellent family message center. At the remote end messages are entered from a telephone keypad. The computer responds with voice messages generated by a speech synthesizer. In the home, messages to be left are entered via the computer keyboard. Messages to be read may be displayed on the computer monitor or "played back" through the speech synthesizer.



Polling system for multiple location remote data collection.

Fig. 17 DTMF Controlled Data Collection



Remote monitors send data while the interconnecting pair of wires is clear of other interrupts.

Fig. 18 Interupt Driven Data Collection System

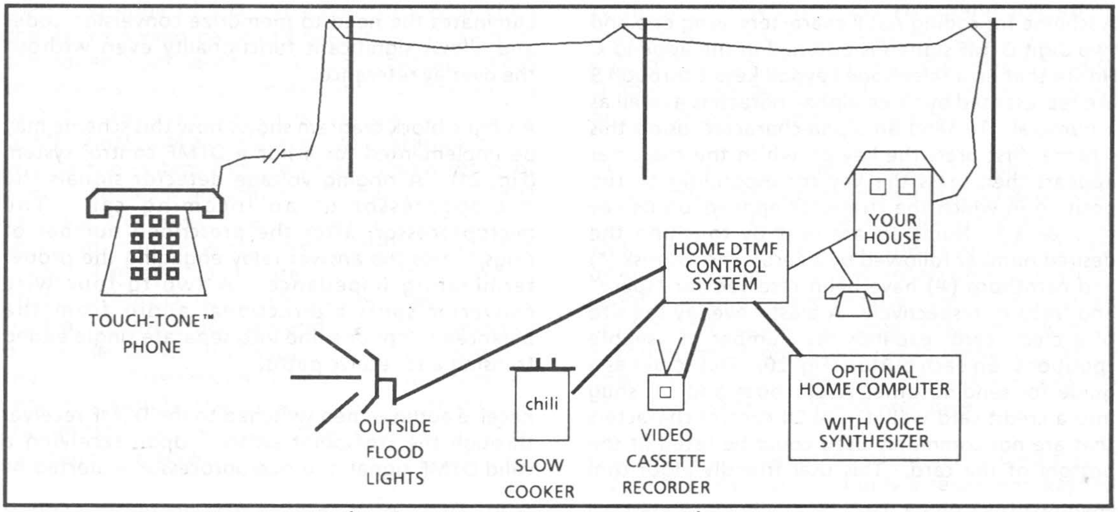
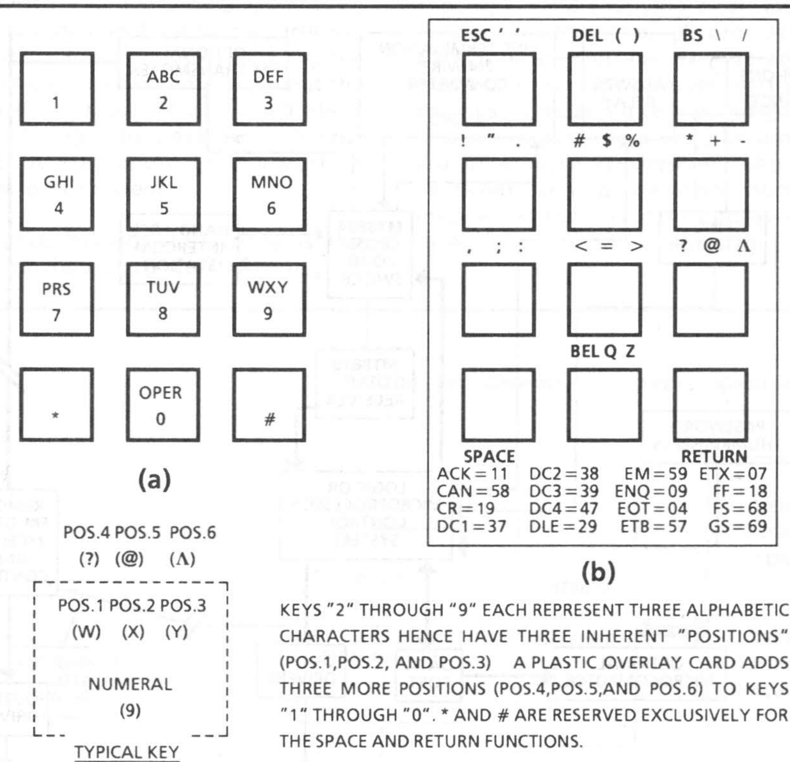


Fig. 19 Home DTMF Remote Control System



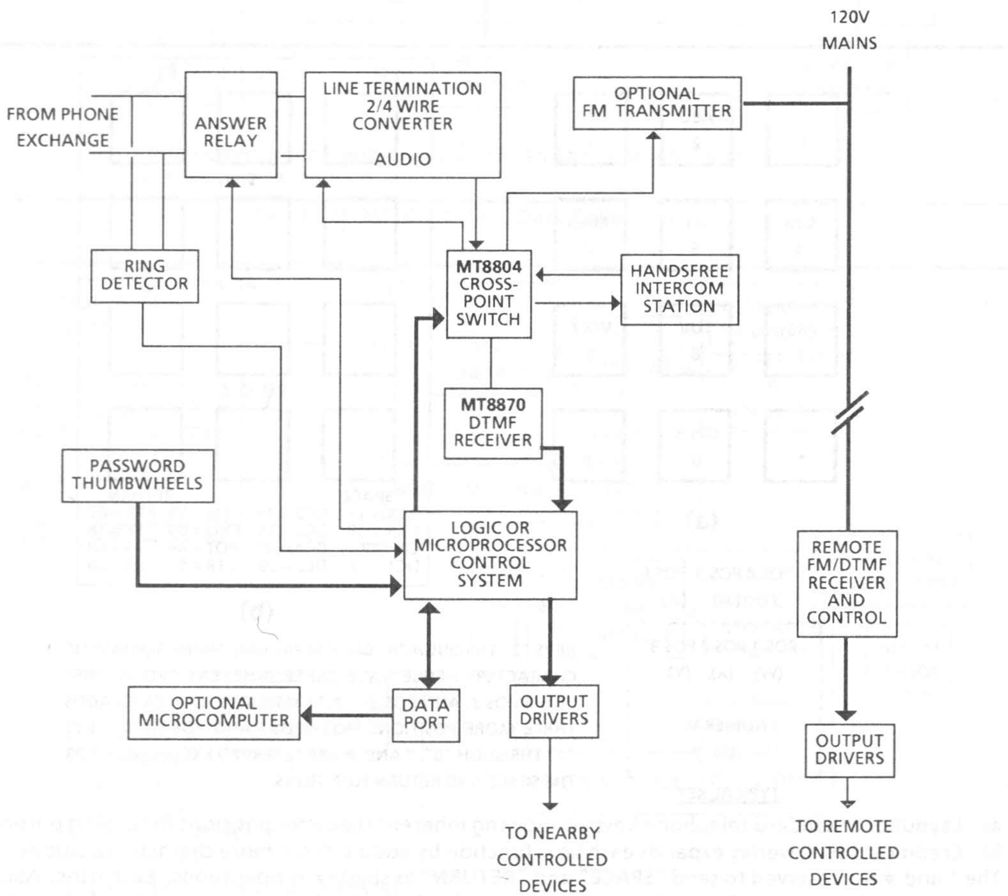
a) Layout of a standard telephone keypad showing inherent character positions for coding purposes.
b) Credit card size overlay expands each keys function by adding three more character positions.
The * and # are reserved to send "SPACE" and "RETURN" as single key operations. Each other ASCII code requires two keystrokes. To send a character simply push the button on or over which it appears, then push the numeral corresponding to its position . For example, to send a "T" push '8' followed by '1', to send "%" push '5' followed by '6'.

Fig. 20 Using A Pushbutton Phone As A Data Terminal

A scheme for coding ASCII characters using one and two digit DTMF signals is outlined in the appendix. Notice that on a telephone keypad keys 2 through 9 are represented by three alpha-characters as well as a numeral. To send an alpha-character, using this scheme, first press the key on which the character appears then press the key corresponding to the position in which the character appears on its key (1, 2 or 3). Numerals are sent by touching the desired number followed by a zero. The asterisk (*) and octothorp (#) have been reserved for "space" and "return" respectively. A plastic overlay the size of a credit card expands the number of useable "positions" on each button (Fig. 20). This serves as a guide for sending other ASCII codes and fits snug into a credit card wallet. ASCII control characters that are not commonly used could be listed at the bottom of the card. This user-friendly algorithm eliminates the need to memorize conversion codes and allows significant functionality even without the overlay reference.

A simple block diagram shows how this scheme may be implemented for a home DTMF control system (Fig. 21). A ringing voltage detector signals the microprocessor of an incoming call. The microprocessor, after the prescribed number of rings, closes the answer relay engaging the proper terminating impedance. A two-to-four wire converter splits bidirectional audio from the balanced telephone line into separate single ended transmit and receive paths.

Receive audio is then switched to the DTMF receiver through the crosspoint switch. Upon receiving a valid DTMF signal, the microprocessor is alerted by



An FM transmitter could be used to couple control signals for distribution over existing power lines. This would eliminate the need for installing wires between the DTMF control unit and remote controlled devices.

Fig. 21 Block Diagram Of Home DTMF Remote Control System

the rising edge of StD. The microprocessor then checks for a valid password sequence and decodes subsequent commands. A command can be entered to put the system into remote-control mode. In this case the crosspoint switch is configured to route DTMF signals into the FM-over-mains transmitter as well as the system tone receiver. Forwarding of control signals is accomplished by applying an FM carrier to the power line. This eliminates the need to string control wires haphazardly about the house. The appropriate device is selected by its unique DTMF I.D. code. The microcomputer keeps track of all device locations and their I.D. codes since it must decide when to supply function outputs to the "nearby" devices and when to let the "remote" receivers handle the data. Subsequent data is transmitted to a selected device until a 'reset' command is entered.

Upon receiving any DTMF signal, answer back tones are returned by the microprocessor to acknowledge valid or invalid operations and to indicate the state of an interrogated device. For example, a low to high tone transition could indicate that a particular device is on, a high to low transition indicating the off state. A command could be entered to put the system in an 'external' mode which would allow communications through the data port. A host computer could be connected to this port to broaden the scope of the system.

The resident microprocessor unit contains the software and hardware to control ringing verification, password and command decoding, answer back tone generation, audio routing, output function latches and an optional data port. Output drivers buffer the latches and switch relays or SCRs to control peripheral devices.

An infinite variety of devices could be controlled by such a system, the spectrum of which is limited only by the ability to provide appropriate interfacing. This system could also be the heart of a DTMF intercom system allowing intercommunication, "phone-patching", and remote control from varied household locations. This type of system concept is, of course, anything but limited to home use. Many applications can provide conveniences to consumers, salespeople and executives.

For example, a merchant could verify credit card accounts quickly utilizing only a telephone keypad for data entry (Fig. 22). Each credit card company could reserve one or more telephone lines to provide this function, reducing the human effort required. The receiving end system would be required to answer the call, provide a short answer back tone or message, receive and decode the credit card account number, verify it, verify the owner's name and give a go/no-go authorization. This return data could easily be provided with the aid of a voice synthesizer. An auto-dialler containing appropriate phone numbers could be installed at the merchant end as an added time saver.

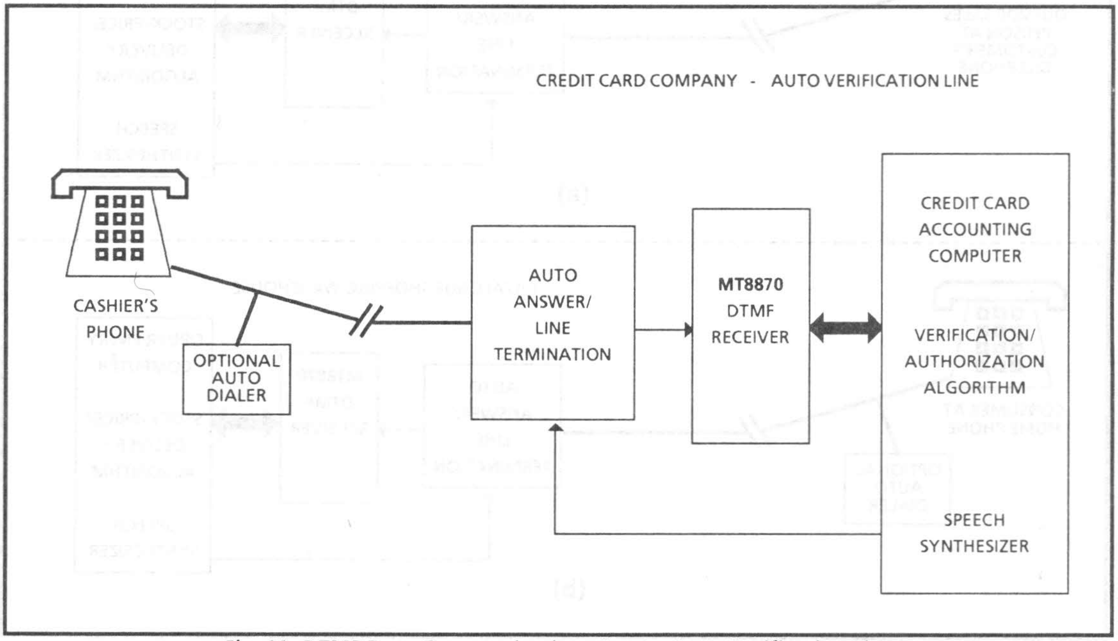


Fig. 22 DTMF Data Communications For An Auto Verification Line

With a similar arrangement, a travelling salesman could access price, delivery and customer status, enter or delete merchandise orders and retrieve messages all from the comfort of the customer's office (Fig. 23a). A department store could provide shop-by-phone service to its customers using telephone keypad data entry (Fig. 23b). Brokerage firms, utilizing the stock exchange mnemonic listings could provide trading price information and buy/sell service via telephone keypad entry. A voice synthesizer could provide opening and current trading price, volume of transactions and other pertinent data. A telephone answering system manufacturer could apply this technique, allowing users to access and change outgoing and incoming messages from a Touch-Tone™ phone.

A PBX manufacturer could offer a feature that relieves the switchboard attendant from unneccesary interaction. A call could be answered automatically and a recording may reply "Thank you for calling XYZ. Please dial the extension you wish to contact or zero for the switchboard". If the caller knows the called party's extension in advance it is not neccesary to wait for the switchboard attendant to forward the call. The attendant could be notified to intervene if there is no action by the caller say, ten seconds after the recording ends. This provides a similar function to a "Direct Inward Dialling" (DID) trunk but without the additional overhead incurred with renting a block of phone numbers as in the DID case.

Now that a DTMF receiver is so easy and inexpensive to implement there are many simple dedicated uses that become attractive. A useful home and office application for DTMF receivers is in a self-contained telephone-line-powered toll call restrictor similar to the block diagram in Fig. 2a. This could be installed in an individual telephone or at the incoming main termination depending on which phone or phones are to be restricted. While disallowing visitors from making unauthorized long distance calls, the owner may still desire access to toll dialling. This could be provided by adding a logic circuit that disables the toll restrictor upon receiving a predetermined sequence of DTMF characters (Fig. 16). In this case, the user must enter his password before dialling a long distance number.

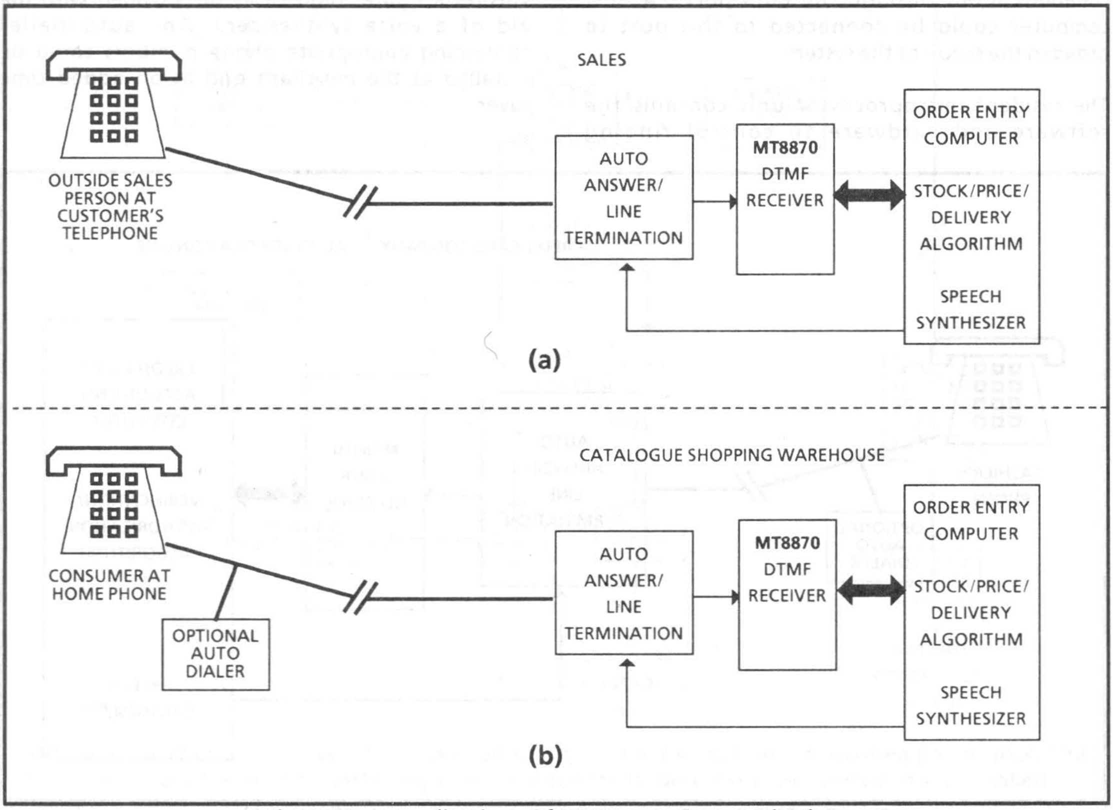


Fig. 23 Two Applications Of DTMF Data Communications

Conclusion

The applications for DTMF signalling are tremendous and due to innovative technological advances its use is increasingly widespread. DTMF offers highly reliable, cost effective signalling solutions which require no development effort on the user's part. The advent of single chip receivers has allowed many products that were previously not cost-effective to be manufactured in production quantities.

DTMF signalling was originally designed for telephony signalling over voice quality telephone lines. This signalling technique has been applied to a multitude of control and data communications systems. All that is required is a voice quality communication channel with appropriate interfacing. The applications are limited only by one's imagination.

Appendix

ASCII TO DTMF CONVERSION

Partial ASCII coding and conversion to 2 sequential DTMF signals

ASCII	HEX	DTMF	ASCII	HEX	DTMF	ASCII	HEX	DTMF
ACK	06	1 1	!	21	4 4	A	41	2 1
BEL	07	0 1	"	22	4 5	B	42	2 2
BS	08	3 4	#	23	5 4	C	43	2 3
CAN	18	5 8	$	24	5 5	D	44	3 1
CR	0D	1 9	%	25	5 6	E	45	3 2
DC1	11	3 7	&	26	7 9	F	46	3 3
DC2	12	3 8	'	27	1 6	G	47	4 1
DC3	13	3 9	(	28	2 5	H	48	4 2
DC4	14	4 7	)	29	2 6	I	49	4 3
DEL	7F	2 4	*	2A	6 4	J	4A	5 1
DLE	10	2 9	+	2B	6 5	K	4B	5 2
EM	19	5 9	,	2C	7 4	L	4C	5 3
ENQ	05	0 9	-	2D	6 6	M	4D	6 1
EOT	04	0 8	.	2E	4 6	N	4E	6 2
ESC	1B	1 4	/	2F	3 6	O	4F	6 3
ETB	17	5 7	0	30	0 0	P	50	7 1
ETX	03	0 7	1	31	1 0	Q	51	0 2
FF	0C	1 8	2	32	2 0	R	52	7 2
FS	1C	6 8	3	33	3 0	S	53	7 3
GS	1D	6 9	4	34	4 0	T	54	8 1
HT	09	1 2	5	35	5 0	U	55	8 2
LF	0A	1 3	6	36	6 0	V	56	8 3
NAK	15	4 8	7	37	7 0	W	57	9 1
NUL	00	0 4	8	38	8 0	X	58	9 2
RS	1E	7 7	9	39	9 0	Y	59	9 3
SO	0E	2 7	:	3A	7 6	Z	5A	0 3
S1	0F	2 8	;	3B	7 5	[	5B	8 7
SOH	01	0 5	<	3C	8 4	\	5C	3 5
SP	20	*	=	3D	8 5	]	5D	8 8
STX	02	0 6	>	3E	8 6	∧	5E	9 6
SUB	1A	6 7	?	3F	9 4	_	5F	8 9
SYN	16	4 9	@	40	9 5	`	60	1 5
US	1F	7 8				DEL	7F	2 4
VT	0B	1 7						

Application Note **MSAN-117**

Applications of the MT3530 300 BPS Single Chip Modem

9161-001-034-NA ISSUE 1 June 1986

Contents

1.0 Introduction

Modems are used for exchanging information between home computers, personal computers, banks, offices and mainframes to name just a few possible applications. Computers and other data processing machines work with data in the form of binary pulses whereas the long distance communication medium, used by the telephone system, requires bandlimited analog signalling. The modem converts digital baseband data to an analog carrier and vice versa so that two devices such as a computer and a data terminal may communicate over a telephone system.

300 baud modems are among the most common data communications devices in use today. Modem system, based on the MT3530, has the advantages of full duplex communication using either Bell 103 or CCITT V.21 Recommendation Standard, a built-in interface to the industry standard RS-232C serial data port, very low system part count, and low power ISO^2-CMOS single chip modem I.C.

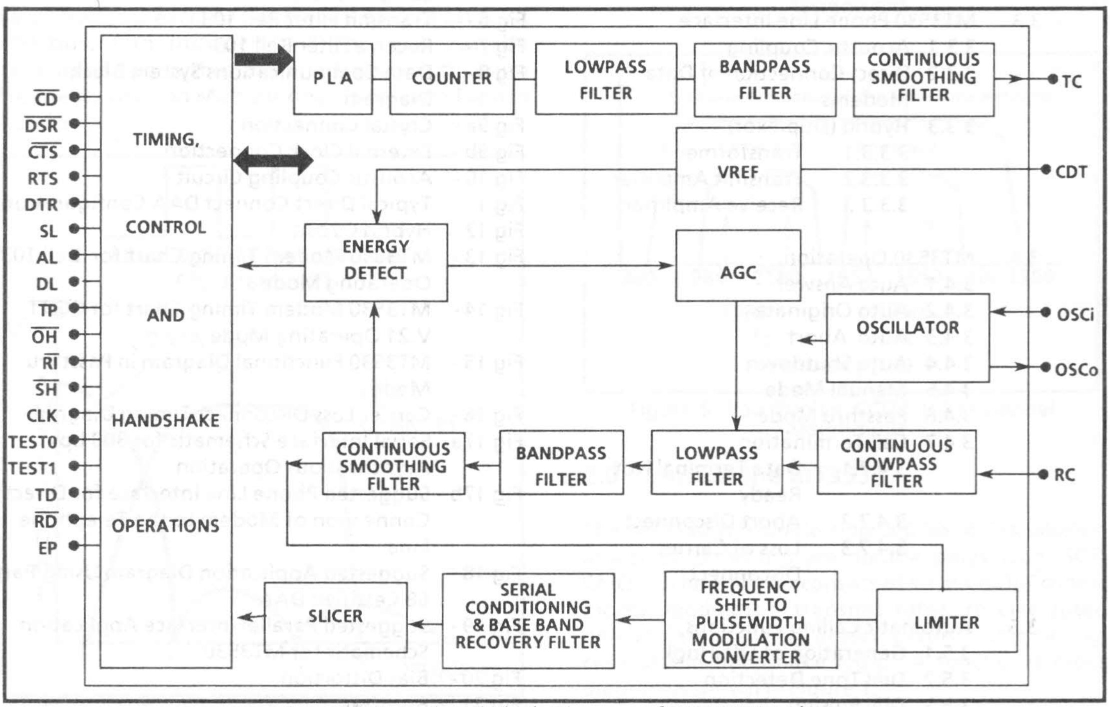


Figure 1 - Functional Block Diagram of MT3530 Modem

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1.1 Why are Modems Used?

The digital data signal is, typically, a random sequence of pulses which has a continuous power spectrum. This spectrum extends to zero frequency, hence, transmission via a telephone line is not possible because a phone line is bandlimited. See Figure 2.

The purpose of a modem is to translate digital signals into analog signals compatible with the existing telephone network bandwidth of 300 Hz to 3400 Hz. In transmit mode the modem converts binary data into analog signals that the phone line can carry. In the receive mode the modem demodulates the analog signals from the phone line, converting them back to the binary form.

1.2 What is a 300 Baud FSK Modem?

Bell 103 and CCITT V.21 are both 300 baud modem specifications. They use Frequency Shift Keying (FSK) modulation for data transmission over standard phone lines. FSK encodes binary data into two discrete frequencies within the bandwidth of the media used. A logic "1" in the bit stream places a Mark frequency (Fm) on the phone line. A logic "0" places a Space frequency (Fs) on the line. See Figure 3. Full duplex operation occurs when two-way transmission happens simultaneously between two modems. Since FSK modulation encodes only one bit per baud, it uses approximately 1 Hz of bandwidth for each bit per second of data rate. At 300 bps, two independent channels can be accommodated within the line's bandwidth using Frequency Division Multiplexing (FDM). See Figures 4 and 5.

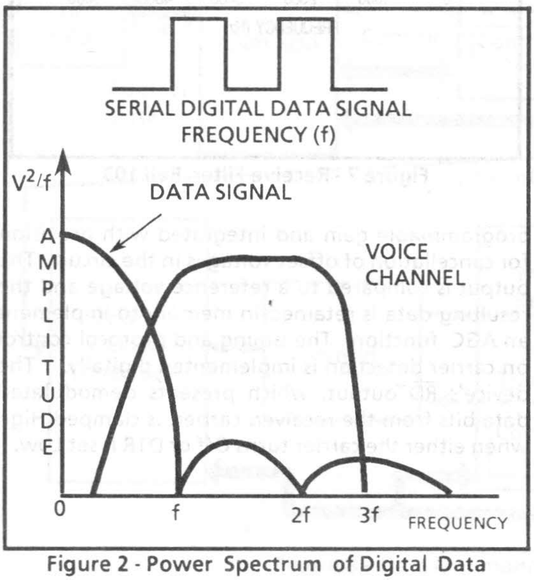

Figure 2 - Power Spectrum of Digital Data

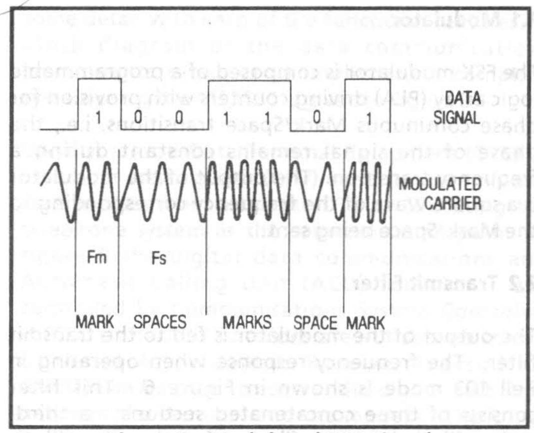

Figure 3 - Modulated FSK Signal

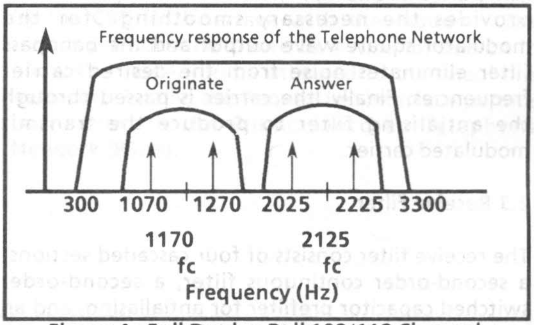

Figure 4 - Full Duplex Bell 103/113 Channel Assignment

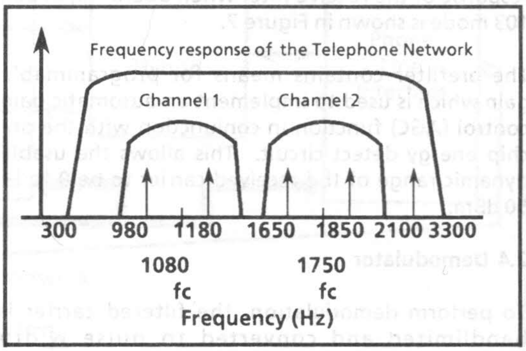

Figure 5 - Full Duplex, CCITT V.21 Channel Assignment

2.0 Inside the MT3530

The MT3530 is a single-chip 300 baud FSK Modem implemented in a 5 μm double polysilicon ISO²-CMOS technology. It consists of six major functional blocks; modulator, transmit filter, receive filter, demodulator, energy detect circuit, and timing, control and handshake logic. A functional block diagram is shown in Figure 1.

2.1 Modulator

The FSK modulator is composed of a programmable logic array (PLA) driving counters with provision for phase continuous Mark/Space transitions, i.e., the phase of the signal remains constant during a frequency transition. The output of the modulator is a square wave of the frequency corresponding to the Mark/Space being sent.

2.2 Transmit Filter

The output of the modulator is fed to the transmit filter. The frequency response when operating in Bell 103 mode is shown in Figure 6. This filter consists of three concatenated sections: a third-order elliptic low pass filter, a fourth-order elliptic bandpass filter, and a second order Sallen and Key low pass smoothing filter. The low pass filter provides the necessary smoothing for the modulator square wave output and the bandpass filter eliminates noise from the desired carrier frequencies. Finally, the carrier is passed through the antialising filter to produce the transmit modulated carrier.

2.3 Receive Filter

The receive filter consists of four cascaded sections; a second-order continuous filter, a second-order switched capacitor prefilter for antialiasing, and an eighth-order bandpass filter, followed by a second-order continuous smoothing filter. The frequency response of the receive filter when operating in Bell 103 mode is shown in Figure 7.

The prefilter contains means for programmable gain which is used to implement an automatic gain control (AGC) function in conjunction with the on-chip energy detect circuit. This allows the usable dynamic range of the received carrier to be 0 to −50 dBm.

2.4 Demodulator

To perform demodulation, the filtered carrier is bandlimited and converted to pulse width modulation format. This is, then, introduced to a baseband recovery filter which includes a third-order Bessel low pass filter.

2.5 Carrier Detection

The carrier detect circuit causes $\overline{CD}$ pin output to turn On and Off at receive carrier levels of −41 and −50 dBm, respectively, with appropriate timing. These levels can be modified by applying an external voltage to the device's CDT pin. The filtered receive carrier is rectified with programmable gain and integrated with provision for cancellation of offset voltages in the circuit. The output is compared to a reference voltage and the resulting data is retained in memory to implement an AGC function. The timing and protocol control on carrier detection is implemented digitally. The device's $\overline{RD}$ output, which presents demodulated data bits from the received carrier, is clamped High when either the carrier turns Off or DTR is set Low.

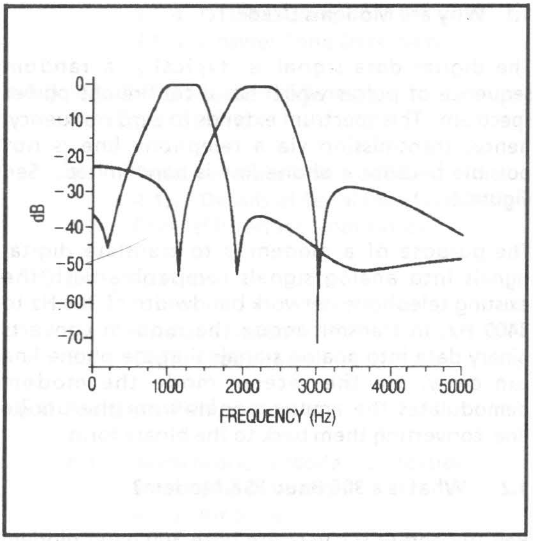

Figure 6 - Transmit Filter Bell 103

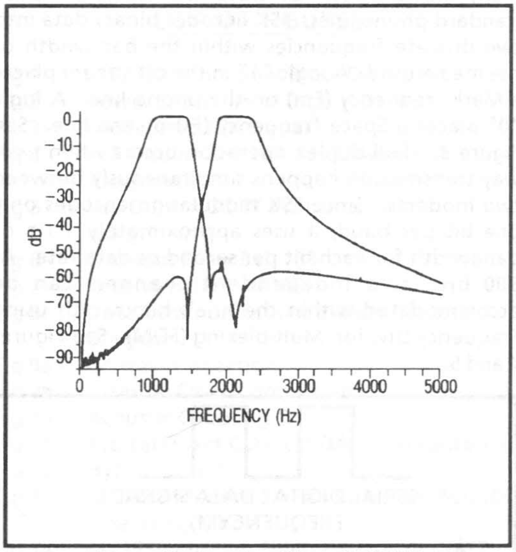

Figure 7 - Receive Filter Bell 103

2.6 Timing, Control and Handshaking

This block, besides providing necessary timing signals to various parts of the device, also implements the RS-232C interface. Further, the control section provides the capability for automatic answering/origination/dialing. It supports Phone Line Interface and Diagnostic control. Timing for the internal operation is governed by the 3.579545 MHz clock.

2.7 Other Functions

The transmit and receive sections are programmable and can be made to work in the same frequency band to allow for true analog loopback capabilities to facilitate local testing. Remote testing is made possible by inclusion of digital loopback capabilities.

3.0 Data Communications System using the MT3530

3.1 Data Communications System Configuration

The MT3530 can be configured to operate with very few external components. However, a sophisticated application will want to incorporate the MT3530 into a data communications system consisting of many functional features. This section deals in some detail with each of the functional features. A block diagram of the data communications components required to implement a complete system using the MT3530 is given in Figure 8.

Usually, a local Data Terminal Equipment (DTE) or central processing unit (CPU) needs to transmit and receive data from a remote DTE or CPU using the telephone system as the communication path. In figure 8 the digital data communications and Automatic Calling Unit (ACU) functions are controlled by Communications System Controller (CSC). If the ACU functions are not desired then a Universal Asynchronous Receiver/Transmitter (UART) can be used to control the digital data flow between the terminal and the modem. The UART type of control function is described more thoroughly in Section 4.2. The control/data information received from the CPU is conditioned by the CSC for interface with the modem. The Hybrid provides the 2-wire to 4-wire conversion to allow the modem to be attached to the telephone network. Finally, the Phone Line Interface permits connection to the Public Switched Telephone Network (PSTN).

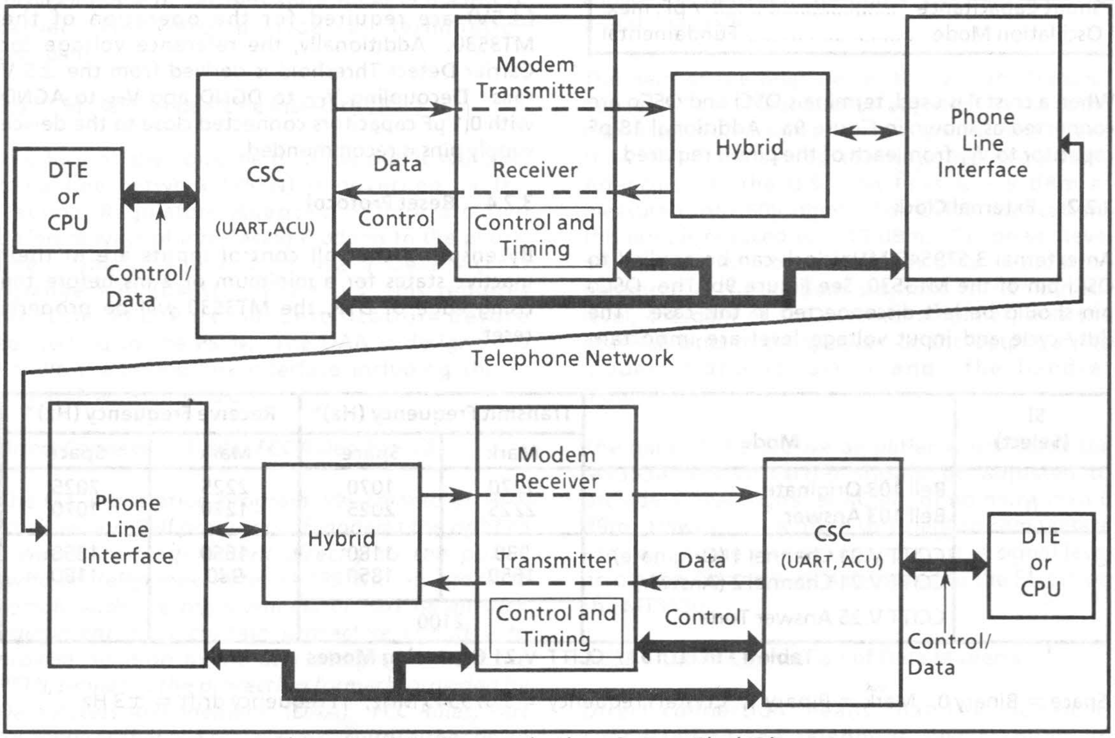

Figure 8 - Data Communications System Block Diagram

3.2 MT3530 Design-In Considerations

In this section, external connections to the MT3530 are defined. Also, special circuit and component considerations for designing the MT3530 based data communications system are explained in detail.

3.2.1 Clock Crystal

The MT3530 has an internal oscillator and clock generator that can be controlled either by an external crystal or external clock. It uses a low-cost 3.579545 MHz crystal as the master clock generator. This crystal is very popular because it is used in all NTSC colour TV's and in many low cost personal computers for interface with TV monitors. The MT3530 can, therefore, use the same system clock as the display interface. The characteristic of a crystal which is acceptable for use with the MT3530 is given below:

Quartz Crystal Specification (25 °C ± 2 °C)	
Operating Temperature Range	0 °C to +70 °C
Frequency	3.579545 MHz
Frequency Calibration Tolerance	± 0.02 %
Load Capacitance	18 pF
Effective Series Resistance	180 ohms, max.
Drive Level-Correlation/Operating	2 mW
Shunt Capacitance	7 pF, max.
Oscillation Mode	Fundamental

When a crystal is used, terminals OSCi and OSCo are connected as shown in Figure 9a. Additional 18 pF capacitor to V_{EE} from each of the pins is required.

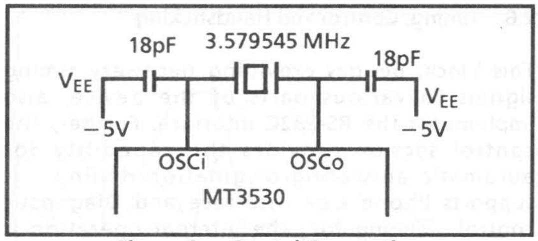

Figure 9a - Crystal Connection

3.2.2 External Clock

An external 3.579545 MHz clock can be applied to OSCi pin of the MT3530. See Figure 9b. The OSCo pin should be left disconnected in this case. The duty cycle and input voltage level are important parameters when an external clock is chosen over a crystal. A TTL level, 50% duty cycle, squarewave can be applied to OSCi pin through a 0.1 µF decoupling capacitor.

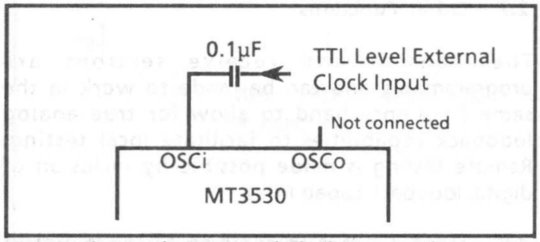

Figure 9b - External Clock Connection

3.2.3 Power Supply Decoupling

Symmetric positive and negative power supplies (±5V) are required for the operation of the MT3530. Additionally, the reference voltage for Carrier Detect Threshold is derived from the ±5 V rails. Decoupling V_{CC} to DGND and V_{EE} to AGND with 0.1 µF capacitors connected close to the device supply pins is recommended.

3.2.4 Reset Protocol

By ensuring that all control inputs are in their inactive states for a minimum of 2 ms before the rising edge of DTR, the MT3530 will be properly reset.

SL (Select)	Mode	Transmit Frequency (Hz)*		Receive Frequency (Hz)*	
		Mark	Space	Mark	Space
0	Bell 103 Originate Bell 103 Answer	1270 2225	1070 2025	2225 1270	2025 1070
1	CCITT V.21 Channel 1 (Originate) CCITT V.21 Channel 2 (Answer)	980 1650	1180 1850	1650 980	1850 1180
	CCITT V.25 Answer Tone	2100			

Table 1 - BELL 103 / CCITT V.21 Operating Modes

Space = Binary 0, Mark = Binary 1, Crystal Frequency = 3.579545 MHz, *Frequency drift = ±3 Hz

3.2.5 Type Selection

MT3530 is Bell 103/113 and CCITT V.21 compatible. Table 1 illustrates the two types of operating modes. The basic principle is the same but the frequencies and the timings are switched. When in V.21 mode the V.25 Answer Tone of 2100 Hz will be generated upon answering.

3.2.6 Carrier Detect Threshold (CDT)

Applying a voltage between 0 and − 5 V_{DC} at this input allows control of the receive carrier detection threshold. This will override the internally determined threshold level of − 41 dBm for receive data carrier. Note that when the CDT pin is left open the output voltage level can vary between -1.5 V and − 4 V. Therefore, the external voltage level needed to set a required carrier detection threshold will vary from device to device.

3.2.7 Timing, Control and Handshake

The RS-232C interface feature facilitates interfacing the modem to a standard RS-232C interface in stand-alone applications or a UART in other applications where the modem is integrated into the Data Terminal Equipment. The control section, in addition, provides the capability for auto answering/origination/pulse dialing. It incorporates a 14 seconds abort timer and a loss of carrier timer which provide call termination capability.

3.3 MT3530 Phone Line Interface (PLI)

Interface of any equipment to the public switched telephone network (PSTN) is governed by the National Regulatory Agencies. There are two different ways of interfacing modems to the phone line. One of these is to use a Data Access Arrangement (DAA). In the U.S. this requires meeting FCC Part 68 Certification before connecting to the PSTN. The DAA is designed to handle the phone line interface including the 4-wire to 2-wire conversion.

Direct Connection Under FCC Rules, Part 68

The FCC registration program was created in 1975 to allow non-Bell producers of modems the right to connect their equipment directly to the public switched telephone network (PSTN). In order to comply with the requirements of Part 68 all such equipment must contain protective circuitry to provide isolation to the user equipment from the PSTN, similar to the protection formerly provided by Data Access Arrangements (DAA). FCC Rules, Part 68, requires that the protective circuitry either be an integral part of the modem and registered as the terminal device or that the protective circuitry be separate from the modem and registered as protective circuitry. Under FCC Rules, Part 68, this registration class is "Terminal Device" and equipment type is "Data Modems".

The second Public Switched Telephone Network connection scheme uses an acoustic coupler. An acoustic coupler uses the existing telephone handset and is not directly connected to the phone line.

3.3.1 Acoustic Coupling

The MT3530 can be connected to the telephone network using an acoustic coupler. Figure 10 shows how acoustic coupling is accomplished. No component values are given because the speaker and microphone impedance characteristics can vary.

Typically, the modem's transmitted carrier is amplified through a speaker and presented to the mouthpiece of a standard telephone handset. The modem received carrier signal is derived from the earpiece of the same handset by a microphone; the signal is then attenuated and presented to the modem. Note that there is a hybrid in the telephone handset that performs a 2-wire to 4-wire conversion between the public switched network and the MT3530.

The gain of the amplifier at the modem Transmit Carrier output (TC) should be adjusted such that the maximum signal power on the phone line is less than the limits set by the National Regulatory Agencies. In the U.S., this limit is − 9 dBm as measured into 600 ohms. For CCITT applications this limit is reduced to − 13 dBm. The power level on the line will be a function of a number of parameters; the modem transmit carrier output level, the gain of the external amplifier, and the characteristics of the speaker on the output of the modem transmit carrier and the handset mouthpiece.

The gain of the receive amplifier which feeds the MT3530 receive carrier should be adjusted to provide a peak signal at RC pin of no more than 0 dBm. However, it is often sufficient to compensate the gain of the receive op-amp so that signal level across the Tip and Ring is delivered to the RC pin on the MT3530 .

3.3.2 Direct Connection of Data Modems

Direct connection means that the modem is connected to the telephone line through an

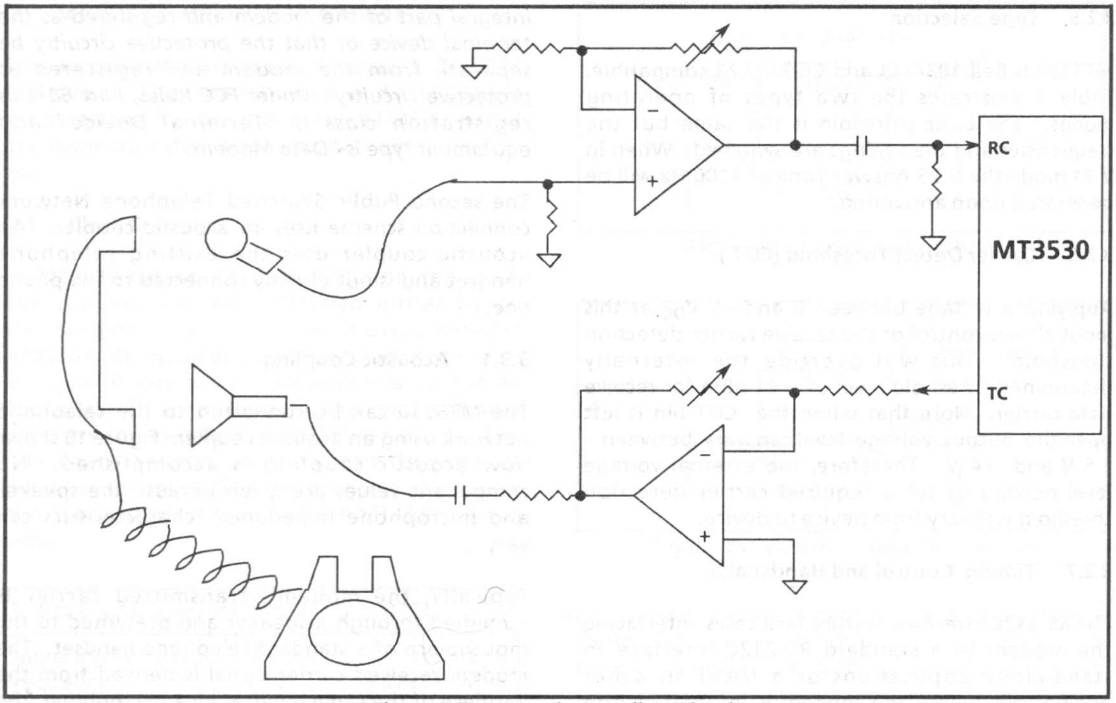

Figure 10 - Acoustic Coupling Circuit

approved interface device termed Data Access Arrangement (DAA).

The prime elements of the DAA are transmit signal level, impedance matching, line isolation, transient protection and the billing timing delay. Other functions integrated as part of the DAA include ring detect and switch-hook circuitry.

Any equipment connected to the switched telephone network must meet "permissive" or "programmable" transmit level specifications. The most commonly used is permissive specification. In this arrangement the level must not be greater than −9 dBm as measured into 600 Ω when averaged over three seconds. For CCITT applications this should be no greater than −13 dBm. The MT3530 transmit carrier output is limited at −8 ± 1 dBm.

Standard termination is defined as 600 Ω and is the reflected impedance required by the primary of the transformer. The impedance matching of the transformer (600 Ω) represents the nominal AC impedance of the phone line which changes with frequency and conductor type and size. Off-hook DC resistance of the terminal equipment circuitry is preferred to be less than 200 Ω.

Figure 11 illustrates a typical Direct Connect DAA.

A set of standard requirements for an isolation transformer is as follows:

- Primary Impedance: 600 Ω;
- Secondary Impedance: 600 Ω (nominal);
- Maximum DC Current: 90 mA (*Note 1*);
- Frequency Response: 300 - 3000 Hz ± 0.5 dB;
- DC Resistance: Preferably less than 200 Ω. This is in compliance with FCC Rules, Part. 68.31;
- Echo Return Loss: 20 dB (*Note 2*);
- Harmonic Distortion: Low (Typ. 0.1% at 300 Hz, 90 mA);
- Dielectric Strength: 1500 V AC or greater between primary and secondary. The core is to comply with FCC Rules, Part 68.302 and 68.304.

Note 1: *As an alternate design, additional electronic components may be used to shunt DC line current, thus allowing use of a smaller transformer which would only carry an AC signal component. The holding coil then provides the DC path for the holding current provided by the Central Office.*
Note 2: *Imperfections in the isolation transformer make impedance matching a complex task. Transformers for phone line isolation reflect incoming signals back into the telephone network at a reduced level. This is known as echo return loss.*

High voltage transient suppression is usually performed with bidirectional Zener diodes which limits the potential between Tip and Ring to a specified threshold (1500 V in the U.S.). The series resistor is inserted for short circuit current limiting. Zener protection may, also, be provided on the secondary side to protect modem equipment. When automatic answering the phone, Part 68 of

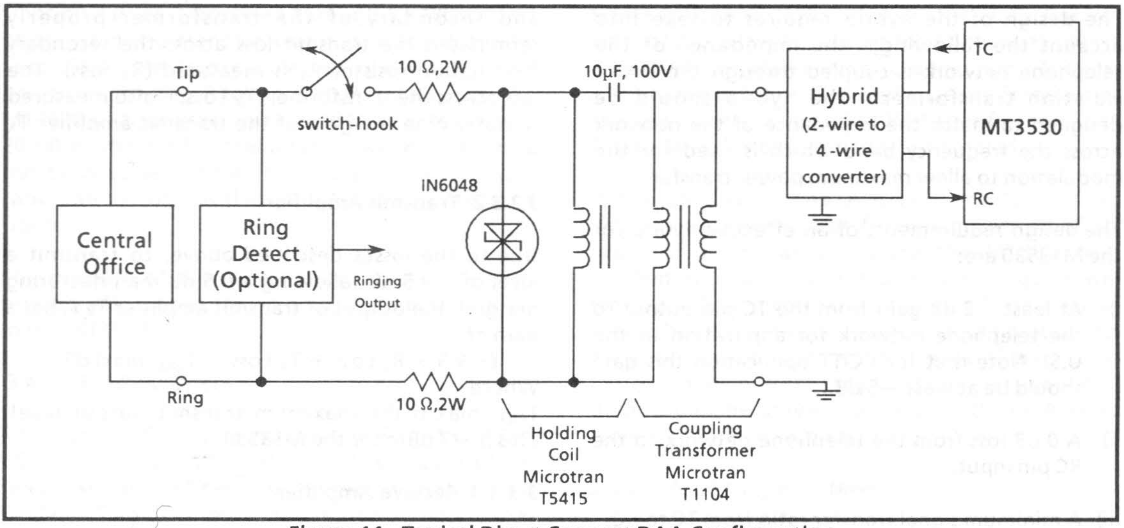

Figure 11 - Typical Direct Connect DAA Configuration

the FCC Rules specifies the user must ensure a silence (non-data) interval on the phone line of at least two seconds for billing purpose before any data or answer tone may be transmitted. CCITT specifies 1.8 to 2.5 seconds of silence. The MT3530 provides for a silence interval of 2.0 seconds mininum when in Answer mode.

The DAA circuit may be used in automatic answering applications with the addition of ringing detection circuitry. The requirements of the ring detection circuitry are as follows:

i) Meet the 1500 volt longitudinal surge requirement and 1000 volt metallic surge requirement of FCC Rules, Part. 68.302;

ii) Provide a minimum on-hook DC resistance of 10 MΩ at 100V DC and 3 kΩ at 300 V DC, and on-hook AC impedance of less than 40 kΩ but greater than 1600 Ω in compliance with FCC Rules, Part 68.312;

iii) Provide immunity to false ring detection caused by rotary dial pulses generated by other telephones which bridge the same metallic pair on the data modem;

iv) Respond to incoming ringing voltage of 40 V_{RMS} to 150 V_{RMS} at frequency of 16 Hz to 68 Hz;

v) Per Bell System Technical Reference PUB6100, the ring detection circuit should ignore valid ring bursts of 125 ms or less.

The DAA interfaces to PSTN on the Tip and Ring leads. The relay provides the on-hook/off-hook control for connection or disconnection from the line. When the DAA is off-hook, the relay is closed, loop current flows through the isolating transformer (or the holding coil) and the rest of the DAA is connected to the line. This indicates a desire to make a call or answer a call. In Answer mode once the ring signal has been detected, the modem is placed off-hook. The off-hook control line may, also, be used for pulse dialing in accordance with Bell Technical Reference PUB 1100, provided that the telephone set is on-hook.

The relay requirements nominally are:

i) Meet or exceed the criteria of FCC Rules, Part 68.302 and 68.304. These rules deal with environmental simulation and leakage current;

ii) Be available with gold capped silver palladium contacts for auto dial applications;

iii) Minimum possible power consumption;

iv) Long life rating as specified in minimum number of operations (contact transfers);

v) Rated at 75 V_{DC}, at 70 mA DC loop current and 150 V_{AC}, at 130 mA AC ring current.

3.3.3 Hybrid (Duplexor)

The receiver and transmitter of the modem require one pair of wire each for physical connection. For standard PSTN connections, only one pair of wire is available. Therefore, a duplexor or electronic hybrid (also known as 2-wire to 4- wire converter) is used to interface the modem with the telephone network.

The design of the hybrid requires to take into account the following; the impedance of the telephone network is coupled through the DAA's isolation transformer. The hybrid should be designed to match the impedance of the network across the frequency band which is used for the modulation to allow maximum power transfer.

The design requirements of an effective hybrid for the MT3530 are:

i) At least −2 dB gain from the TC pin output to the telephone network for application in the U.S. Note that for CCITT application this gain should be at least −5 dB.

ii) A 0 dB loss from the telephone network to the RC pin input.

iii) A minimum signal transfer ratio from TC to RC.

Figure 12 illustrates a hybrid circuit using operational amplifiers. The design calculations include the following: Transformer, Transmit Amplifier and Hybrid Receive Amplifier.

3.3.3.1 Transformer (T1 in Figure 12)

Standard termination is defined as 600 Ω and is the reflected impedance required by the primary of the transformer. In this design a representative transformer is selected and the secondary termination resistance is determined (equivalent to R_1) for a reflected impedance of 600 Ω at the primary.

The receive loss (R_X Loss) from primary to secondary needs to be measured and must be compensated for by the receive amplifer R_XA. With the primary and secondary of the transformer properly terminated the transmit loss across the secondary termination resistor R_1 is measured (R_1 loss). The loss across the transformer, T_X Loss, is also measured to determine the gain of the transmit amplifier T_X A.

3.3.3.2 Transmit Amplifier

Due to the losses described above, to transmit a level of −9.5 dB (allowing a 0.5 dB manufacturing margin), the output of transmit amplifier T_X A has a gain of:

$$(-9.5 + R_1 \text{ Loss} + T_X \text{ Loss} - T_{OUT} \text{ max}) \text{ dB}.$$

Where:

T_{OUT} max is the maximum transmit output level. This is −7 dBm for the MT3530.

3.3.3.3 Receive Amplifier

The hybrid receive amplifier R_XA requires that the maximum level which can be applied to the RC input of the MT3530 is 0 dB. Therefore, the voltage output of the receive amplifier should not exceed 0 dB. The receive amplifier must, also, make up for the receiver transformer amplifier loss, R_X Loss. However, it is often sufficient for the receive amplifier gain to be such that the signal across Tip and Ring is delivered to the Receive Carrier pin at the same level. The receive amplifier R_XA, then, has a gain of : R_X Loss dB.

Although, the MT3530 provides 55 dB of adjacent channel rejection, the hybrid receive amplifier can be used for additional rejection of the MT3530 transmit signal through use of differential amplifier techniques. The resistor R_2 from the Transmit Carrier pin to the inverting input of the receive amplifier is to provide side tone suppression. The

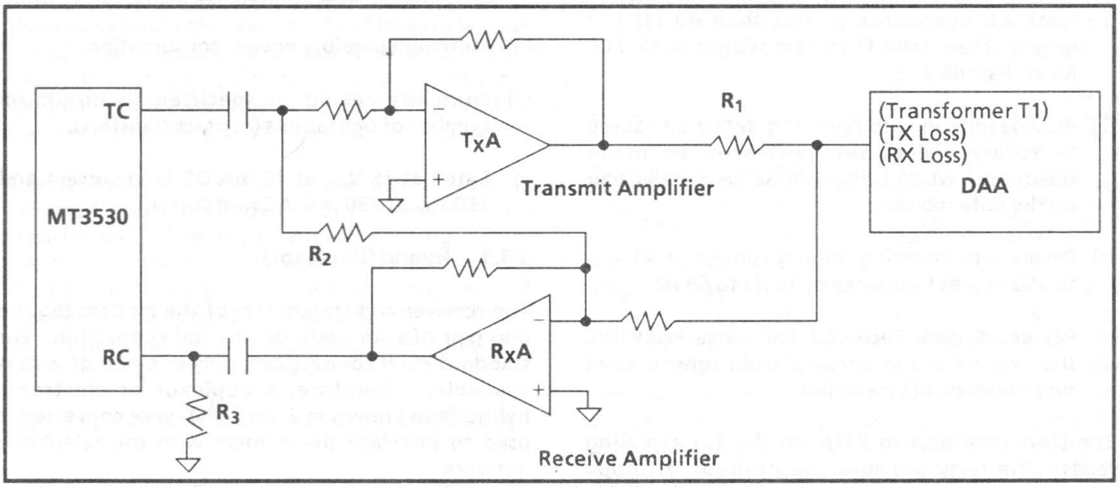

Figure 12 - Hybrid Circuit

transmit carrier is provided through R_2 180° out of phase from the transmit carrier presented to the line. Thus, the transmit carrier is cancelled and presented to the Receive Carrier input on the MT3530 at a reduced level. Under ideal conditions 20 dB or more of cancellation might be achieved, but because telephone lines vary considerably, a cancellation not less that 10 dB is a more realistic figure.

The purpose of the termination resistor R_3 is to provide a DC bias to the op amp of the receive filter in the MT3530.

3.4 MT3530 Operation

The modem I.C. may be operated in Bell 103/113 or CCITT V.21 type applications. Logic control on select (SL) pin defines the operating mode. See Table 1. Two diagnostic modes, analog and digital loopback, allow for system tests. Refer to Section 5.0 for details. In addition, Passthru mode is available in which the timing and the protocol handshake depedence can be suspended.

3.4.1 Auto Answer

In the Answer mode the MT3530 stands idle waiting for an incoming call. To assist in answering incoming calls, the ring indicate signal (RI) from DAA is connected to the $\overline{RI}$ pin of the MT3530. With DTR High and RTS Low, a Low from the ring detector to $\overline{RI}$ causes the MT3530 to initiate Auto Answer sequence by setting $\overline{OH}$ and $\overline{DSR}$ Low (See Figure 13). $\overline{OH}$ Low enables the hookswitch relay, thereby, connecting the modem to the telephone line. The duration of $\overline{RI}$ Low should be greater than 107 ms . Otherwise, the device will disable $\overline{OH}$ and disconnect the telephone line. The modem commences 2.0 seconds (minimum) of silence followed by Answerback Tone. This is a 2225 Hz (Mark) carrier when operating in Bell 103 mode. The generation of Answer Tone continues until:

i) The 1270 Hz (Mark) carrier from the originating modem is detected and the answering modem automatically picks up within 100 ms by setting $\overline{CD}$ and $\overline{CTS}$ Low. This completes the handshaking sequence and communication is established;

or

ii) DTR is set Low. See Reset Protocol in Section 3.2.4 for details.

If no Answer Tone is detected within 14 seconds of being put into the Answer mode, the modem will abort the call. Refer to Auto Abort section 3.4.3 for details.

When operating in V.21 mode the V.25 Answer Tone of 2100 Hz is generated for 3.4 seconds. 80 ms later 1650 Hz (Mark) carrier is generated. The rest is the same as Bell 103 except that the frequencies and timings are switched to V.21 specification. See Figure 14 and Table 1 for additional details.

If the chip is in the Answer mode and an originating modem, not following Bell or CCITT protocol, sends carrier before the MT3530 has finished the Auto Answer sequence the modem will lock-up. This means that there will be Carrier Detect but handshaking will not be completed and data will not be transferred. This is of particular importance in V.21 application because the duration of the answer sequence with the Answer Tone is almost six seconds.

3.4.2 Auto Originate Mode

With DTR High, a call is initiated by applying a High to the RTS input. This will cause $\overline{OH}$ to go Low, enabling the hook-switch relay and connecting the telephone line. This puts the MT3530 in the Auto Originate mode. When dial tone is detected, RTS can be pulsed Low/High to provide dial pulses. The $\overline{OH}$ will follow the RTS pulses, sending the desired digits over the telephone line. The proper timing for dialing must come from the Data Terminal on the RTS line.

When the answering modem comes on line it will wait for 2.0 seconds ("billing" delay) and then send the 2225 Hz Answer Tone for Bell 103 operating mode. Refer to Figure 13. Note that if the answering modem sends a carrier within 2.0 seconds the modem will lock-up. The $\overline{CD}$ pin output on the originating modem will go Low 200 ms (max.) later indicating received carrier. 236 ms (max.) later, the MT3530 will respond with 688 ms (max.) of 1270 Hz carrier. At the end of that time $\overline{CTS}$ (Clear-To-Send) will go Low indicating to the Data Terminal Equipment that the communication link has been established. If no carrier is detected within 14 seconds of being put into Originate mode, the modem will abort the call.

When in V.21 mode, the principle is the same but the frequencies and timings are switched to V.21 specifications. See Figure 14 and Table 1 for additional details.

3.4.3 Auto Abort

There is an automatic abort feature in the MT3530 to avoid tying up a system when there is a difficulty in establishing the link. If no carrier is detected within 14 seconds after the device has been put into the Answer or Originate mode it will abort the call

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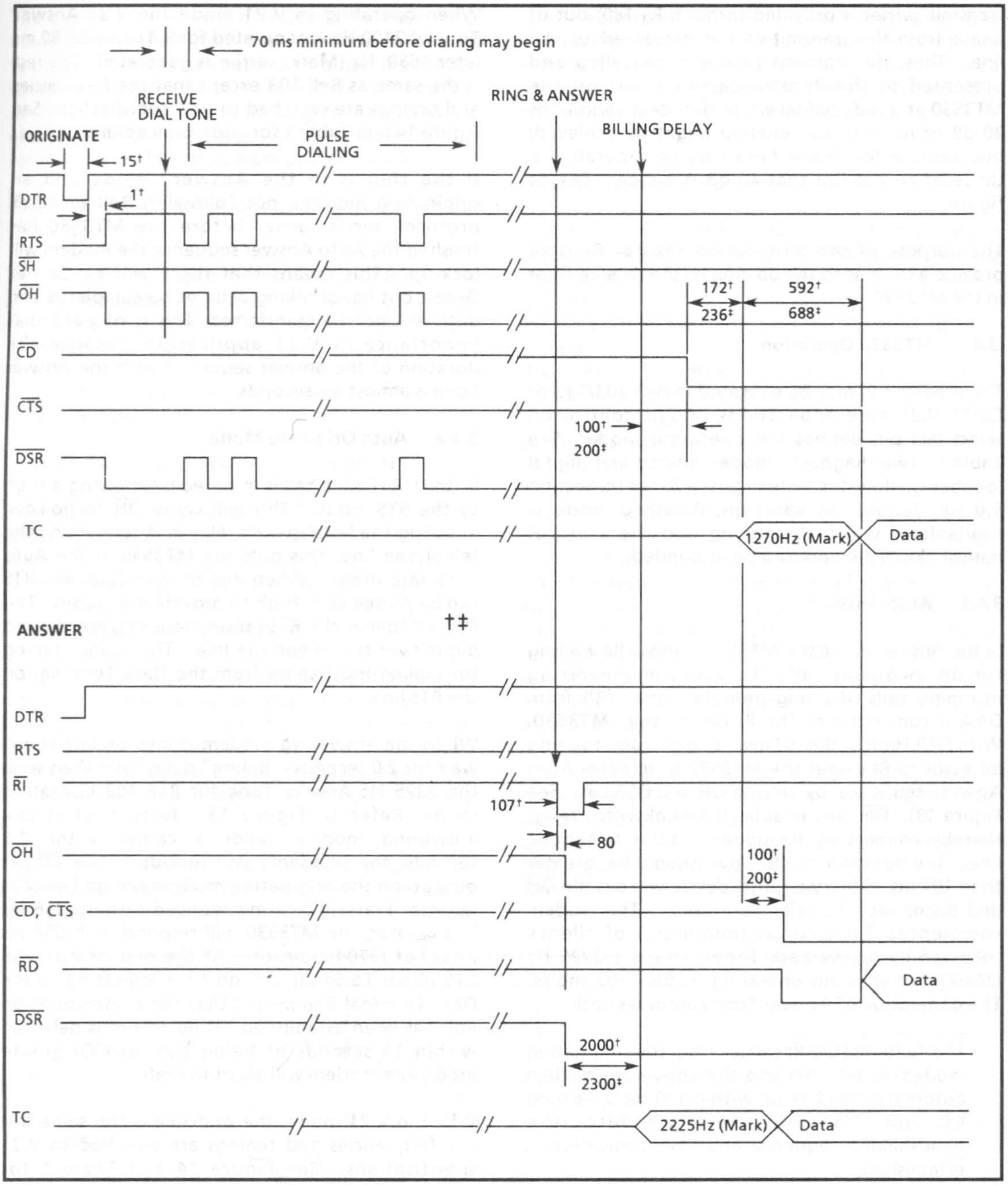


Figure 13 - MT3530 Modem Timing* Chart for Bell 103 Operating Mode

* All timing is in milliseconds and the value is typical unless specified.
† Denotes the minimum value.
‡ Denotes the maximum value.

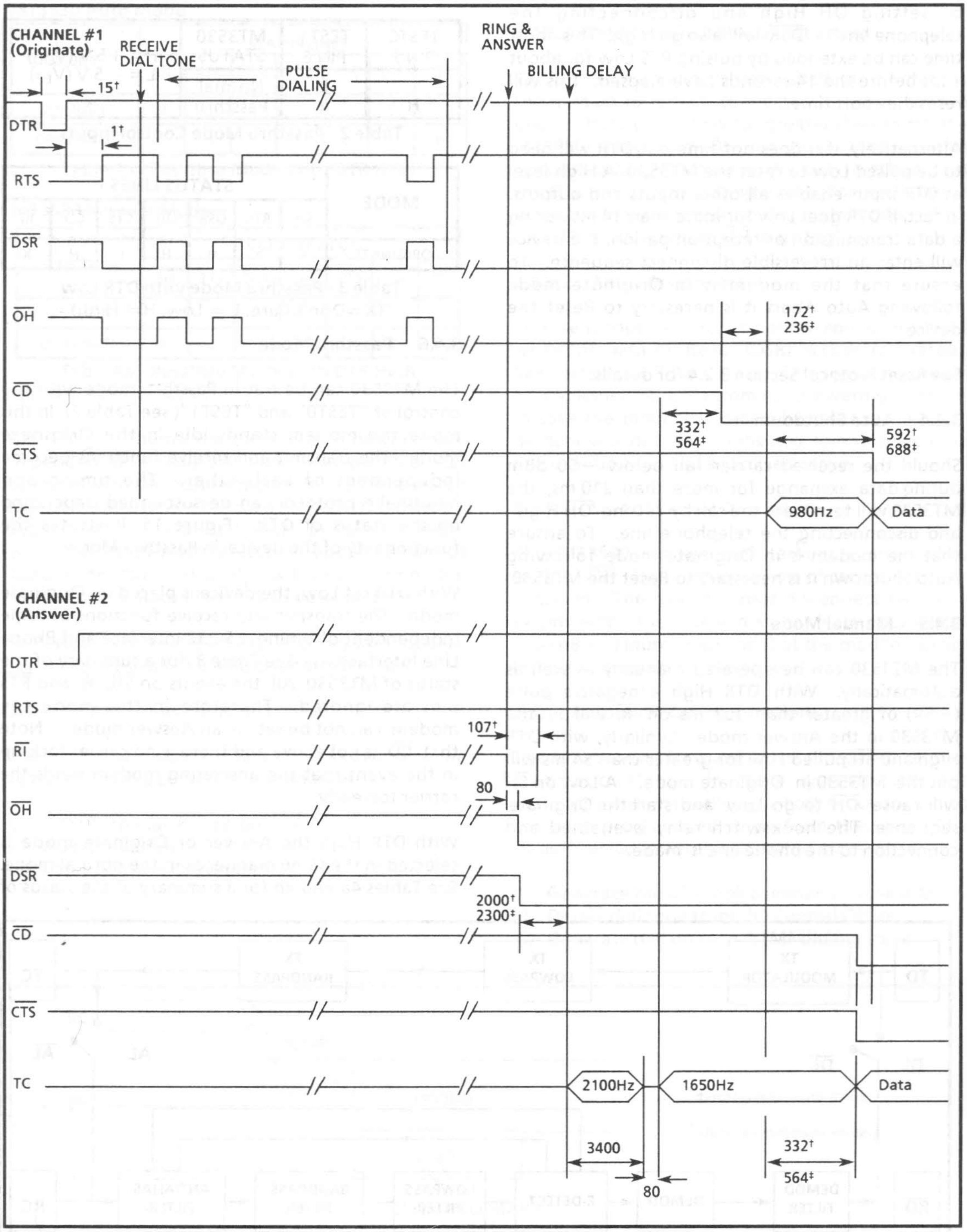


Figure 14 - MT3530 Modem Timing* Chart for CCITT V.21 Operating Mode

* All timing is in milliseconds and the value is typical unless specified.

† Denotes the minimum value.

‡ Denotes the maximum value.

by setting $\overline{OH}$ High and disconnecting the telephone line. $\overline{DSR}$ will also go High. This abort time can be extended by pulsing RTS Low for about 1 ms before the 14 seconds have elapsed. This will reset the abort timer.

Alternatively, if it does not time out DTR will need to be pulsed Low to reset the MT3530. A High level at DTR input enables all other inputs and outputs. In fact, if DTR goes Low for more than 14 ms during a data transmission or reception period, the device will enter an irreversible disconnect sequence. To ensure that the modem is in Originate mode following Auto Abort it is necessary to Reset the device.

See Reset Protocol Section 3.2.4 for details.

3.4.4 Auto Shutdown

Should the received carrier fall below −50 dBm during data exchange for more than 210 ms, the MT3530 will terminate the call by setting $\overline{OH}$ High and disconnecting the telephone line. To ensure that the modem is in Originate mode following Auto Shutdown it is necessary to Reset the MT3530.

3.4.5 Manual Mode

The MT3530 can be operated manually as well as automatically. With DTR High a negative pulse (−5V) of greater than 107 ms on $\overline{RI}$ will put the MT3530 in the Answer mode. Similarly, with DTR High and $\overline{SH}$ pulled Low for greater than 54 ms will put the MT3530 in Originate mode. A Low on $\overline{SH}$ will cause $\overline{OH}$ to go Low and start the Originate sequence. The hookswitch relay is enabled and connection to the phone line is made.

TEST0 PIN 7	TEST1 PIN 6	MT3530 STATUS	H = +5 V (V_{DD}) L = − 5 V (V_{EE})
L	L	Normal	
H	L	Passthru	

Table 2 - Passthru Mode Control Inputs

MODE	STATUS LINES †						
	$\overline{SH}$	RTS	$\overline{DSR}$	$\overline{OH}$	$\overline{CTS}$	$\overline{CD}$	$\overline{RI}$
ORIGINATE	X	X	H	H	L	H	X

Table 3 - Passthru Mode with DTR Low
†(X = Don't Care, L = Low, H = High)

3.4.6 Passthru Mode

The MT3530 can be put in Passthru mode with the control of "TEST0" and "TEST1" (see Table 2). In this mode the modem stands idle in the Originate mode. The transmit and receive functions become independent of each other. The timing and handshake protocol can be suspended depending on the status of DTR. Figure 15 illustrates the functionality of the device in Passthru Mode.

With DTR set Low, the device is placed in Originate mode. The transmit and receive functions become independent of timing, RS-232 Interface and Phone Line Interface. See Table 3 for a summary of the status of MT3530. All the events on $\overline{SH}$, $\overline{RI}$ and $\overline{RTS}$ pins are ignored. Therefore in this mode the modem can not be set in an Answer mode. Note that $\overline{CD}$ is not active and there is no carrier lock-up in the event that the answering modem sends the carrier too early.

With DTR High the Answer or Originate mode is selected in the same manner as in the normal mode. See Tables 4a and 4b for a summary of the status of

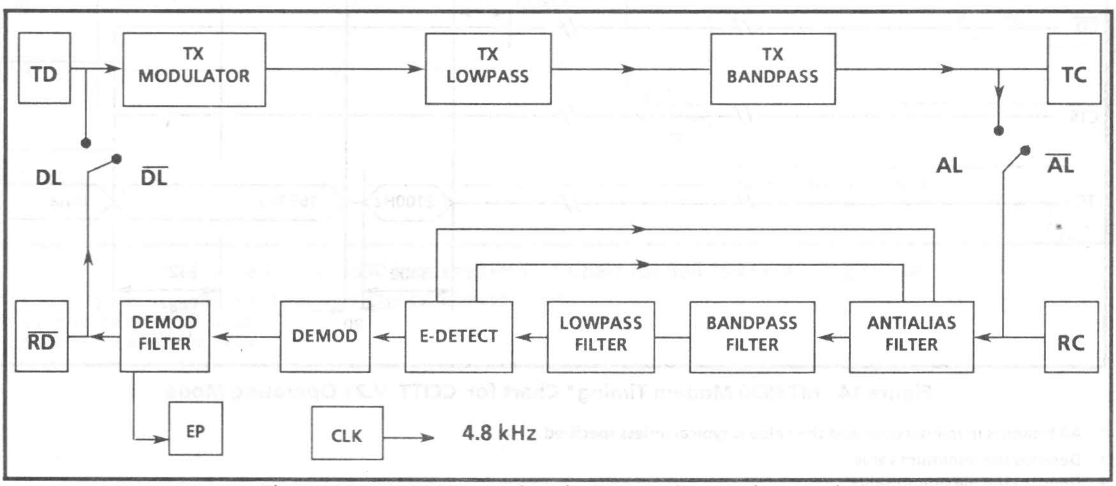


Figure 15 - MT3530 Functional Diagram in Passthru Mode

MT3530 Auto Mode

MODE	STATUS LINES †						
	$\overline{SH}$	RTS	$\overline{DSR}$	$\overline{OH}$	$\overline{CTS}$	$\overline{CD}$	RI
ANSWER	H	L	L	L	L	L	L
ORIGINATE	H	H	L	L	L	L	H

Table 4a - Passthru Mode with DTR High

MT3530 Manual Mode

MODE	STATUS LINES †						
	$\overline{SH}$	RTS	$\overline{DSR}$	$\overline{OH}$	$\overline{CTS}$	$\overline{CD}$	$\overline{RI}$
ANSWER	H	L	L	L	L	L	L
ORIGINATE	L	L	L	L	L	L	H

Table 4b - Passthru Mode with DTR High

†(L = Low, H = High)

MT3530. The transmit and receive functions are dependent on timing and handshake protocol. $\overline{CD}$ operates as in the normal mode. It should be noted that, if a Space is sent before a Mark, $\overline{CD}$ will not be active until it sees a Mark first. In Passthru mode with DTR High Auto Shutdown applies where as Auto Abort does not apply. After call termination the modem is placed in the Originate mode.

In Passthru mode the analog and digital loopback functions are available as in the normal mode.

3.4.7 Call Termination Procedures

The MT3530 modem offers the following three features which permits call termination:

i) Data Terminal Ready not active
ii) Abort Disconnect
iii) Loss of Carrier Disconnect

3.4.7.1 Data Terminal Ready not active

The DTR signal must be High (active) in order for the modem to remain connected to the telephone line. If DTR is set Low for greater than 15 ms, the MT3530 resets and $\overline{OH}$ pin goes High. This disconnection procedure is the only method that the DTE has of terminating a call. The exception is when the modem is in Auto Originate mode. In this case RTS Low will cause $\overline{OH}$ to go High.

3.4.7.2 Abort Disconnect

This sequence is not an option and is employed when the Data Set Ready ($\overline{DSR}$) is Low (activated). See Section 3.4.3 for details. This sequence should be implemented on automatic answering modems in case the modem is called by mistake, i.e., the modem will not stay connected to the telephone line in anticipation of a received carrier.

3.4.7.3 Loss of Carrier Disconnect

The MT3530 modem will terminate the call by setting $\overline{OH}$ High when a loss of carrier energy is detected. The loss of carrier disconnect sequence begins when the received signal level goes below −50 dBm. Figure 16 shows that the modem carrier loss disconnect timing diagram.

3.5 Automatic Calling Functions

The MT3530 can be used in systems which require automatic calling. In these systems, calls are generated automatically by a host processor which has been programmed to perform the tasks. The steps involved in automatic calling are:

i) Generate the off-hook command to the DAA
ii) Detect dial tone from the Central Office
iii) Generate dial pulse or DTMF dialing tones

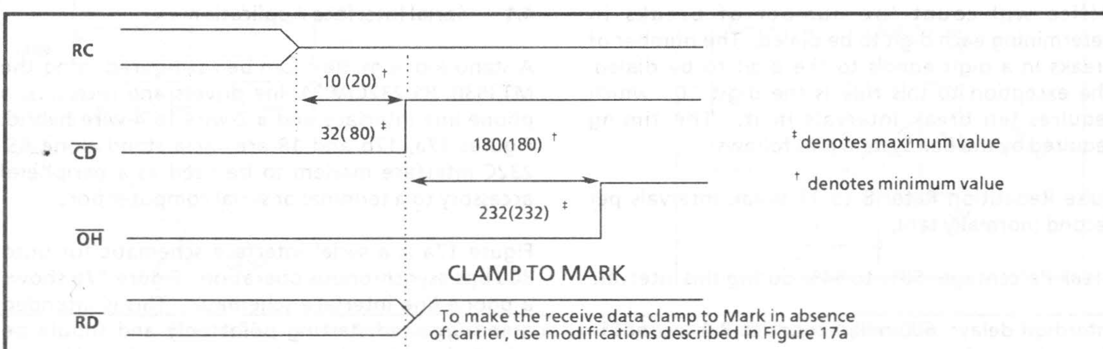


Figure 16 - Carrier Loss Disconnect Timing * Diagram

*Bell 103 (CCITT V.21) timing is in milliseconds

iv) Detect remote modem Answer Tone
v) Transmit data

3.5.1 Generation of Off-Hook

In automatic calling systems, normally the connection to the phone line is controlled by an off-hook relay lead. With DTR High, and a High applied to the RTS input, $\overline{OH}$ pin 24 will go Low. This enables the hook-switch relay and connects the telephone line. This puts MT3530 in the Auto Originate mode.

3.5.2 Dial Tone Detection

After going off-hook, the C.O. will provide dial tone to the subscriber. In modern central offices which accept DTMF dialing, the C.O. will provide a "precise" dial tone which is a composite of 350 and 400 Hz. In older central offices which do not accept DTMF dialing it is difficult to predict exactly what the frequency spectrum of the dial tone will look like. It is nominally in the 300 to 700 Hz range. A call progress detection chip is required.

It is assumed that if automatic calling functions are performed there is a host processor in the system which can provide the control. Once dial tone has been detected by the host processor, dialing may begin.

3.5.3 Dial Pulsing

Pulse dialing is the process of opening (breaking) and closing (making) the loop connection. This is accomplished in MT3530 by pulsing RTS Low/High to provide dial pulses. The $\overline{OH}$ will follow the RTS pulses. The proper timing for dialing must come from the Data Terminal or Host Processor on the RTS line.

If the making and breaking of the loop conforms to requirements set by the Bell System, the Central Office will count the number of breaks in determining each digit to be dialed. The number of breaks in a digit equals to the digit to be dialed. The exception to this rule is the digit "0" which requires ten break intervals in it. The timing required by the Bell System is as follows:

Pulse Repetition Rate: 8 to 11 break intervals per second (normally ten);

Break Percentage: 58% to 64% during this interval;

Interdigit delay: 600 milliseconds to 3.0 seconds in the make condition.

3.5.4 DTMF Dialing

The easiest way of generating DTMF tones is to use a DTMF tone generator integrated circuit.

3.5.5 Answer Tone Detection

After the host processor has dialed the desired number, a number of events may occur. Assuming that the call goes through, the remote (answer) modem will provide an Answer Tone to the calling (originate) modem. When an Answer Tone is detected by the MT3530, $\overline{CD}$ pin output will go Low. When in Bell 103 mode, the Answer Tone is 2225 Hz carrier (Mark). This will set $\overline{RD}$ pin output of the MT3530 High. The 2100 Hz Answer Tone is followed by 1650 Hz carrier. This causes the $\overline{CD}$ pin output to go Low and the $\overline{RD}$ pin will be Low. Once an Answer Tone has been detected the calling modem responds with transmit carrier. This is a 1270 Hz carrier (Mark) for Bell 103 operation and 980 Hz carrier (Mark) for V.21 operation. Data exchange may begin after detection of an Answer Tone by the far end (answering) modem. Refer to Figures 13 and 14 for timing details.

If Answer Tone is not detected by the MT3530 after a user determined length of time, the host processor may retry the call later. See Section 3.4.3 for details.

4.0 MT3530 Modem System Configurations

The MT3530 can be interfaced to either parallel or serial I/O ports of standard data terminal equipment. Connection to an intelligent terminal or serial computer port is accomplished using only line receivers and drivers. An Asynchronous Communications Interface Adapter (ACIA) is required to connect the MT3530 modem system to a parallel microcomputer bus.

4.1 Serial Interface Application

A stand-alone modem can be configured using the MT3530, RS-232C/V.24 line drivers and receivers, a phone line interface and a 2-wire to 4-wire hybrid. Figures 17a, 17b and 18 are for a stand-alone RS-232C interface modem to be used as a peripheral accessory to a terminal or serial computer port.

Figure 17a is a serial interface schematic for upto 300 bps asynchronous operation. Figure 17b shows a phone line interface schematic. This is intended as a suggested starting point only and should be adapted to fit each particular application. It is not FCC Part 68 approved.

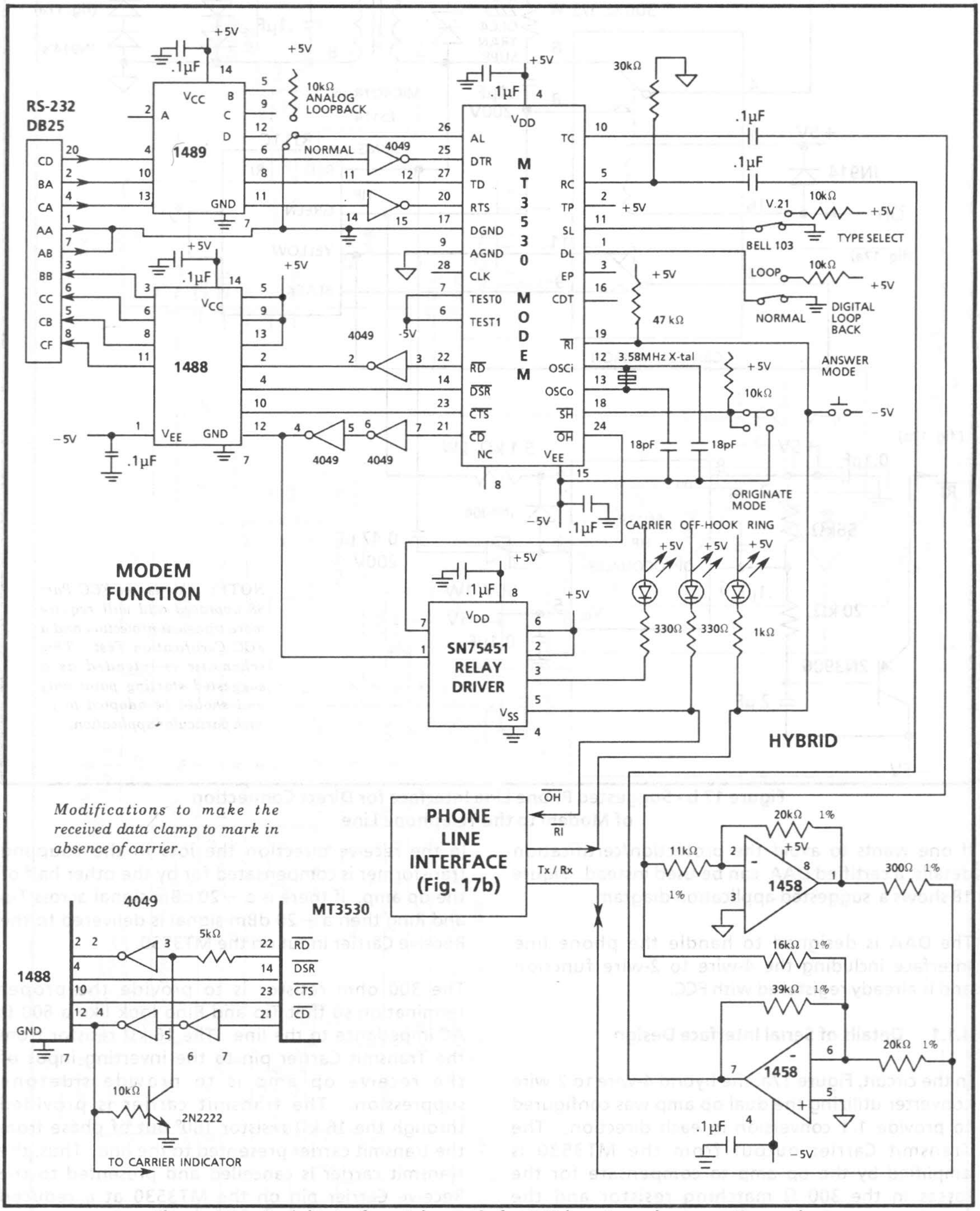


Figure 17a - Serial Interface Schematic for 300 bps Asynchronous Operation

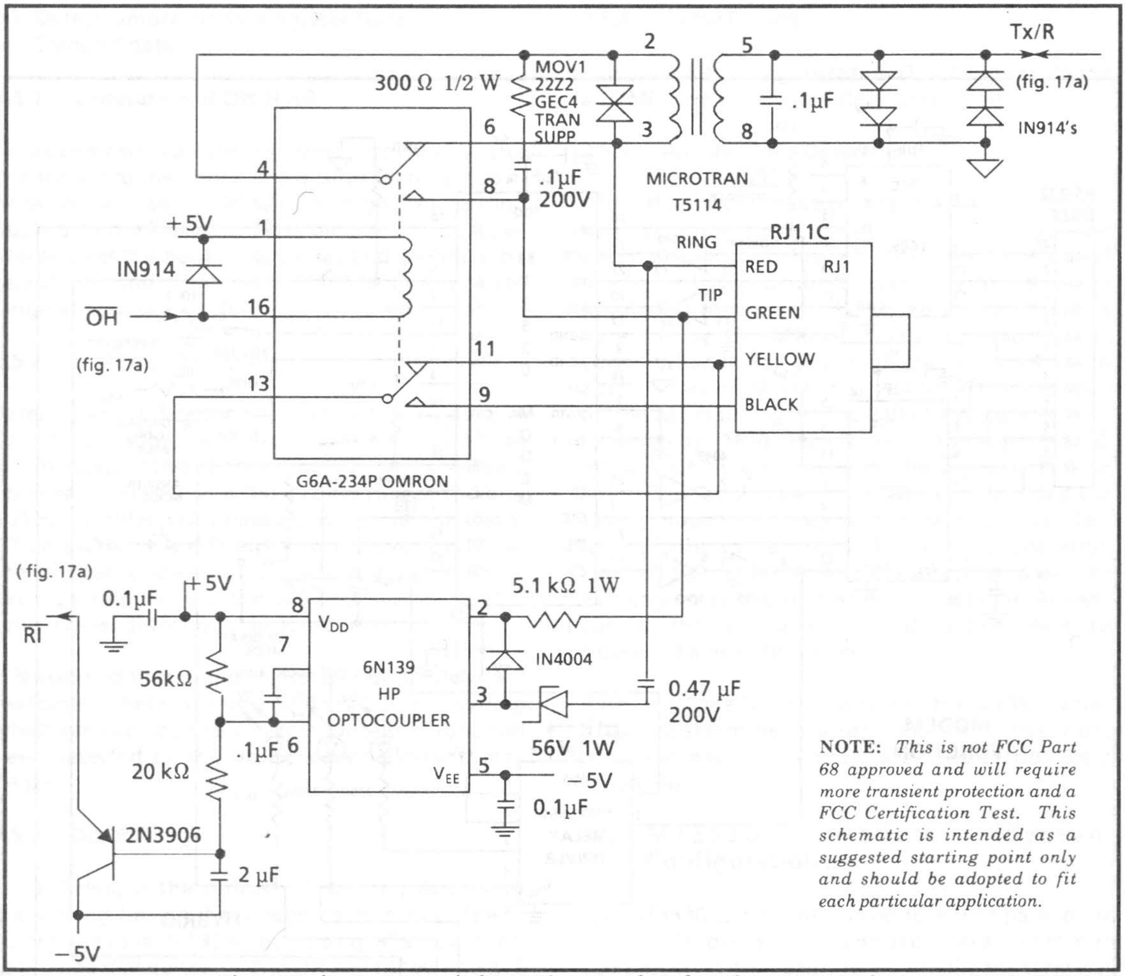


Figure 17 b - Suggested Phone Line Interface for Direct Connection of Modem to the Telephone Line

If one wants to avoid the protection/certification details, a certified DAA can be used instead. Figure 18 shows a suggested application diagram.

The DAA is designed to handle the phone line interface including the 4-wire to 2-wire function and is already registered with FCC.

4.1.1 Details of Serial Interface Design

In the circuit, Figure 17a, the hybrid 4-wire to 2-wire converter utilizing the dual op amp was configured to provide 1:1 conversion in each direction. The Transmit Carrier output from the MT3530 is amplified by the op amp to compensate for the losses in the 300 Ω matching resistor and the coupling transformer. The transmit carrier is delivered to the line at −9 dBm. For CCITT applications this should be reduced to −13 dBm.

In the receive direction the loss in the coupling transformer is compensated for by the other half of the op amp. If there is a −20 dBm signal across Tip and Ring then a −20 dBm signal is delivered to the Receive Carrier input on the MT3530.

The 300 ohm resistor is to provide the proper termination so that Tip and Ring look like a 600 Ω AC impedance to the line. The 16 kΩ resistor from the Transmit Carrier pin to the inverting input of the receive op amp is to provide sidetone suppression. The transmit carrier is provided through the 16 kΩ resistor 180° out of phase from the transmit carrier presented to the line. Thus, the transmit carrier is cancelled and presented to the Receive Carrier pin on the MT3530 at a reduced level.

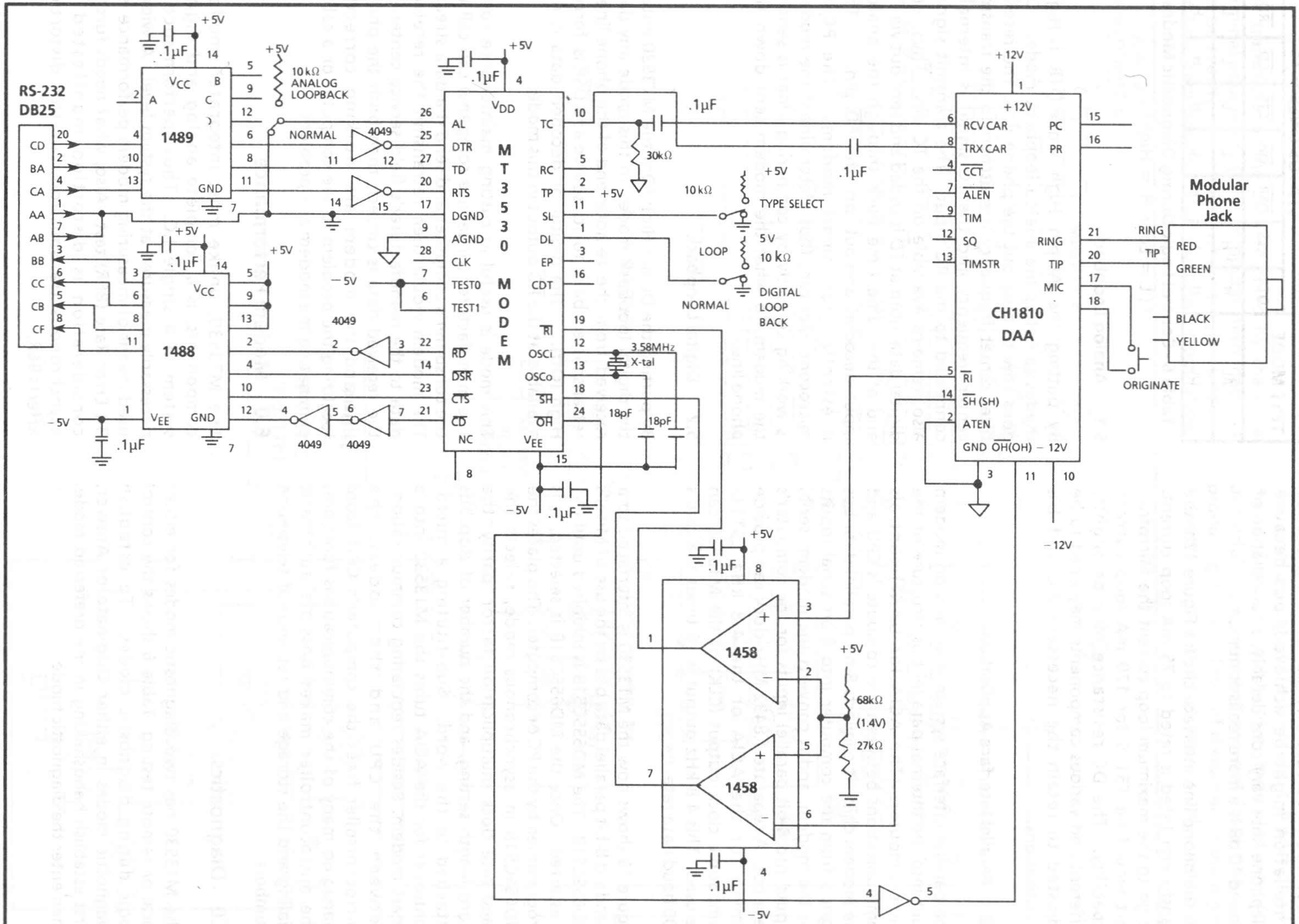


Figure 18 - Suggested Application Schematic Using Part 68 Certified DAA

Under ideal conditions 20 dB or more of cancellation might be achieved, but because telephone lines vary considerably, a cancellation of around 10 dB is a more realistic number.

For the phone line interface circuit, Figure 17b, the transformer listed is rated to 75 mA loop current. To go to the maximum loop current the Microtran part would be T5115 for 120 mA loop current capability. The DC resistance may be slightly different and various components may need to be adjusted to retain the necessary AC and DC specifications.

4.2 Parallel Interface Application

The parallel interface system is an add-on modem built into the internal parallel bus structure of the microcomputer. The ACIA (or UART) controls communications between the computer's CPU and the modem chip. It converts 8-bit parallel data bus signals from the computer into 8-bit serial inputs for the modem, and it converts the modems serial inputs into 8-bit parallel inputs for the computer's data bus. A separate 1.8432 MHz clock can provide timing for the ACIA or the 4.8 kHz LSTTL-compatible clock output (CLK) of the MT3530 can be used. This 4.8 kHz output is 16 times the chip's 300 baud data rate.

Figure 19 shows how the MT3530 is interfaced to a standard 8-bit parallel data bus by the use of Mitel's MD65SC51B. The MD65SC51B is inhibited until CS1 is asserted. Once the MD65SC51B is selected, it is programmed by the PC or computer. This places the MD65SC51B in asynchronous mode, selects the baud rate clock multiplication factor, parity, the word length setting, and the number of stop bits attached to the word. Substituting a micro-controller for the ACIA turns the MT3530 into a smart modem. Besides regulating communications between the CPU and the modem, the microcontroller frees the computer's CPU from managing many of the communications functions. The microcontroller makes possible automatic dialing and the storage and retrieval of telephone numbers.

5.0 Diagnostics

The MT3530 has two diagnostic modes for either local or remote testing. Table 6 shows the control logic during diagnostic modes. To establish diagnostic modes in either Originate or Answer, first establish handshaking in the preferred mode, then enter the diagnostic mode.

TEST MODE	STATUS LINES †						
	DTR	RTS	$\overline{DSR}$	$\overline{OH}$	$\overline{CTS}$	$\overline{CD}$	$\overline{RD}$
AL	H	H	L	L	L	L	L
DL	H	H	H	L	H	H	H

Table 6 - Control Logic During Diagnostic Modes
†(L = Low, H = High)

5.1 Analog Loopback

By putting the AL pin High while DTR is High, thedevice enters the analog loopback mode. $\overline{OH}$ goes Low to busy out the phone line. The receive filter center frequency is switched to the transmit center frequency and the TC signal is internally connected to the RC input. The transmit signal, also, remains available on the TC pin. Thus, any digital data input at TD is coded and sent out via TC, and at the same time back through the analog input, decoded, and out on the $\overline{RD}$ pin. This is essential for smart modems. The PC or microcontroller can, thus, determine if the modem is working correctly by comparing what is sent to the modem, to what the modem sent down the phone line.

5.2 Digital Loopback

By putting the DL pin High (On) the MT3530 enters the digital loopback mode. In this mode any data received from the remote end of the phone line is retransmitted back to its source and $\overline{DSR}$ is forced High (Off). The digital or decoded data is not available at the $\overline{RD}$ output in this mode.

This mode is useful in cutting maintenance costs. The manufacturer (or service company) can call up the consumer's computer and send it a data stream. The modem would then retransmit the received data to the manufacturer's field service center. If the received data is correct, then both the phone line and the modem are working correctly, localizing the problem to the computer or a cable, eliminating the modem as a problem.

6.0 Modem Performance

The MT3530, unlike most integrated modem components, is a complete analog and digital system in a single I.C. Thus, performance is necessarily measured at the system level. A widely used means of measuring modem performance is a Bit Error Rate (BER) test. Also, what needs further consideration is distortion manifested in asynchronous transmission, for this distortion affects BER.

6.1 Asynchronous Modem Distortion

The transitions in the data received by the data terminal equipment (CPU, computer, terminal) will not be exactly at the points where they occurred in the test transmission. This is because modulation, network imperfections and demodulation affect the analog carrier adversely. Additionally, transitions in both the modulation and demodulation processes are not instantaneous, producing another form of distortion in the digital waveform. While this distortion is only manifested

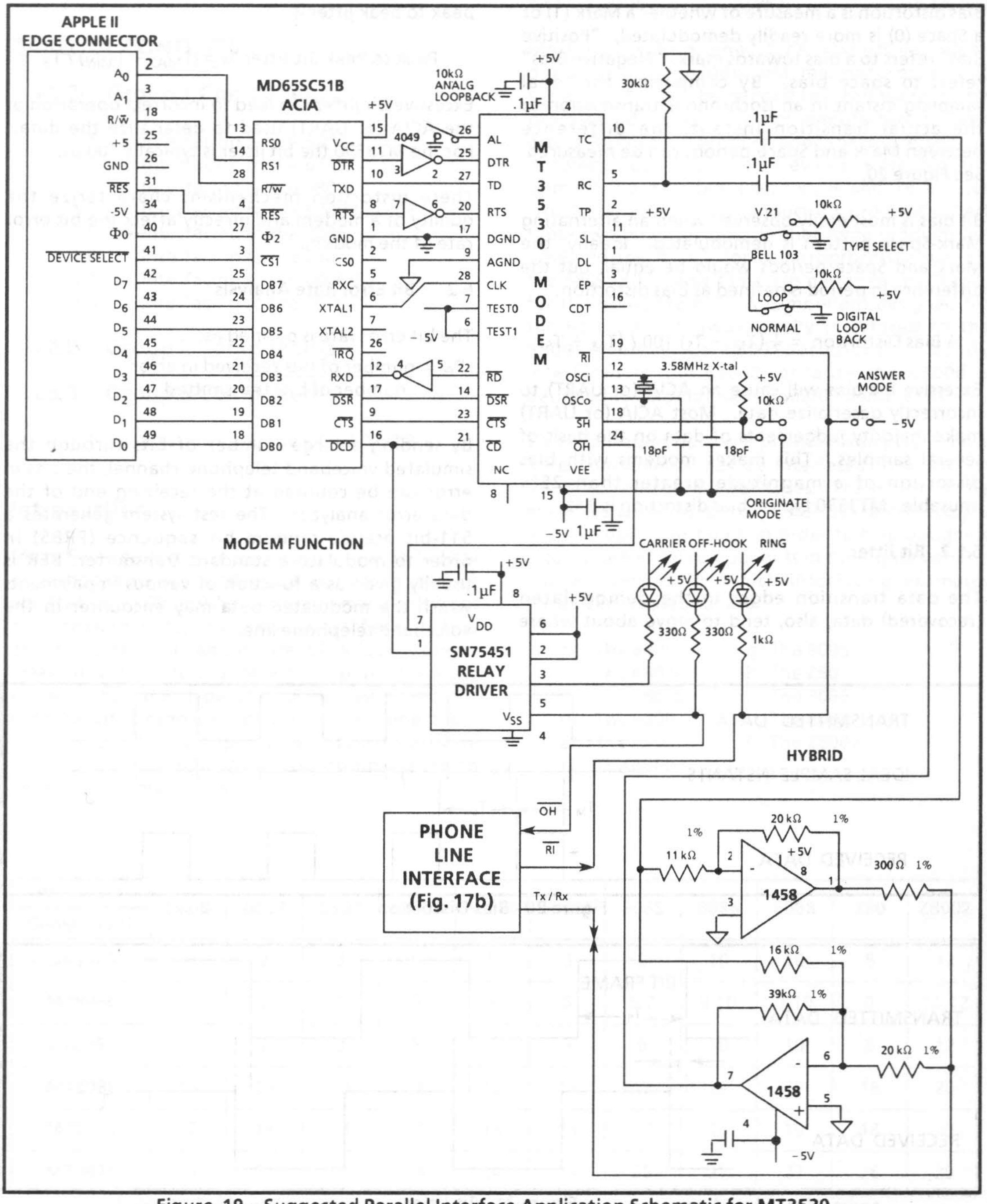


Figure 19 - Suggested Parallel Interface Application Schematic for MT3530

in asynchronous transmission there are various names and definitions given to this digital distortion. Two of the best known forms of digital distortion are: bias distortion and bit jitter.

6.1.1 Bias Distortion

Bias distortion is a measure of whether a Mark (1) or a Space (0) is more readily demodulated. "Positive Bias" refers to a bias towards mark. "Negative Bias" refers to space bias. By comparing the ideal sampling instant in an isochronous transmission to the actual transition instant, the difference between Mark and Space periods can be measured. See Figure 20.

Bit bias is most easily observed when an alternating Mark-Space pattern is demodulated. Ideally, the Mark and Space periods would be equal, but the difference in period is defined as bias distortion:

$$\% \text{ Bias Distortion} = \tfrac{1}{2}(T_M - T_S)\ 100 / (T_M + T_S)$$

Excessive bit bias will cause an ACIA (or UART) to incorrectly deserialize data. Most ACIA (or UART) make majority judgements of data on the basis of several samples. This makes modems with bias distortion of a magnitude greater than 25% unusable. MT3530 typical bias distortion is 3 %.

6.1.2 Bit Jitter

The data transition edges in the demodulated (recovered) data, also, tend to move about where they should ideally be, leading to bit jitter. See Figure 21.

$$\text{Bit Jitter} = T_{MAXIMUM} - T_{MINIMUM}$$

The bit jitter is usually specified in percent, indicating what percentage of the bit frame the peak to peak jitter is.

$$\text{Peak to Peak Bit Jitter } \% = (T_{MAX} - T_{MIN}) / T_B$$

Excessive bit jitter can lead to incorrect operation of the ACIA (or UART) used to deserialize the data. For the MT3530 the bit jitter is typically 100 µs.

These distortion mechanisms characterize the quality of a modem and directly affect the bit error rate of the modem.

6.2 Bit Error Rate Analysis

The bit error rate is defined as:

$$P_e = \frac{\text{number of bits received in error}}{\text{number of bits transmitted}}$$

By sending a large number of bits through the simulated voiceband telephone channel, the bits in error can be counted at the receiving end of the data error analyzer. The test system generates a 511-bit pseudo-random bit sequence (PRBS) in order to modulate a standard transmitter. BER is usually given as a function of various impairments which the modulated data may encounter in the voiceband telephone line.

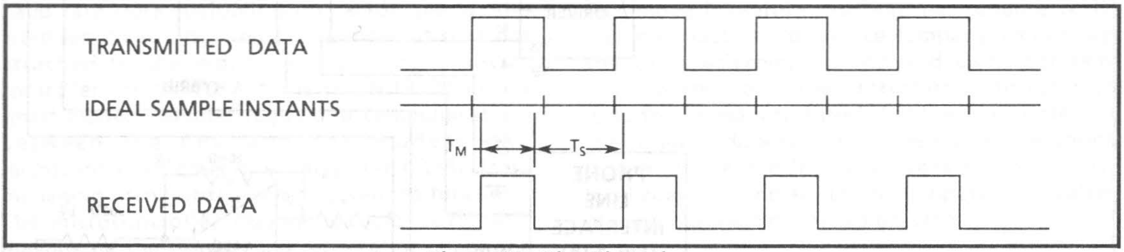


Figure 20 - Bias Distortion

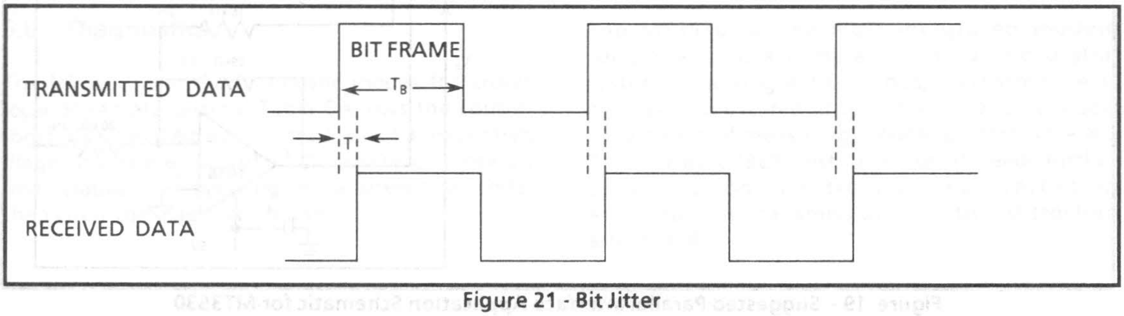


Figure 21 - Bit Jitter

Application Note **MSAN-119**

How to Interface Mitel Components to Microprocessors

9161-001-028-NA ISSUE 1 January 1986

TABLE OF CONTENTS

Introduction

Mitel Semiconductor manufactures a wide variety of components oriented towards microprocessor applications. Obviously, there are many different microprocessors, and many different bus architectures. This abundance of unique designs makes it difficult to interface a component directly to more than one type of microprocessor without running into complications for at least one type. The purpose of this application note is to provide assistance in interfacing Mitel components to various microprocessors.

Most of Mitel Semiconductor's products have been designed around Motorola microprocessors, so extra circuitry may be needed to interface to microprocessors designed by other manufacturers. Even across Motorola's product line, there are several different bus structures in evidence (segmented primarily by data bus size, i.e., 8 and 16 bit bus structures). Mitel Semiconductor's products reflect these two bus structures, in that some products are designed specifically for a microprocessor such as the 6809 (8 bit) and some are designed specifically for the 68000 (16 bit). A component designed for the 68000 is not always easily interfaced to the 6809, however, a 6809 peripheral is easily interfaced to the 68000, because the 68000 is designed to accommodate 6802/09 peripherals.

This application note will provide examples of how Mitel components may be interfaced to several of the major microprocessor types. The intent of the examples is to categorize interface architectures and microprcessor types, in order to help designers incorporate Mitel components in their systems. The microprocessors for which interfacing examples have been created for are:

- a/ The 68000
- b/ The 68010
- c/ The 68008
- d/ The 6809
- e/ The 6802
- f/ The 6800
- g/ The 8085
- h/ The Z80
- i/ The 8086
- j/ The 8088
- k/ The Z8002

Processor / Component	6800	6802	6809	68000	68010	68008	8085	8086	8088	Z80	Z8002
MD65SC51	4	2	3	5	5	5	6	10	10	8	12
MT8880	4	2	3	5	5	5	6,7	9,10	9,10	8	11,12
MT8952	4	2	3	5	5	5	6	10	10	8	12
MT8980	15	14	13	16	16	16	17	19	19	18	20
MT8981	15	14	13	16	16	16	17	19	19	18	20
MT8920	23	22	21	24	24	24	25	27	27	26	28

Table 1 - Table of Circuits Cross Referenced by Microprocessor and Mitel Part Number

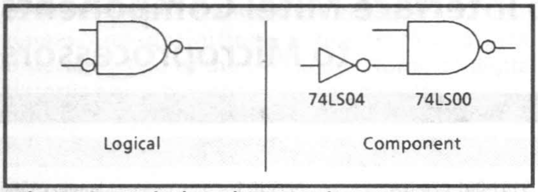


Figure 1 - Logical Implementation vs. Component Implementation

These microprocessors are believed to be the industry's most popular. In most cases, microprocessors not included in the list will have architectures similar to one of those mentioned.

To minimize the number of interfaces that have to be dealt with, it is possible to segment the listed microprocessors into groups. Members of a group are related by similar bus structures. The microprocessors that can be grouped together are:

a/ 68000, 68010, 68008
b/ 8088, 8086

The remaining microprocessors have subtle differences between each other that cause a need for individual interface circuits.

Grouping Mitel's components on the basis of similar interfacing requirements also minimizes the total number of interface circuits. Mitel devices with similar bus architectures are grouped as follows:

Group 1

a/ MD65SC51 Asynchronous Communications Interface Adapter (ACIA)
b/ MT8952 HDLC Controller
c/ MT8880 DTMF Transceiver

Group 2

a/ MT8980 Digital Switch
b/ MT8981 Digital Switch

Group 3

MT8920 ST-BUS Parallel Access Device (STPA)

The majority of the application note is dedicated to describing the interface circuits and explaining their operation. Each interface shall have an accompanying block diagram to enhance understanding of the circuit. To keep the interfaces independent of a particular system, as few actual "glue" components as possible will be shown in the diagrams. Instead of showing commercially available components, only the logical symbol representing the desired operation shall be shown. This will leave the actual implementation to the designer (see Figure 1).

Table 1 is a cross reference of interface circuit diagrams, referenced by microprocessor and Mitel Semiconductor part number. To find the appropriate interface circuit, select the column corresponding to the microprocessor being used, and select the row corresponding to the Mitel component being used. The figure number of the required circuit diagram(s) is indicated in the table element common to the row and the column.

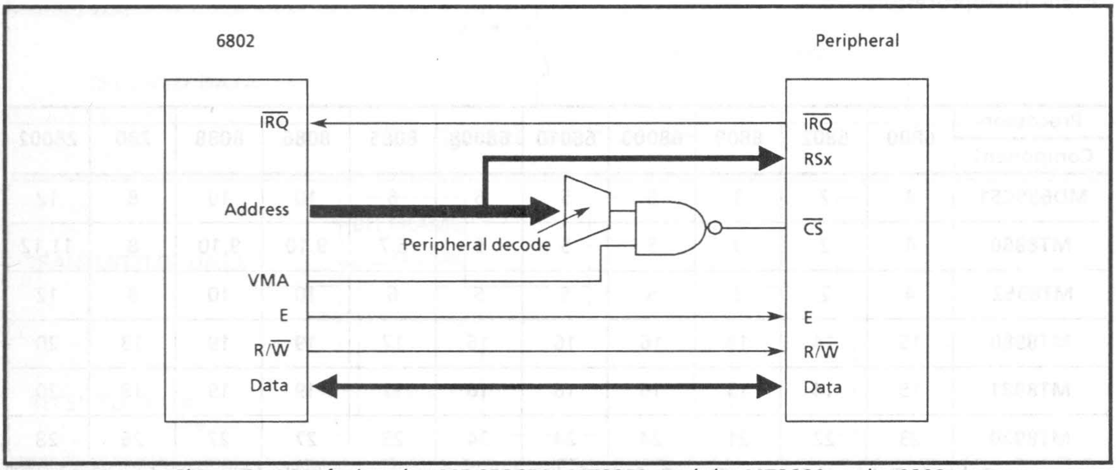


Figure 2 - Interfacing the MD65SC51, MT8952, and the MT8880 to the 6802

1.0 Group 1 Components

Group 1 consists of the MD65SC51, the MT8952 and the MT8880. All of these components have the same basic interface, but a subtle requirement causes several of the parts to use a separate and more complex circuit design (depending on the microprocessor interfaced to).

The Group 1 interface consists of:

a/ an 8 bit data port,

b/ several inputs used for selecting internal registers (register selects),

c/ chip select input(s) ,

d/ a read/write control that specifies the direction of data flow (to or from the component),

e/ an enable strobe that synchronizes component timing to the microprocessor's timing,

f/ an interrupt output that is used to alert the microprocessor that a specific event has occurred at the component.

The subtle difference mentioned above divides Group 1 components into two sub-groups: those components that require a constantly active Enable clock and those components that do not. The MT8880 is the component that requires a constant clock on the E input (in some of their operating modes). This may cause a more complicated circuit design when interfacing to microprocessors that have more than one clock cycle per bus cycle, i.e., 8085, 8086, 8088, Z80 and the Z8000. When interfacing to the 6802/09, 6800, and the 68000, the circuit design is the same for both sub-groups.

1.1 Interfacing to the 6802

Interfacing Group 1 components to the 6802 is the simplest interfacing task. The 6802 has the following interface:

a/ an 8 bit data port,

b/ 16 bit address bus for addressing 64 kbytes of memory or I/O,

c/ a read/write output that specifies the direction of data flow (to or from the microprocessor),

d/ an enable strobe output that synchronizes component timing to microprocessor timing, (This signal strobes with a constant frequency unless the microprocessor is in the reset condition. Cycles may be stretched, but should only be stretched for several normal E cycles. Note that, because E is constant, all group 1 devices may use the same circuit when interfacing to the 6802. Also note that one bus cycle is equivalent to one E cycle.)

e/ an interrupt input that is used to alert the microprocessor that a specific event has occurred at the component.

The 6802's signals relate to Group 1 signals almost directly. The data port of the 6802 may be connected directly to the data port of any of the Group 1 components. Information is transferred between microprocessor and the component on this bus. The address bus of the microprocessor must be decoded to produce the chip select(s) needed by a component before it will participate actively on the data bus. In a decode of the address bus, the validity of the address bus state-must be qualified by the VMA (Valid Memory Address) signal. Any of the address bits may be connected directly to the register select inputs of the component (the least significant bits are the bits most commonly used).

When the chip select is active, and the enable signal is active, the data bus will be carrying either information from the microprocessor, or information from the component. The source of the information is dependent on the state of the R/$\overline{W}$ signal from the 6802. If the R/$\overline{W}$ is high (read), the selected Group 1 component will turn on its data bus drivers and the contents of the selected register will be transferred to the data bus. If the R/$\overline{W}$ signal is low (write), the Group 1 device's data port will be high impedance and the microprocessor will transfer information to the data bus. The bus cycle is terminated by the falling edge of the E clock (strobe is a more appropriate term). When a write bus cycle is ended, the Group 1 component will latch the state of the data bus into the selected register. When a read bus cycle is ended, the component holds the data bus in the same state for a short period of time (hold time) before relinquishing control of the bus. Note that some of the components "acquire" the data from the bus on the rising edge of E. Appropriate set up time before this rising edge must be observed. Set up time is applicable to control signals, data and address information.

The interrupt output of Group 1 devices is an open drain configuration (analogous to open collector in TTL devices), therefore it must be pulled up to V_{CC} by a resistor. This output can be connected directly to the 6802 or to a priority encoder, which is then connected to the 6802. Group 1 components signify the presence of an interrupt condition by pulling this line low. The microprocessor must clear this interrupt through an established procedure that is dependent on the type of component that initiated the interrupt. The resistor used to pull up any open drain outputs is not shown any of the diagrams in this note.

Figure 2 shows the connection of data bus as a straight connection; in reality, there will probably be a buffer intervening to give the microprocessor more driving capability. R/$\overline{W}$ and E are also shown to be a straight connection. These signals are also usually buffered. In further figures, details such as buffers will be omitted as they are dependent on the design of the target system.

The address bits are shown connected to a box labelled "peripheral decode". This can refer to any circuitry that produces an active high signal when the correct address is on the bus. The active signal is 'NAND'ed with VMA to produce an active low chip select. Most Group 1 components have at least two chip select inputs, usually of opposite active logical states, so the active low signal in Figure 2 could have been a high signal, depending on the device

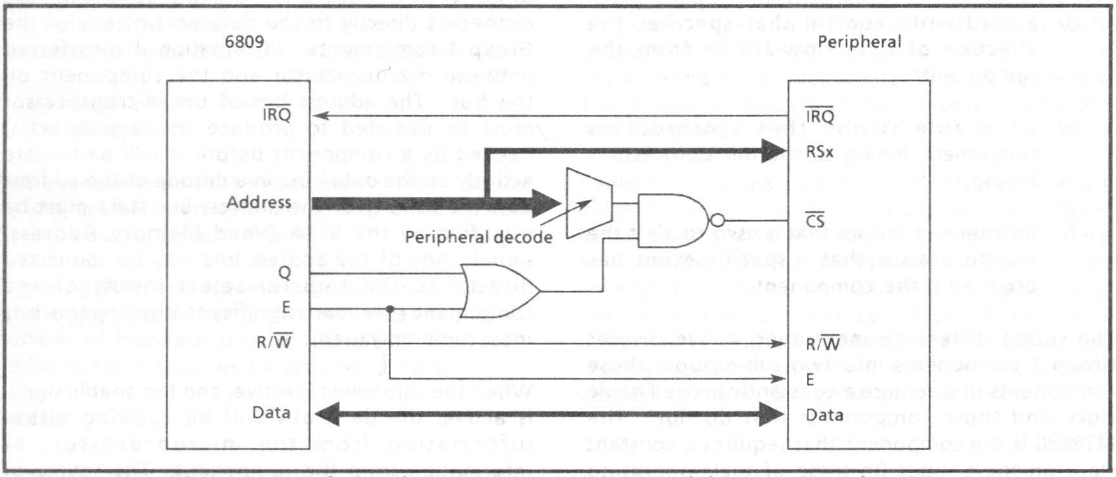


Figure 3 - Interfacing the MD65SC51, MT8952, and the MT8880 to the 6809

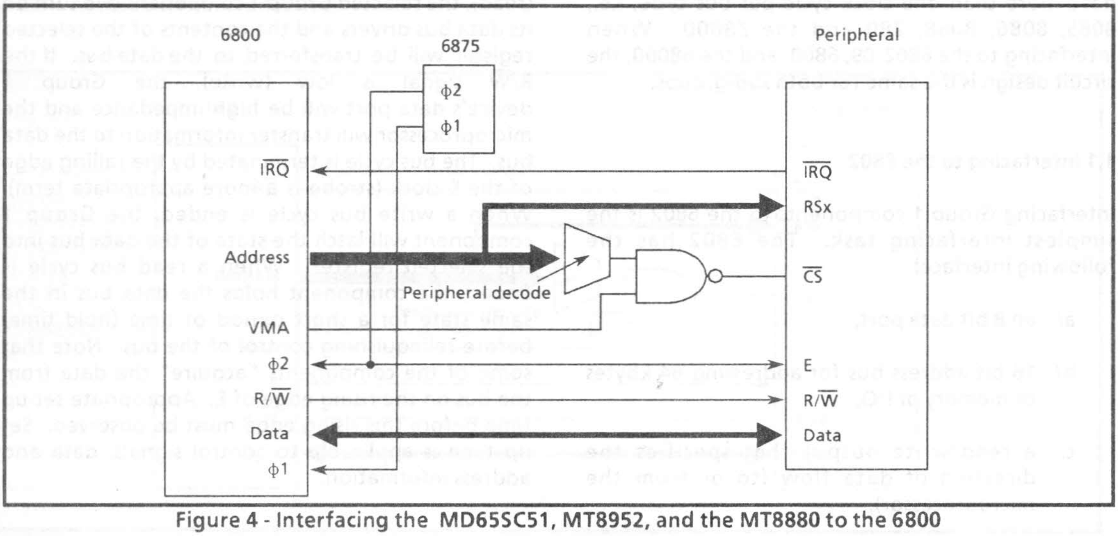


Figure 4 - Interfacing the MD65SC51, MT8952, and the MT8880 to the 6800

and the select used (remaining unused chip selects can be used to decode the address bus further, or may be tied to their active voltage levels). The most important point implied by the presence of the NAND gate is that the 6802's VMA signal must qualify any decode of Group 1 components (VMA could have been tied to the active high chip select input to save an external gate).

1.2 Interfacing to the 6809

The circuit needed to interface the 6809 to Group 1 devices (Figure 3) is almost the same as the circuit used to interface to the 6802, due to the similarity between the two microprocessors' bus architectures. The only difference between the two circuits is that the 6809 does not have a VMA signal, so an equivalent signal must be generated by 'OR'ing the E and the Q signals of the 6809.

1.3 Interfacing to the 6800

Interfacing the 6800 to Group 1 devices requires the same circuit used for interfacing Group 1 components to the 6802. The only difference between the circuits is that in Figure 4 the 6875 clock generator IC is shown connected to the 6800.

1.4 Interfacing to the 68000/10/08

Motorola's 68000 16 bit microprocessor takes advantage of the broad line of interfaces designed around its 8 bit microprocessors. Normally, information transferral between the 68000 and a peripheral is performed asynchronously, as opposed to the synchronous method used by the 8 bit microprocessors (6800, 6802, 6809, etc.). The 68000, however, can be forced to perform a synchronous transfer.

Synchronous transfers are achieved by referencing all bus events to the edges of the E strobe. Asynchronous transfers involve a handshake between the 68000 and the component involved in the data transfer. When the 68000 wants to read or write a device, the 68000 asserts $\overline{LDS}$ or $\overline{UDS}$ ($\overline{DS}$ in the 68008) and when the component has accepted the data (write) or has put valid data on the data bus (read), the component asserts an open drain signal called $\overline{DTACK}$ (Data Acknowledge). This signal causes the 68000 to end the bus cycle by removing the data strobe signal. Following DS negation, a read latches data into the microprocessor, the peripheral releases the data bus and negates $\overline{DTACK}$. If a write, the data is latched into the peripheral and it then negates $\overline{DTACK}$.

Motorola designed a mechanism to accommodate peripherals that do not have the capability to perform an asynchronous transfer with-the 68000. The 68000 supplies an E clock, a $\overline{VMA}$ signal and an input called $\overline{VPA}$. If an address supplied by the 68000 (qualified by $\overline{AS}$) causes the $\overline{VPA}$ signal to be asserted, the 68000 synchronizes the data transfer to the E clock (see 68000 data sheet for timing details).

To synchronize, the 68000 waits for the E clock to go low (E clock timing has no relation to normal 68000 bus cycles), then the 68000 asserts $\overline{VMA}$ and finishes out the bus cycle like an 8-bit microprocessor. The finishing sequence is as follows: E goes high, data is transferred, the bus cycle terminates with E falling, $\overline{VMA}$ is negated, $\overline{AS}$ and the data strobes are negated).

The 68000's exception handling is very different from the 8-bit processors. Peripherals can take an active role in the determination of the exception vector. Any state on the Interrupt Priority Level inputs (IPL0-2), other than all ones (level 0), indicates an interrupt. If an interrupt is indicated, the state of the $\overline{IPL0-2}$ inputs codes the level of the interrupt's priority. The information encoded on these inputs is inverted in the 68000 to represent the priority level on the 3 bit interrupt mask in the internal status register.

When the instruction that is being executed at the time of the interrupt is finished, the 68000 performs an interrupt acknowledge cycle. During an interrupt acknowledge cycle, the 20 most significant bits of the address are set high, the three least significant bits reflect the interrupt level, and the FC0-2 pins on the 68000 are all set (the real indicator that an interrupt acknowledge cycle is occurring). $\overline{AS}$ is asserted, and then $\overline{LDS}$ is asserted (an interrupt vector may only be transferred on the lower half-of the data bus in the 68000). The R/$\overline{W}$ pin will be high because the 68000 is expecting the peripheral to place vector information on the data bus, as if the 68000 was reading one of the peripheral's internal registers. A peripheral designed for the 68000 will complete the handshake with the data required and return $\overline{DTACK}$ just like a normal exchange.

Group 1 components do not have the above facility to provide the 68000 with an interrupt vector, just as they cannot perform an asynchronous transfer. However, Motorola has provided for 6800 peripherals in 68000 exception processing, just as provision was made for data transfers with 6800 peripherals. If the information that the 68000 provides to indicate an interrupt acknowledge cycle and the level of the interrupt can cause $\overline{VPA}$ to

be asserted, the 68000 will automatically fetch an exception vector at an address determined by the level of the interrupt (Motorola calls this autovectoring). There are seven autovector locations (7 interrupt priority levels) and they are located at address 000064_H to $00007C_H$.

The circuit to interface Group 1 components to the 68000 (Figure 5) must be able to assert $\overline{VPA}$ not only when the component is directly addressed, but also when the 68000 is indicating that the component was the source of the interrupt. Figure 5 shows a block symbol to represent the decode of a group 1 device. The input of this block is the address bus and $\overline{AS}$; the output is a signal that has two destinations: the in put to the circuit that asserts $\overline{VPA}$ and the input to the circuit that asserts the group 1 components chip select.

To select the component for data transfer, the output of the peripheral decode circuitry is further decoded by $\overline{VMA}$. To generate $\overline{VPA}$, the peripheral decode ouput is 'NOR'ed with an interrupt acknowledge (IACK) signal. The IACK signal is formed by 'AND'ing the FC0-2 outputs, asserting $\overline{AS}$, and placing the correct priority level information on the 3 least significant address pins. All this information is 'AND'ed to produce IACK. Figure 5 shows a possible interrupt encoding scheme implemented with the Group 1 component's $\overline{IRQ}$ line driving a 74LS348 eight to three encoder. The 74LS348, in turn, drives the $\overline{IPL}$ inputs (remember that the logic level is inverted to form the internal priority level).

The remaining signals that Group 1 components require are derived in a more standard manner. R/$\overline{W}$ from the 68000 can be connected directly to the component, as can E and one half of the 16 bit data bus (the component will be found at either odd or even addresses from the base address). The 68008 has only two interrupt inputs, with $\overline{IPL0}$/$\overline{IPL2}$ being functionally equivalent to tying $\overline{IPL0}$ and $\overline{IPL2}$ together on the 68000 (only priority levels 0, 2, 5 and 7 are available on the 68008).

1.5 Interfacing to the 8085

There are two circuits needed to interface group 1 components to the 8085, depending on the requirement for a continuous E clock on the MT8880. The circuit in Figure 6 assumes that the application can accommodate the lack of a continuous E clock; in some applications the MT8880 can do so.

The circuit is different from the interface to the Motorola 8 bit microprocessors in many respects. The first difference is that the Intel 8085 has a multiplexed address/data bus, the Motorola parts do not. The first step in decoding an address

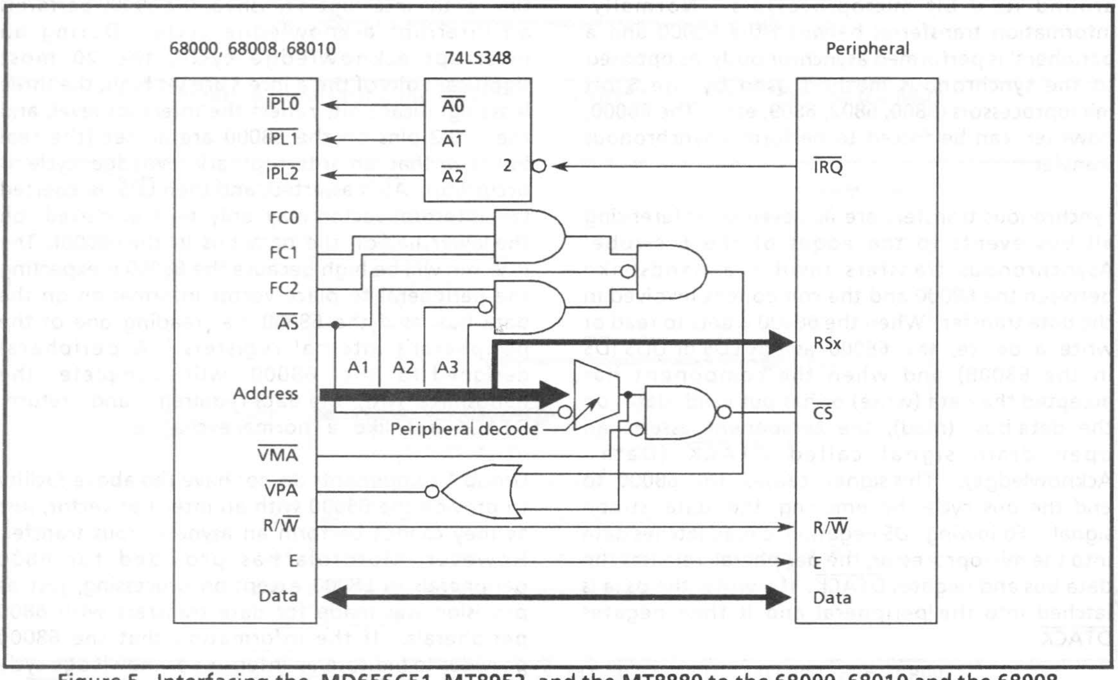


Figure 5 - Interfacing the MD65SC51, MT8952, and the MT8880 to the 68000, 68010 and the 68008

generated by the 8085 is to demultiplex the least significant half of the address from the data. Intel provides a latch, the 8212, that does this. It is strobed by the ALE (Address Latch Enable) signal from the 8085, when the address on the Address/data bus is valid. The demultiplexed address may then be decoded as in the Motorola system. The register select pins may be derived from any of the address bits.

The second difference is that rather then using the combination of a R/$\overline{W}$ direction pin and an E strobe, the 8085 uses a $\overline{Read}$ strobe and a $\overline{Write}$ strobe. When either of these strobes are active, the active period is equivalent to the period in a Motorola bus cycle where the E strobe is active. The direction of the data transfer is determined by which strobe, the $\overline{RD}$ or the $\overline{WR}$, is present. For correct operation of Group 1 components, R/$\overline{W}$ and E must be generated from $\overline{RD}$ and $\overline{WR}$. To generate E, $\overline{RD}$ and $\overline{WR}$ are 'NAND'ed together. The generation of the R/W signal is done by driving the Set input and the Reset input of a $\overline{RS}$ flip flop with $\overline{RD}$ and WR, respectively. The Q output may be connected directly to R/$\overline{W}$. R/$\overline{W}$ will maintain the same state until the opposite operation occurs, but it will only affect the Group 1 component when the device is selected, and then it will have the correct state with ample set up and hold times. It is important to note that R/$\overline{W}$ has a minimum set up time with respect to the rising edge of E. This must be accounted for in the circuit design, therefore E may have to be delayed.

The final difference in the 8085 circuit is that the interrupt input RST is active high, so the $\overline{IRQ}$ output of the Group 1 component must be inverted.

As stated before, the reason that a different interface is required for several Group 1 components in various applications is that these components require a regular E strobe. The MT8880 uses the E strobe to update the status of the $\overline{IRQ}$ pin and a bit in the status register that shows a valid DTMF (Dual Tone Multiple Frequency) tone has been received. These MT8880 signals will only become active if E is strobed during a period when a DTMF tone is actually present (the device retains no memory of such an event if it has already passed when E is strobed), so the period between E strobes should not be quite as long as the minimum time a DTMF tone must be present. The clock need not be present if no tones are expected.

Given that these devices have the above requirements, the circuit in Figure 6 must be modified to provide an E strobe with some regularity. The clock of the 8085 cannot be used directly because this clock has several cycles per bus cycle (four for opcode fetches, and three for data reads/writes to memory and I/O). It would be possible to keep using the signal derived by 'NAND'ing the $\overline{RD}$ and $\overline{WR}$ that is used in Figure 6, if it could be guaranteed that the microprocessor would not be placed in a hold state ($\overline{RD}$ and $\overline{WR}$ will cease to toggle until the microprocessor is released). If this cannot be guaranteed, then the circuit in Figure 7 may be required.

The circuit in Figure 7 is only different from the circuit of Figure 6 in the way E is generated. To generate a constant E strobe, the circuit takes advantage of the fact that ALE and the system clock (CLK) never get placed into a high impedance state (even in hold conditions). Also, events involving the $\overline{RD}$ strobe, $\overline{WR}$ strobe, ALE and CLK have a constant relationship that allows ALE to initiate an "event sequence" that is sustained by CLK and results in an E strobe synchronized with the termination of the $\overline{WR}$ and $\overline{RD}$ strobes (See Timing Diagram 1).

ALE occurs a minimum of 15 nS before the falling edge of clock cycle 1 in any 8085 bus cycle. The next falling edge of clock cycle 1 will clock the output of the first flip flop through the second flip flop to drive the E input of the group 1 component. This output is input into a third flip flop that is clocked by the rising edge of CLK, so on the rising edge of the clock cycle 2 the output of the third flip flop will be clocked low. This output drives the D input of a fourth flip flop, which will propagate this signal on the next rising edge of CLK (clock cycle 3). A low on the fourth flip flop's output will clear the first two flip flops and coincidently clear the signal driving the E input of the Group 1 component. This is also the point where data may be removed from the bus by the component if a read is occurring and where data is still valid from the microprocessor if a write is occurring, so the proper relationship between the microprocessor and the Group 1 component is maintained. Flip flops 3 and 4 are preset by ALE going high, so all flip flops are initialized for the next bus cycle.

1.6 Interfacing to the Z80

The circuit in Figure 8 is very similar to the circuit in Figure 6 in that the Z80 must transform a $\overline{RD}$ strobe and a $\overline{WR}$ strobe into an E strobe and a R/$\overline{W}$ signal (recall the set up time for the R/$\overline{W}$ signal with respect to the E signal). This portion of the circuit is exactly the same as the circuit used for the 8085, i.e., 'NAND'ing $\overline{RD}$ and $\overline{WR}$ to form E and the RS flip flop-used to create R/$\overline{W}$. In the Z80 circuit the peripheral decode has been arbitrarily chosen to include $\overline{IORQ}$ (I/O request) active. By doing this, the 8 most significant address bits need

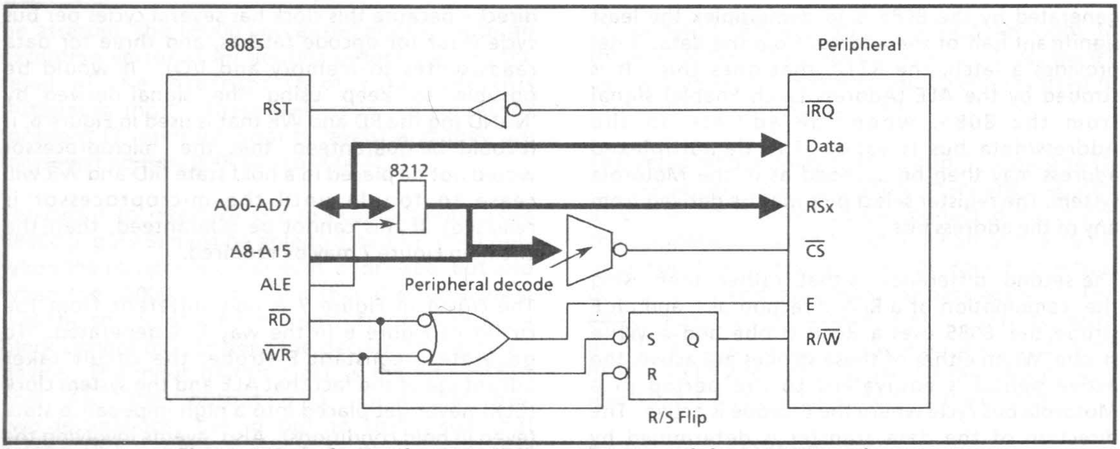


Figure 6. Interfacing the MD65SC51, MT8952, and the MT8880 to the 8085

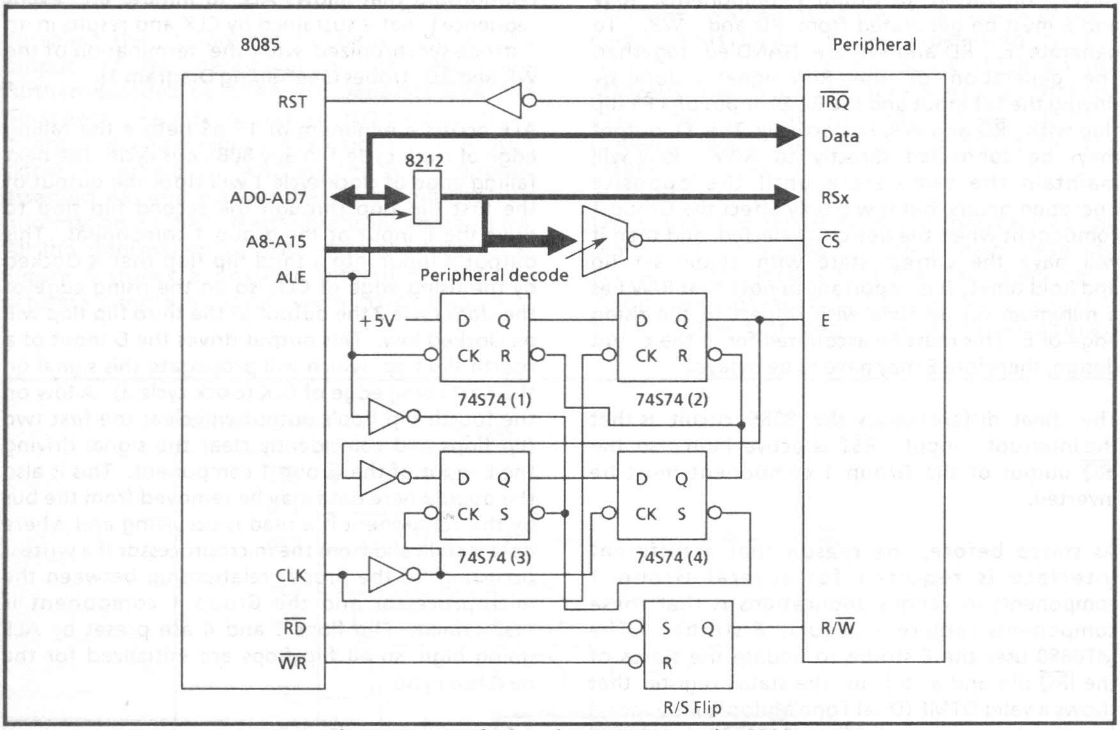


Figure 7 - Interfacing the MT8880 to the 8085

not be decoded, as an I/O access doesn't allow specification of more than an 8-bit address. Another difference between this circuit and the 8085 circuit is that the address bus of the Z80 is not multiplexed so no latch is needed for-a portion of the address. $\overline{\text{INT}}$, the interrupt input does not need an inverter between the Z80 and the Group 1 component. Both the 8085 and the Z80 have autovectored interrupts or vector acquisition modes (like the 68000). The autovectored interrupts should be used.

It is impossible to generate a regular E strobe, that is not based on the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals from the Z80. This is because the Z80 does not have a signal like ALE to unconditionally indicate the start of a bus cycle when $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are not present. This may make it difficult to use the MT8880 with the Z80, given the constraints on E mentioned earlier.

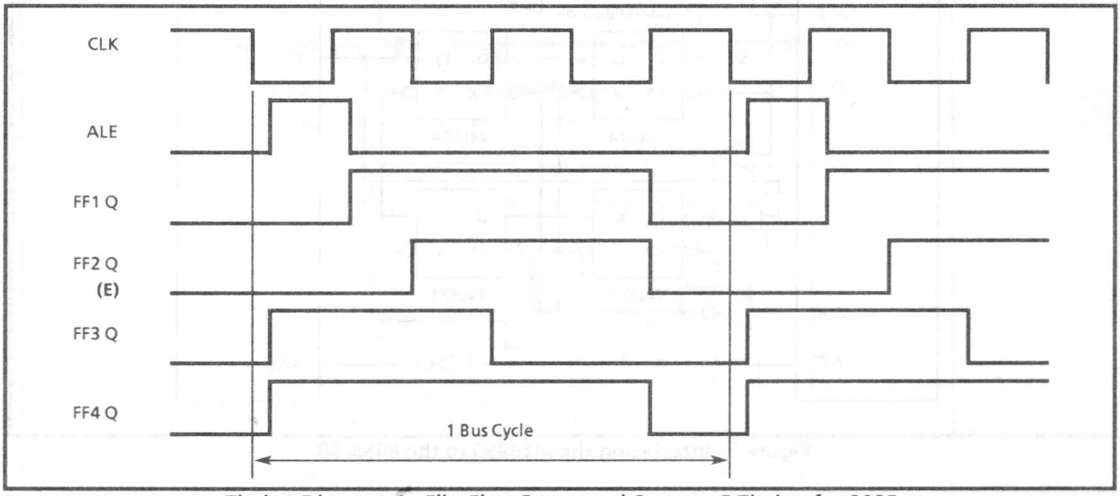
1.7 Interfacing to the 8086/88

The 8086/88 can interface to Group 1 components in a very similar manner to the way the 8085 does. The 8086/88 has a multiplexed address/data bus (AD0-15 for the 8086 and AD0-8 for the 8088), ALE strobes and $\overline{RD}$ and $\overline{WR}$ strobes. Conveniently, there is a signal that can be inverted and connected directly to the R/$\overline{W}$ inputs of Group 1 components, DT/$\overline{R}$ (Data Transmit/Receive).

$\overline{BHE}$ (Bus High Enable) is an output used to indicate that information is on the high portion of the data bus (8086 only). This signal is used to qualify chip selects. To generate the E signal in applications where E need not be constant, $\overline{RD}$ and $\overline{WR}$ may be 'NAND'ed together (Figure 10). The difference in the interrupt circuitry is that an 8259 Programmable Interrupt Controller may be used to handle the 8086/88's need for acquiring an interrupt vector (the 8086/88 does not provide autovectoring).

Note that although the 8086/88 has a minimum and maximum mode, the only difference in the signals required by Group 1 components is that when in maximum mode the signals may be generated by an 8288 bus controller rather than the 8086/88 itself. This is not shown in Figure 9 and Figure 10.

To generate the constant E strobe for the MT8880, a slightly altered 4 flip flop circuit that uses ALE and CLK as its inputs is shown in Figure 9. This circuit accommodates differences in the sequence of events between the 8086/88 and the 8085.



Timing Diagram 1 - Flip-Flop Generated Contant E Timing for 8085

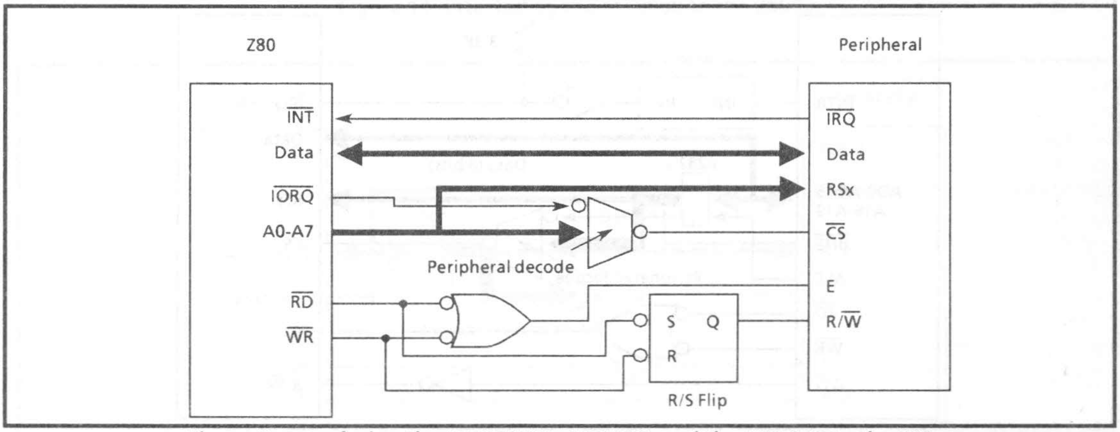


Figure 8 - Interfacing the MD65SC51, MT8952, and the MT8880 to the Z80

1.8 Interfacing to the Z8002

The circuits for interfacing the Z8002 to Group 1 components (Figures 11 and 12) are similar to the circuits for the 8086/88. The differences are:

a/ The Z8002 has an active low "autovector" input (the 8259 PIC is not needed).

b/ $\overline{AS}$, the Zilog version of ALE, is active low and must be used to strobe the multiplexed address bits from the Address/Data bus into a 16-bit latch.

c/ The Z8002 supplies a R/$\overline{W}$ signal.

d/ The Z8002 $\overline{DS}$ signal is the equivalent of the 8086/88 $\overline{RD}$ and $\overline{WR}$ strobes. This signal can be inverted to form E (Figure 12) for Group 1 components.

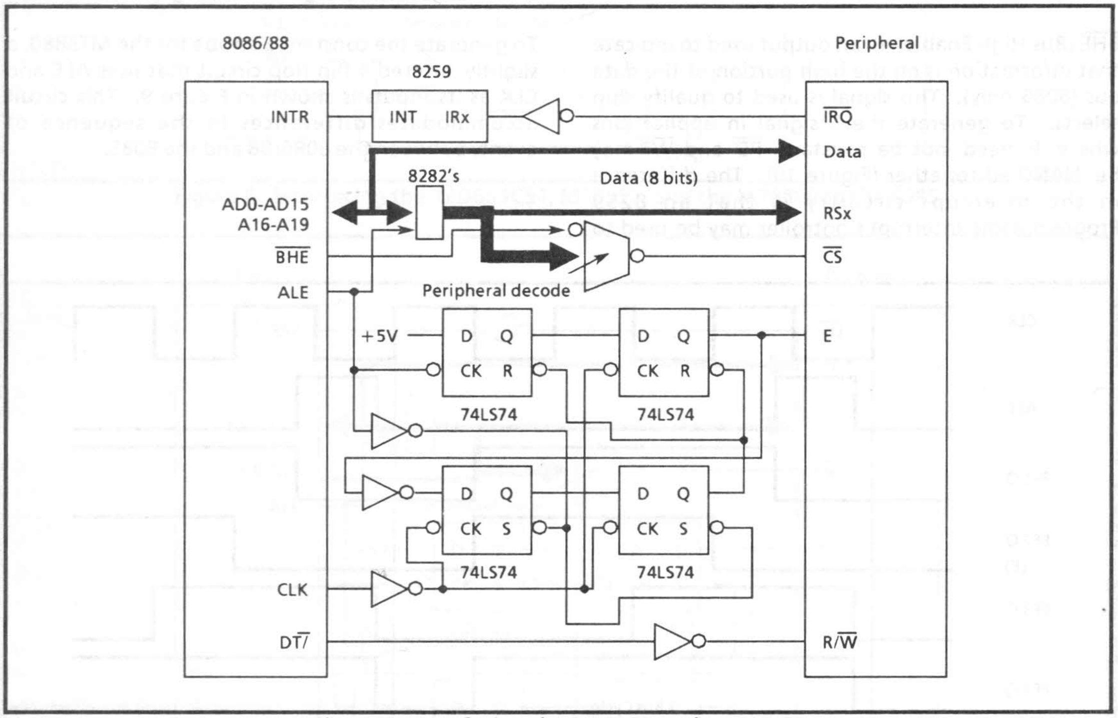


Figure 9 - Interfacing the MT8880 to the 8086/88

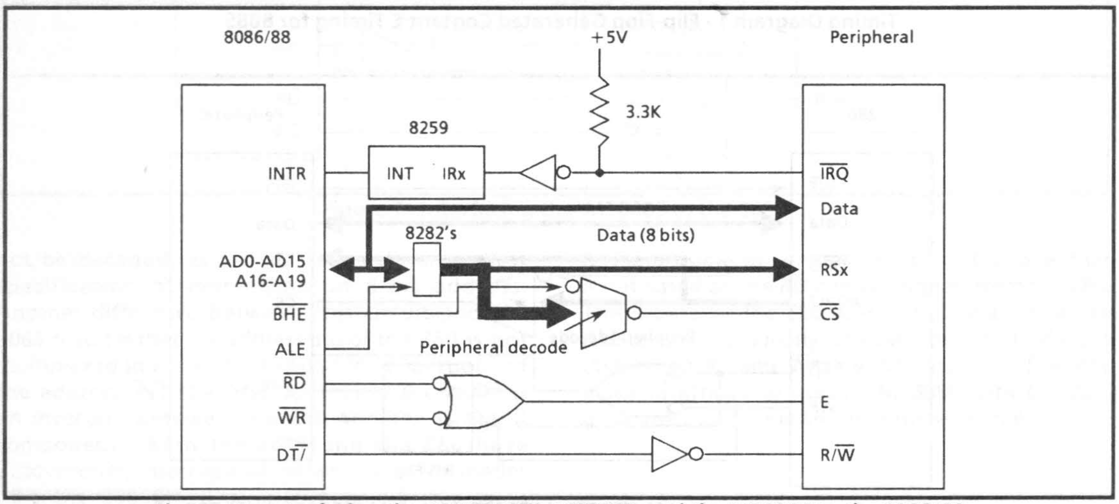


Figure 10 - Interfacing the MD65SC51, MT8952, and the MT8980 to the 8086/88

e/ Differences between the four flip flop circuit in Figure 11 and that in Figure 9 reflect the differences in event sequencing between the Z8002 and the 8088/86.

These two circuits complete the Group 1 components. Fortunately, the following two groups are not complicated by the need for a constant E clock.

2.0 Group 2 Components

The interface of a Group 2 component is different from that of a group 1 component in only two ways. The first difference is that there is no requirement for a Group 2 component to interrupt the microprocessor. This simplifies the circuit required by most of the microprocessors minimally, but for others (68000/10/08, 8086/88) the simplification is extensive. The other difference is that a Group 2 device may respond more slowly to microprocessor accesses. This suggests a

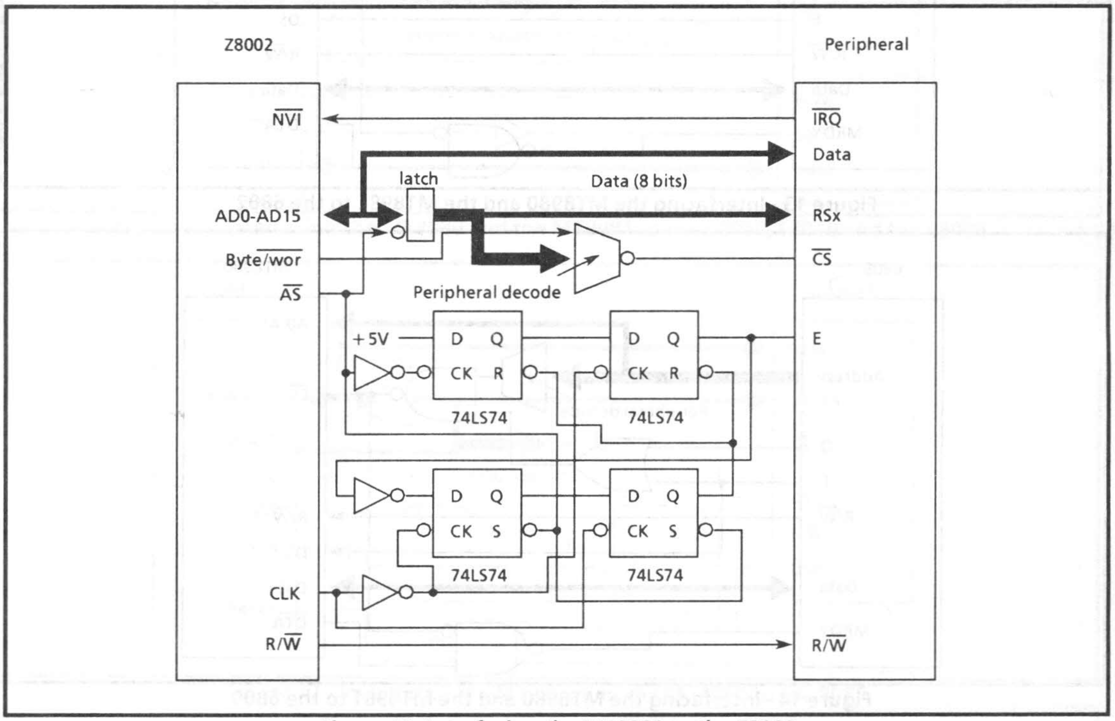


Figure 11- Interfacing the MT8880 to the Z8002

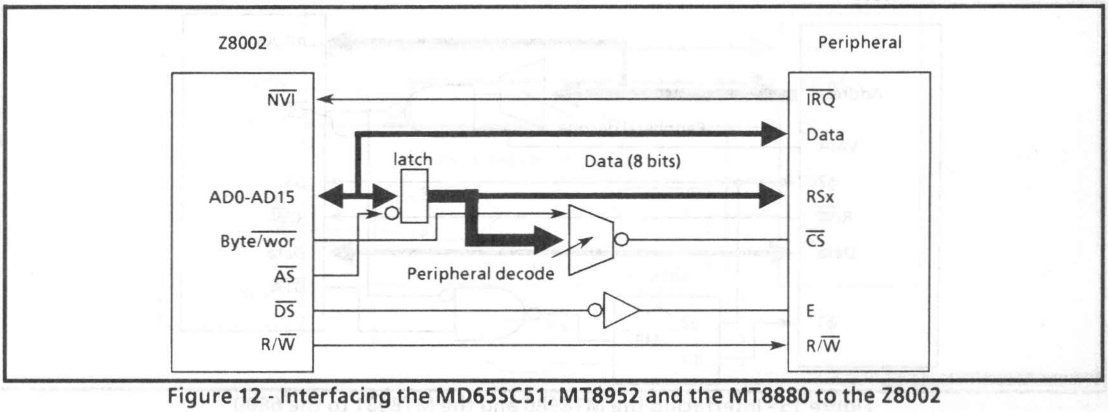


Figure 12 - Interfacing the MD65SC51, MT8952 and the MT8880 to the Z8002

requirement for a Memory Ready output from the Group 2 component.

Actually, Group 2 components have an output called $\overline{DTA}$ which can also serve as an input to $\overline{DTACK}$ on the 68000/10/08. In fact, DTA was designed for the 68000, so it needs extra circuitry to interface to the "memory ready" schemes of the synchronous microprocessors. This circuit consists of 'NAND'ing the signal that

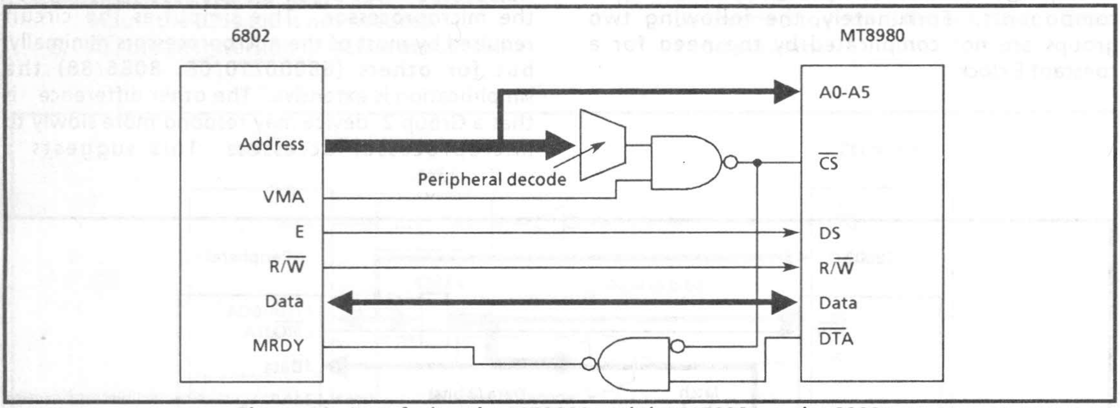


Figure 13 - Interfacing the MT8980 and the MT8981 to the 6802

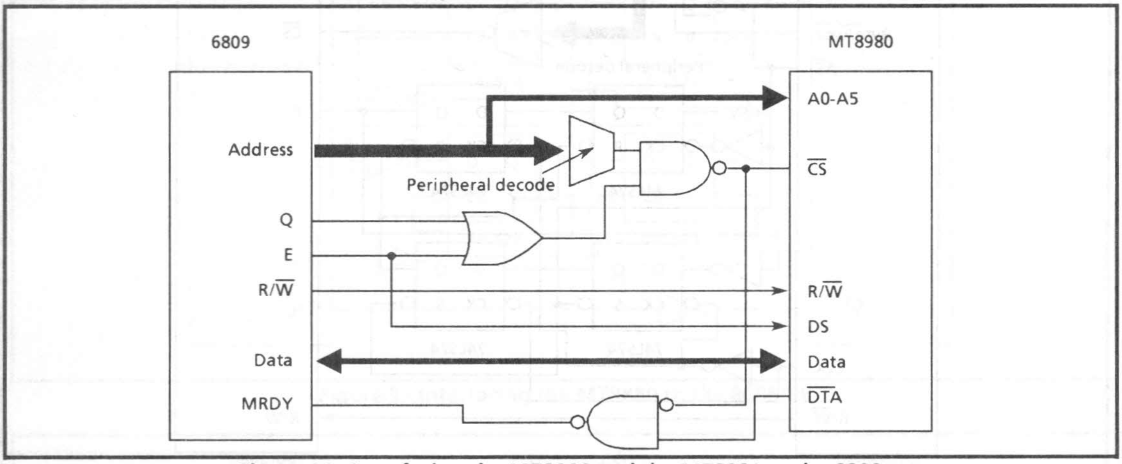


Figure 14 - Interfacing the MT8980 and the MT8981 to the 6809

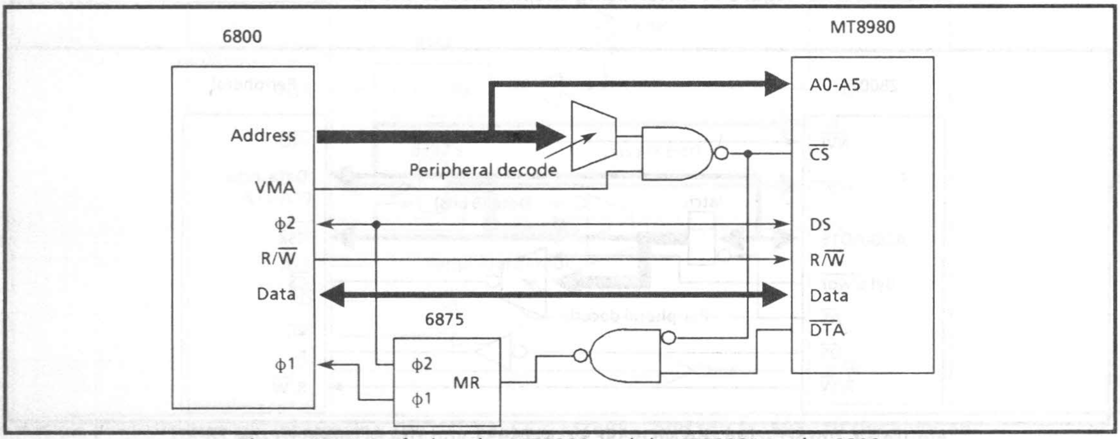


Figure 15 - Interfacing the MT8980 and the MT8981 to the 6800

selects the Group 2 component with the $\overline{DTA}$ signal.

Aside from the above circuit changes, each Group 2 interface circuit is the same as the Group 1 circuit, so a discussion on each circuit is not necessary. However, note that the 68000/10/08 circuit does not require the use of the E/$\overline{VMA}$/$\overline{VPA}$ interface (data strobe from the microprocessor must be inverted). Interfaces for Group 2 components are shown in Figures 13 to 20.

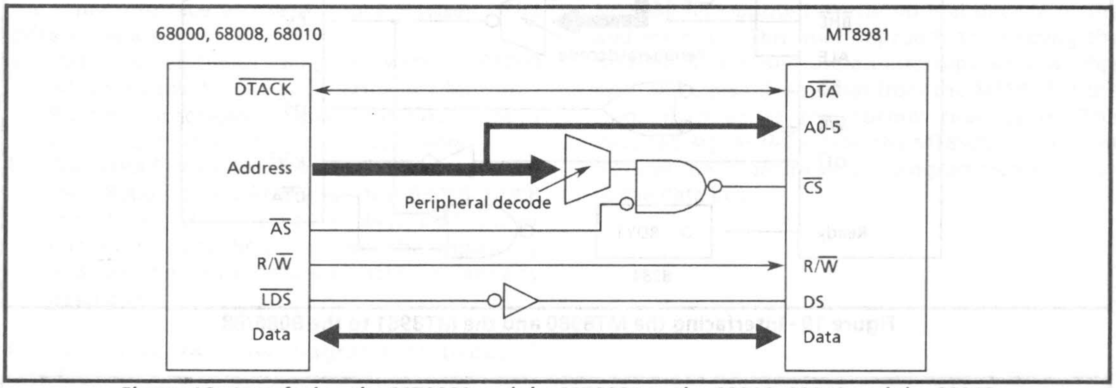


Figure 16 - Interfacing the MT8980 and the MT8981 to the 68000, 68010 and the 68008

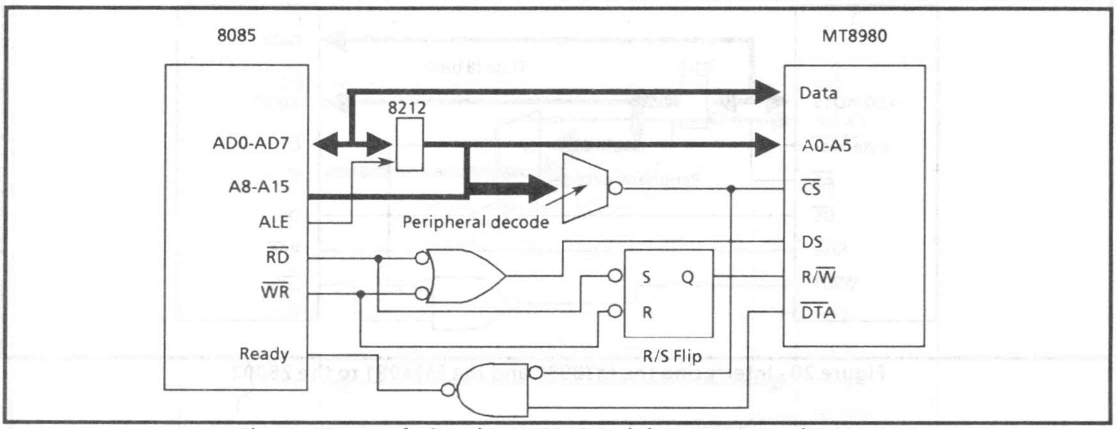


Figure 17 - Interfacing the MT8980 and the MT8981 to the 8085

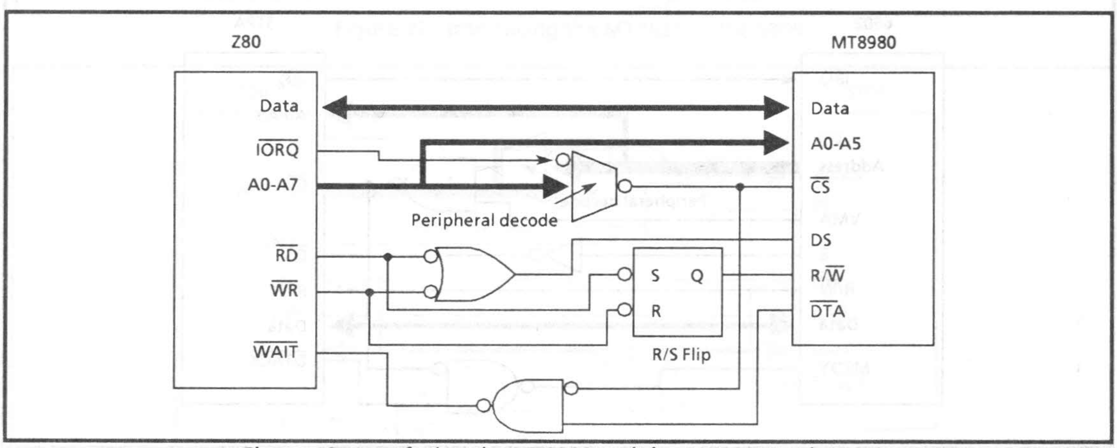


Figure 18 - Interfacing the MT8980 and the MT8981 to the Z80

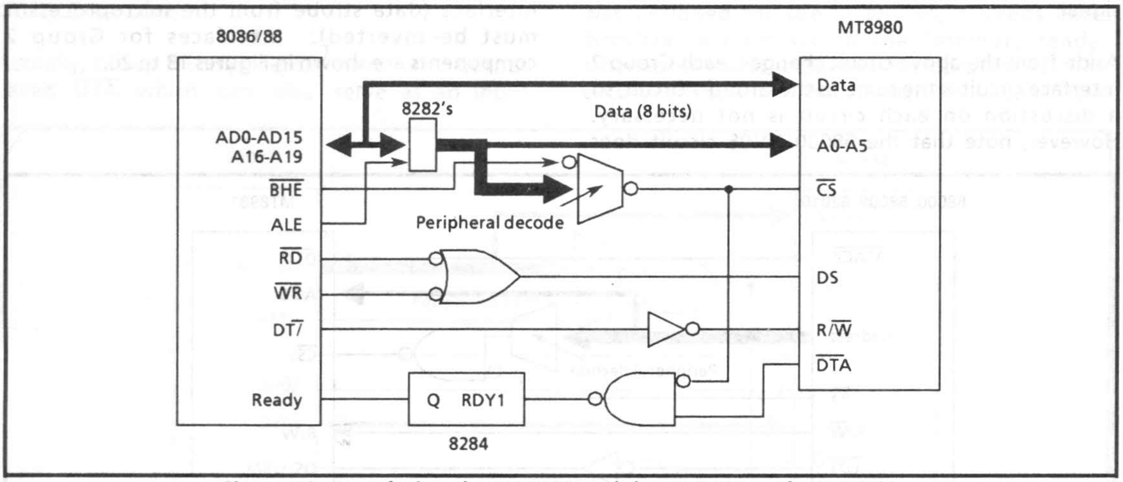


Figure 19 - Interfacing the MT8980 and the MT8981 to the 8086/88

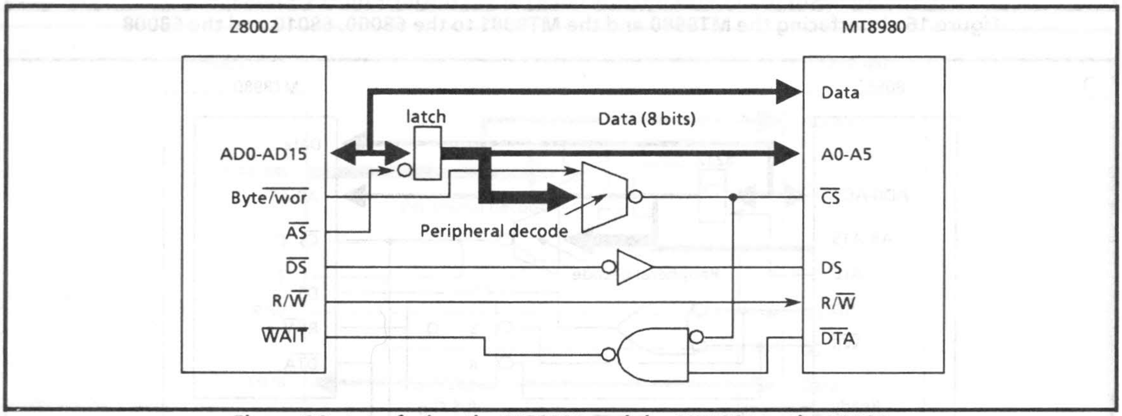


Figure 20 - Interfacing the MT8980 and the MT8981 to the Z8002

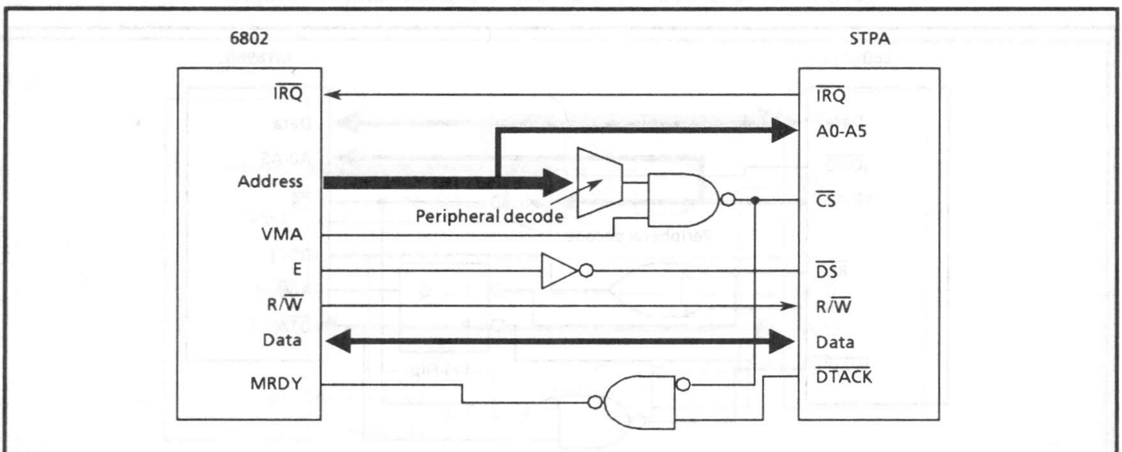


Figure 21 - Interfacing the MT8920 to the 6802

3.0 Group 3 Components

The Group 3 component is a device called the ST-BUS Parallel Access (STPA). The STPA has three operating modes, but only one mode was designed specifically for microprocessor control, so the others shall not be covered. The STPA has almost the same interface as the Group 1 devices. The differences are:

a/ Data strobe is the proper polarity for the 68000 which means it must be inverted for Motorola 8-bit microprocessors. Only slight modifications are performed for other microprocessors.

b/ The STPA can provide vectored interrupts for the 68000. This will change the 68000/10/08 interface circuit (Figure 24), but other microprocessors should ignore this capability and use the "autovectoring" schemes already described.

Figures 21 to 28 show diagrams of Group 3 interfaces.

3.1 Interfacing to the 68000/10/08

Figure 24 shows the circuit required to interface the MT8920 to the 68000. Note that $\overline{IACK}$ is decoded, but rather than being combined with the chip select signal to produce $\overline{VPA}$, $\overline{IACK}$ combines with the state of A1-3 to provide an alternative select to the MT8980 (as opposed to the normal decode of the address bus). This dual approach to selecting the MT8980 is used because an interrupt acknowledge cycle transfers information from the MT8920 in the same manner as any normal read cycle. The decoded signal $\overline{IACK}$ tells the MT8920 that it must transfer the interrupt vector programmed into it on to the data bus.

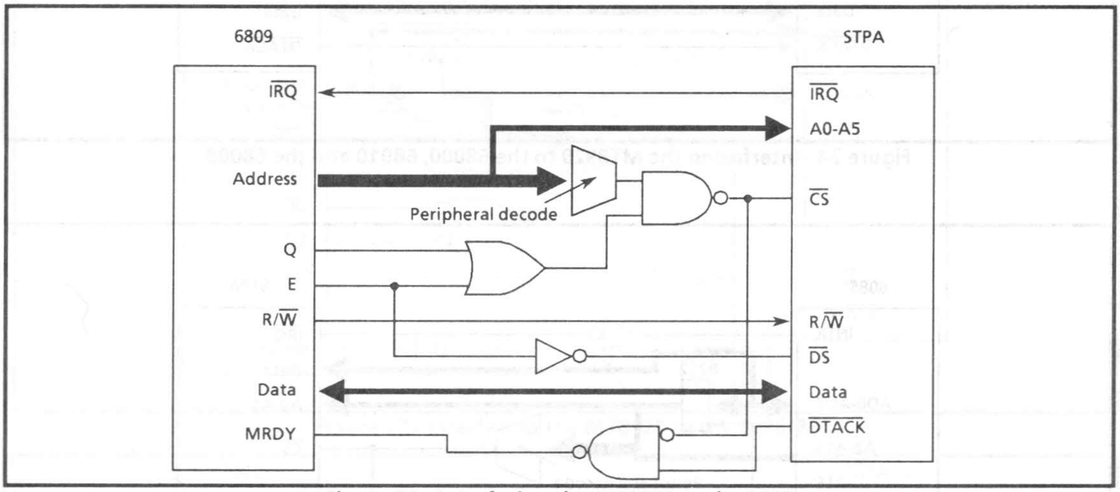


Figure 22 - Interfacing the MT8920 to the 6809

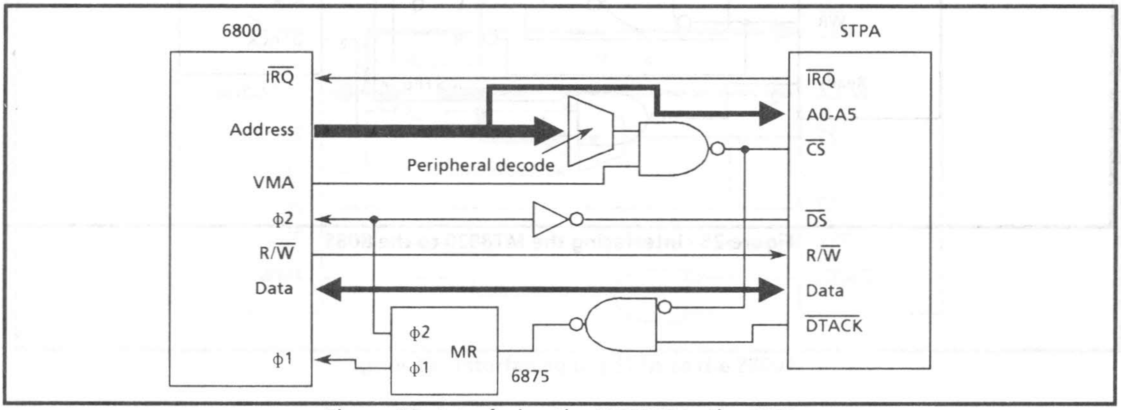


Figure 23 - Interfacing the MT8920 to the 6800

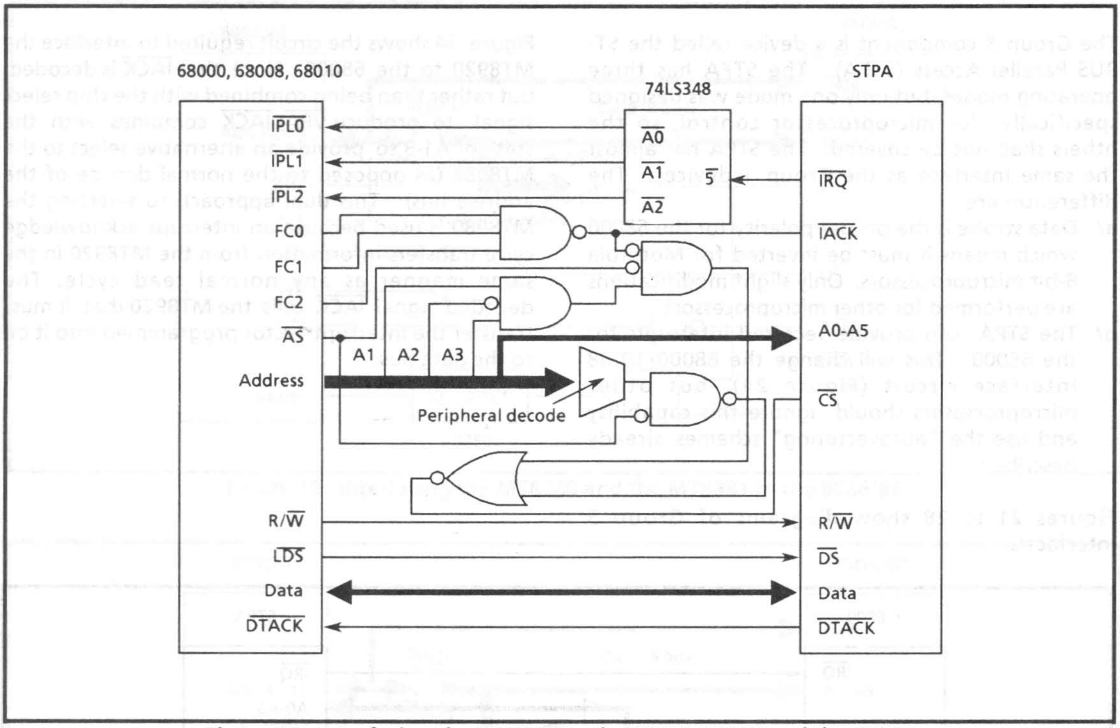


Figure 24 - Interfacing the MT8920 to the 68000, 68010 and the 68008

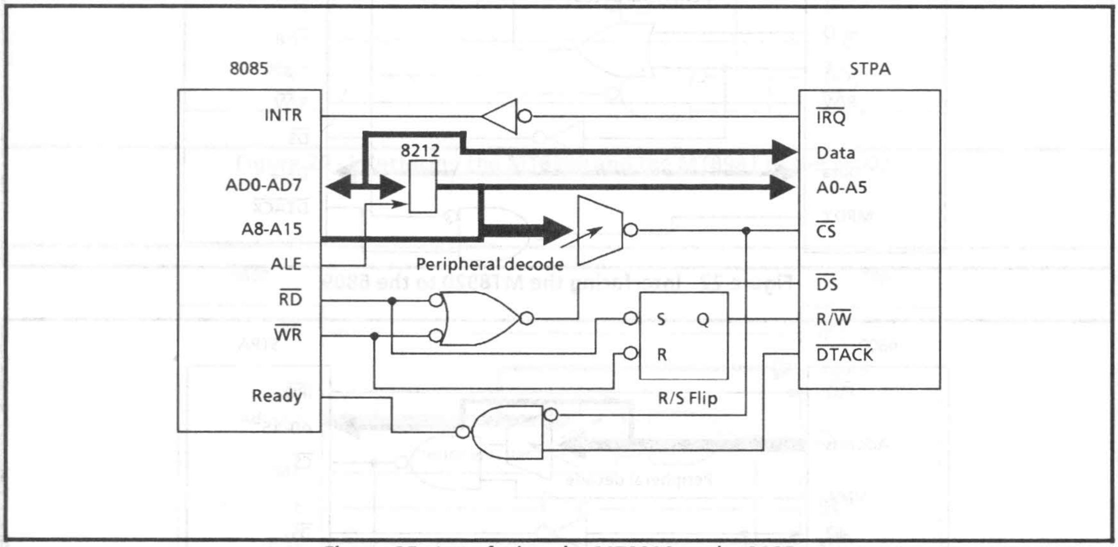


Figure 25 - Interfacing the MT8920 to the 8085

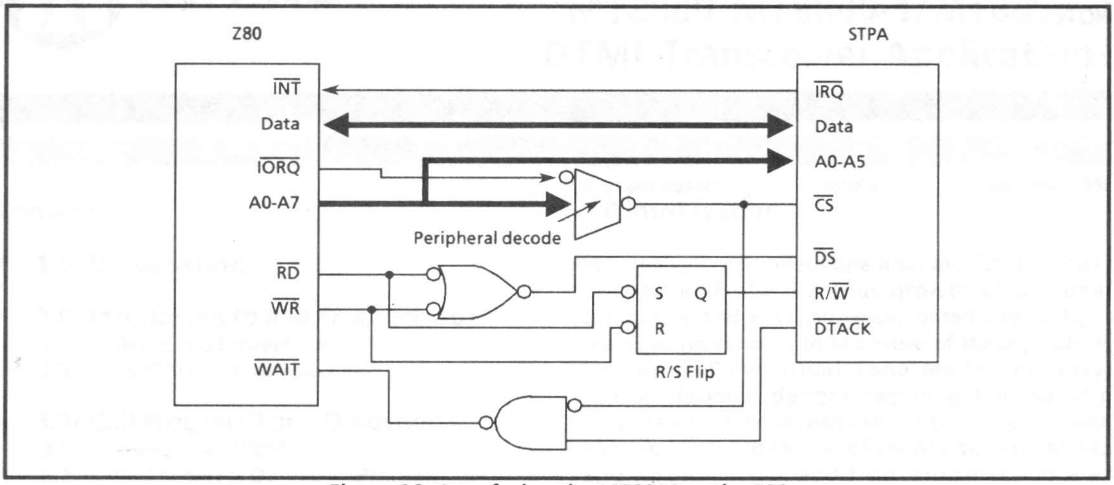


Figure 26 - Interfacing the MT8920 to the Z80

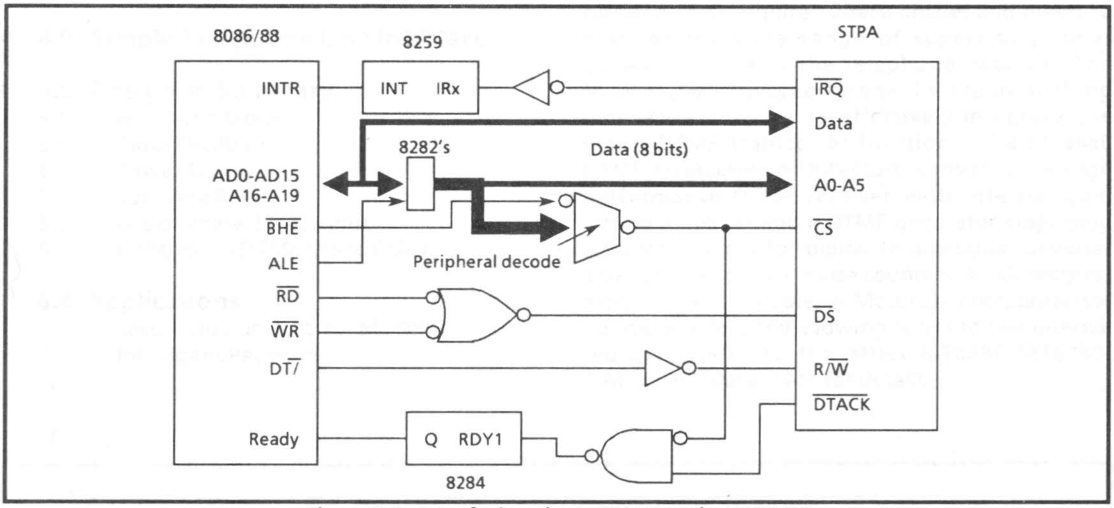


Figure 27 - Interfacing the MT8920 to the 8086/88

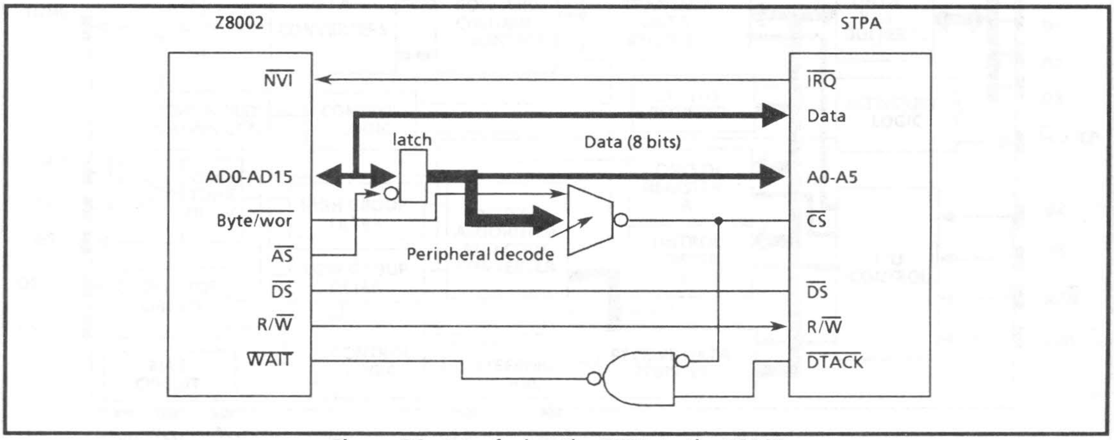


Figure 28 - Interfacing the STPA to the Z8002

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NOTES:

Applications Note **MSAN-120**

MT8880/MT8880-1/MT8880-2 DTMF Transceiver Applications

9161-001-003-NA ISSUE 3 September 1988

Contents

1.0 Introduction

With voice grade telephone lines available globally coupled with the vigorous growth of personal computers and microprocessor based products, it comes as no surprise to see more of these products employing DTMF (Dual Tone Multi-Frequency) devices. Product designs requiring the use of a DTMF transmitter, receiver and microprocessor have also required a collection of various buffers, latches and counters. In addition automatic dialer applications (mobile radio and alternate common carrier access) require filters, latches and timers to monitor the wide range of supervisory tones currently in use in the telephone network. The Mitel MT8880 saves costly board space by applying innovative circuitry to effectively integrate the entire DTMF transceiver function. The MT8880 DTMF transceiver architecture consists of a high performance DTMF receiver with internal gain setting amplifier and a DTMF generator employing a switched capacitor digital to analogue converter and automatic burst mode counters. A call progress mode is also available. A Motorola microprocessor interface is included allowing access to five internal registers. Refer to the Mitel MT8880/MT8880-1/MT8880-2 data sheet for details.

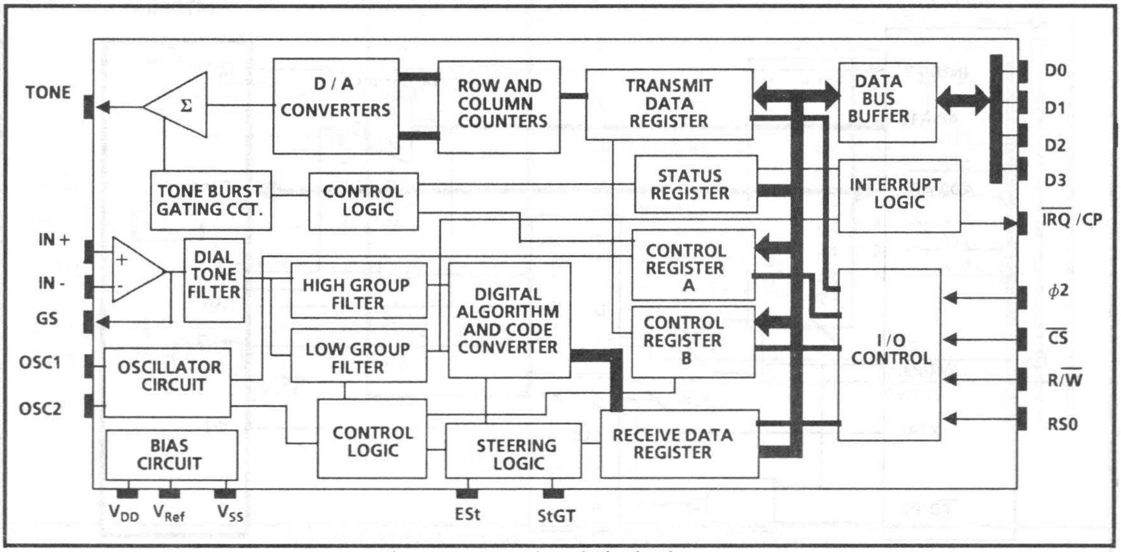


Figure 1. Functional Block Diagram

2.0 Interface to a Microprocessor

2.1 INTEL 8051 Interface

The Intel 8051 is a microcomputer which can provide a cost effective solution for many controller applications. Very compact systems including autodialers, secure access modems, credit card verification and telemetry systems can be implemented with the MT8880 and the 8051.The circuitry shown in Figure 2 shows how the MT8880 and 8051 can be interfaced. The application outlined here uses the internal program memory on the 8051 and accesses the MT8880 via external data memory. By using external data memory the RD and WR pins (alternate functions of P3.7 and P3.6) are activated which can be used to generate the required Phase 2 clock and R/W signals on the MT8880. When external data memory is not being accessed there will be no activity on the RD and WR outputs, however, the MT8880 requires a clock input on the Phase 2 pin at all times. Activity is necessary to update the internal registers and provide interrupt signals used in servicing the DTMF receiver or transmitter functions. If the MT8880 is not being accessed, the frequency of the Phase 2 signal may be reduced. The recommended maximum Phase 2 period (when the MT8880 is not selected) is 1 ms. Durations longer than this may result in failure to produce an interrupt at the correct time or failure in updating the Status Register. Suitable activity for the Phase 2 input can be obtained by writing or reading to external data memory with attention given to the maximum Phase 2 period mentioned above. If external program memory is being used, this allows the output PSEN to be used as a source of activity suitable for the MT8880 Phase 2 input. The circuit shown in Figure 4 could be modified to make Phase 2 a function of RD, WR and PSEN. When external program memory is not being used, the 8051 internal timer can be used as a baud rate generator set up in mode 0. This mode sets up a baud rate which is 1/12 the oscillator frequency. The output is transmitted through TXD.

During the period when the MT8880 is being accessed (external data memory) the circuit shown in Figure 4 will provide proper timing. The RD and WR signals are NANDed and fed to the Reset input on RS latch 1 (see Figure 2). The output of RS latch 1 is connected to the phase 2 input of the MT8880. A WR signal from the 8051 will set the output of latch 2 low inducing a Write condition at the MT8880 R/W input. Phase 2 will be asserted on the next rising edge of the system clock allowing suitable setup time. Following the Write operation (when the MT8880 is deselected), Phase 2 is reset to a logic low condition and the output of RS latch 2 (see Figure 2) will be set to a logic high which will induce a "read" condition. When accessing external memory the low byte of the address is time multiplexed with the data byte on port 0. However, in this application the low order address byte is not used and as such no demultiplexing circuitry is used. Note that EA

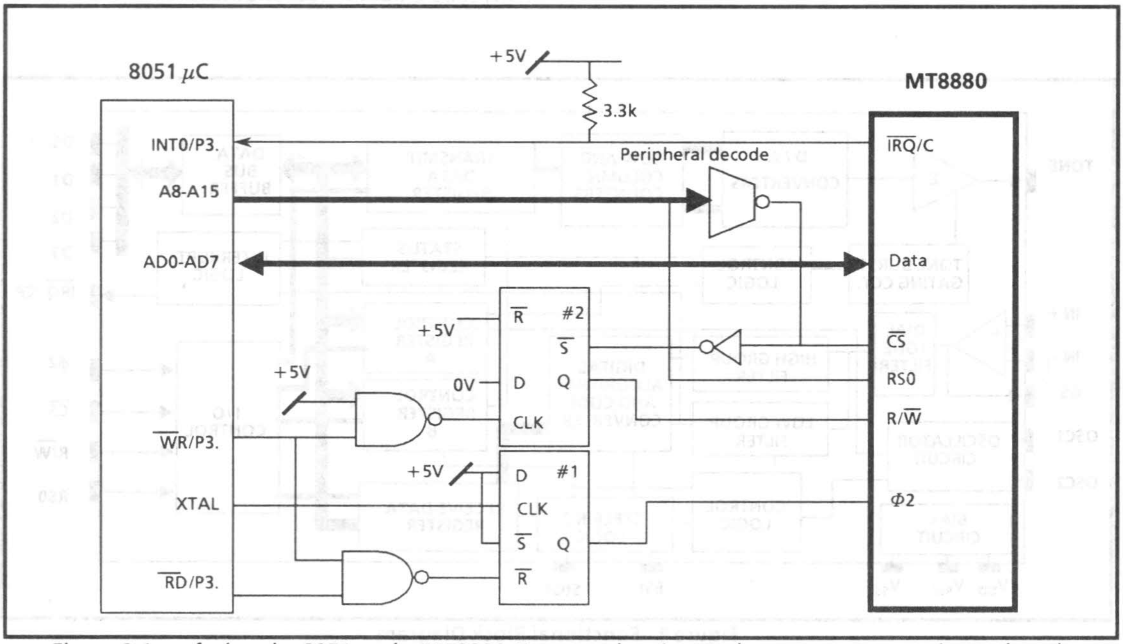


Figure 2. Interfacing the 8051 to the MT8880. For use when internal program memory is employed.

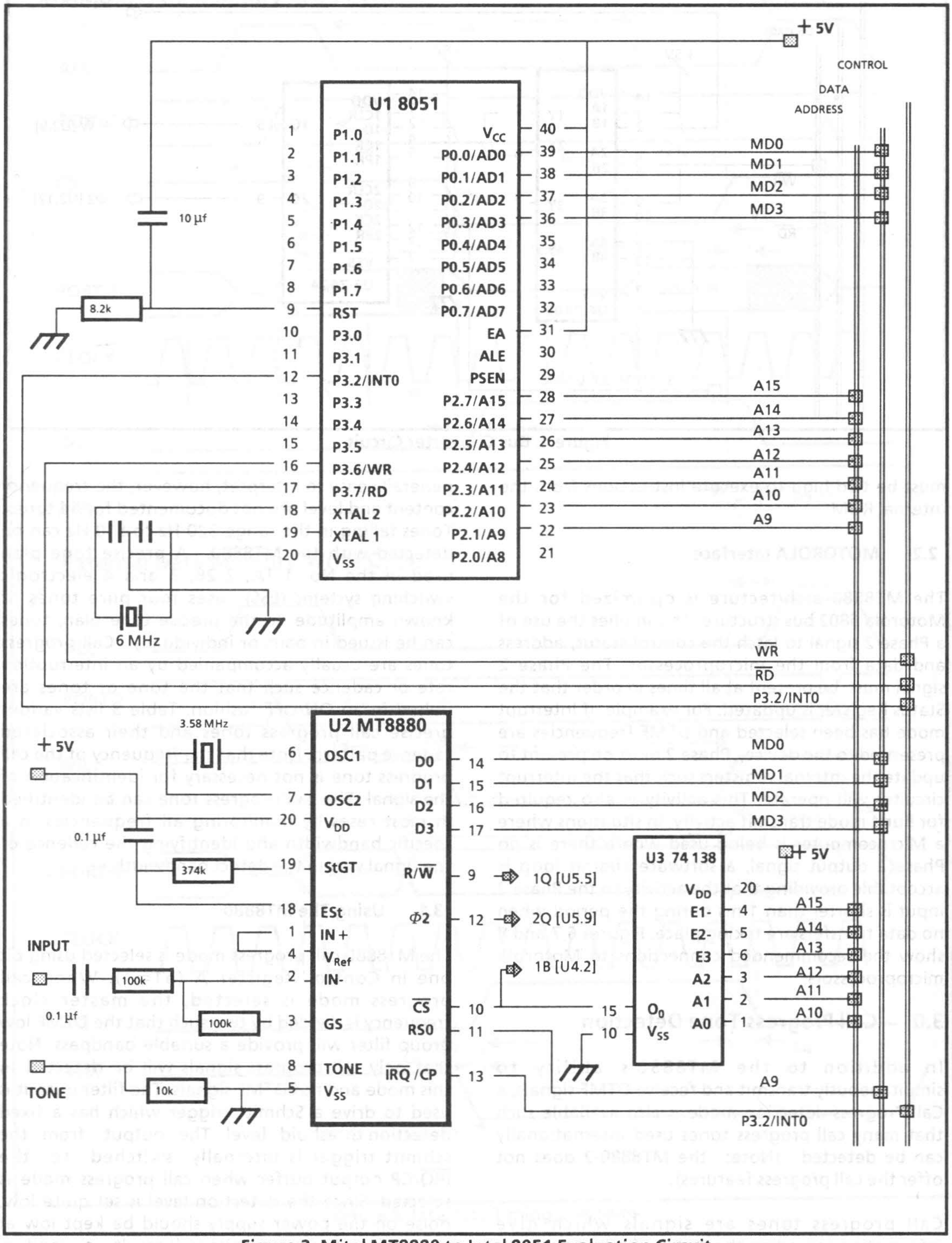


Figure 3. Mitel MT8880 to Intel 8051 Evaluation Circuit

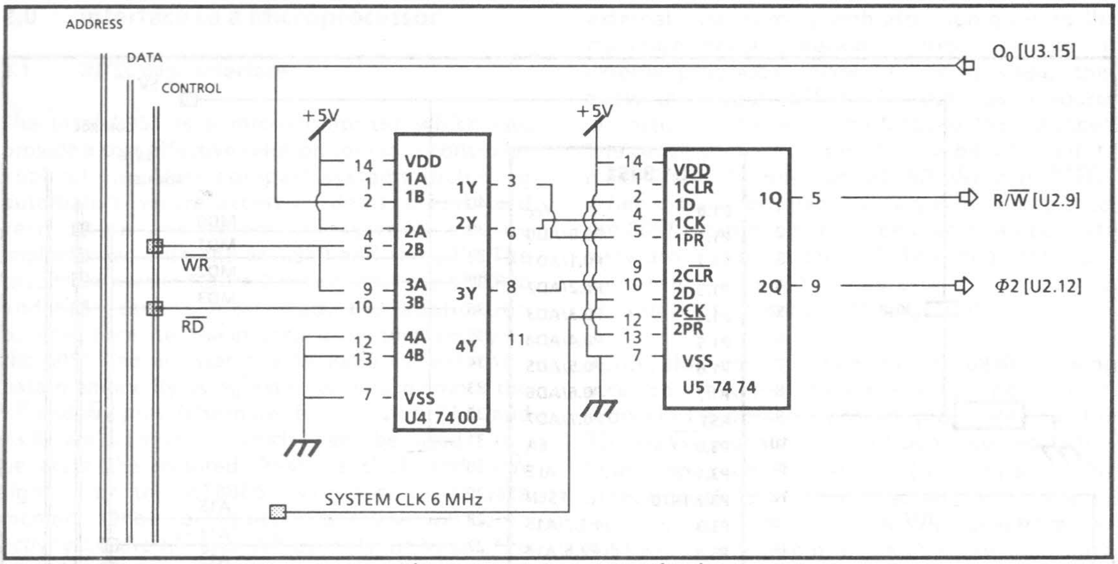


Figure 4. Bus Converter Circuit

must be tied high to execute instructions from the internal ROM.

2.2 MOTOROLA Interface

The MT8880 architecture is optimized for the Motorola 6802 bus structure. This implies the use of a Phase 2 signal to latch the control status, address and data from the microprocessor. The Phase 2 signal must be present at all times in order that the Status Register is updated. For example, if Interrupt mode has been selected and DTMF frequencies are presented to the device, Phase 2 must be present to update the internal registers such that the interrupt circuitry will operate. This activity is also required for Burst mode transmit activity. In situations where a Microcomputer is being used where there is no Phase 2 output signal, a software timing loop is acceptable providing that the activity to the Phase 2 input is shorter than 1 ms during the period when no data transfers are taking place. Figures 6,7 and 8 show the recommended connections to Motorola microprocessors.

3.0 Call Progress Tone Detection

In addition to the MT8880's ability to simultaneously transmit and receive DTMF signals, a Call Progress detection mode is also available such that many call progress tones used internationally can be detected. (Note: the MT8880-2 does not offer the call progress features).

Call progress tones are signals which give information regarding the status of telephone calls to operators and customers. These tones are generally easy to interpret, however, the frequency content and level are not documented for all tones. Tones falling in the range 320 Hz to 510 Hz can be detected with the MT8880. A precise tone plan used in the No. 1/1A, 2/2B, 3 and 4 electronic switching systems (ESS) uses four pure tones of known amplitude. In the precise tone plan, tones can be issued in pairs or individually. Call progress tones are usually accompanied by an interruption rate or cadence such that the tone or tones are pulsed in an ON/OFF fashion. Table 3 lists various precise call progress tones and their associated cadence pattern. Note that the frequency of the call progress tone is not necessary for identification of the signal. The call progress tone can be identified in most cases by monitoring all frequencies in a specific bandwidth and identifying the cadence of the signal within the detect bandwidth.

3.1 Using The MT8880

The MT8880 call progress mode is selected using bit one in Control Register A (b1 = 1). When call progress mode is selected, the master clock frequency is divided by two such that the DTMF low group filter will provide a suitable bandpass. Note that only call progress signals will be detected in this mode and not DTMF signals. The filter output is used to drive a Schmitt trigger which has a fixed detection threshold level. The output from the schmitt trigger is internally switched to the IRQ/CP output buffer when call progress mode is selected. Since the detection level is set quite low, noise on the power supply should be kept low at the device. Excessive noise will result in random activity on the IRQ/CP output. The output signal

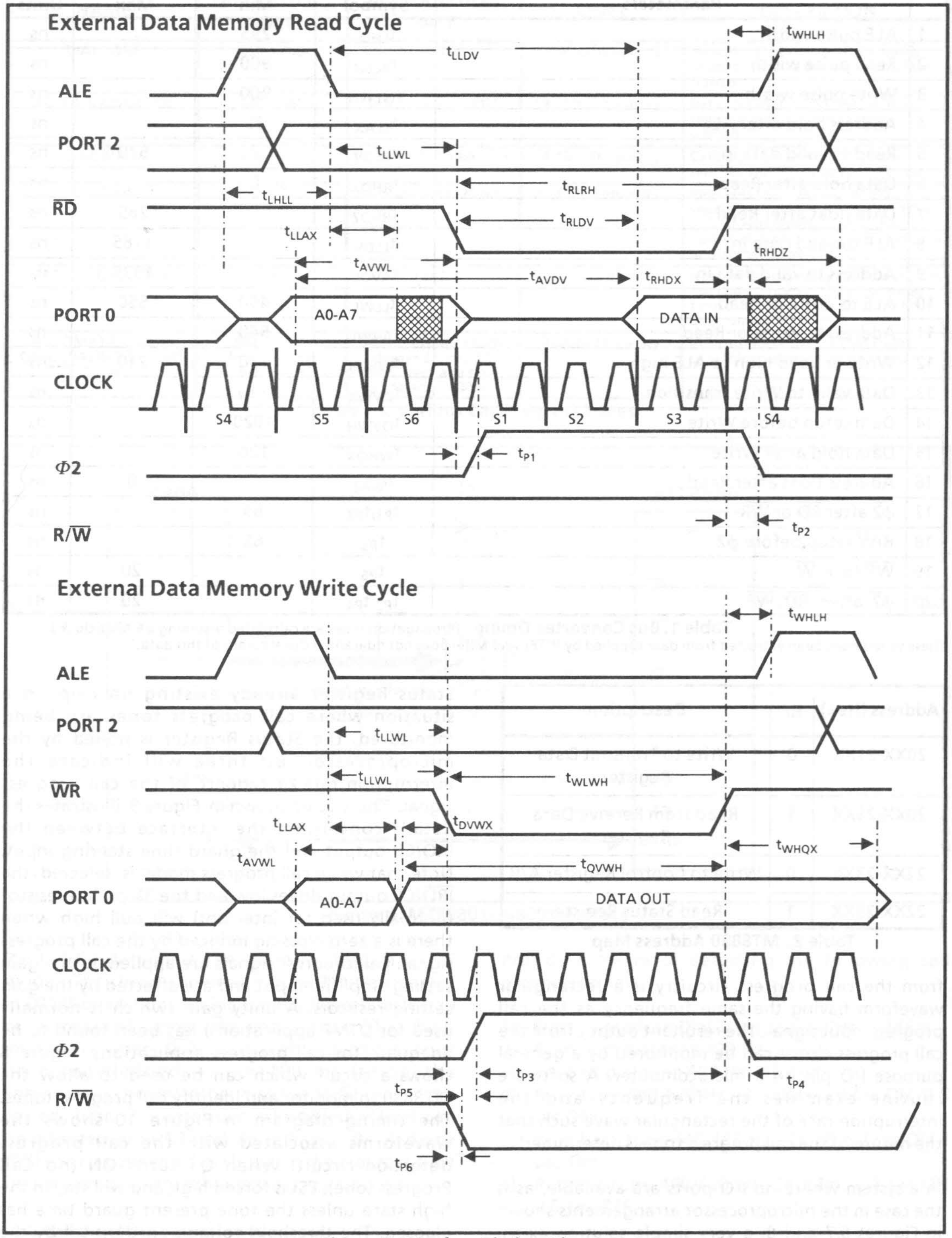


Figure 5. Interface Timing Diagrams

	Parameters	Symbol	Min	Max	Units
1	ALE pulse width	t_{LHLL}	295		ns
2	Read pulse width	t_{RLRH}	900		ns
3	Write pulse width	t_{WLWH}	900		ns
4	Address hold after ALE	t_{LLAX}	35		ns
5	Read to valid data in	t_{RLDV}		670	ns
6	Data hold after Read	t_{RHDX}	0		ns
7	Data float after Read	t_{RHDZ}		265	ns
8	ALE to valid data in	t_{LLDV}		1185	ns
9	Address to valid data in	t_{AVDV}		1335	ns
10	ALE to Write or Read	t_{LLWL}	450	550	ns
11	Address to Write or Read	t_{AVWL}	540		ns
12	Write or Read high to ALE high	t_{WHLH}	130	210	ns
13	Data valid to Write transition	t_{DVWX}	110		ns
14	Data setup before Write	t_{QVWH}	1020		ns
15	Data hold after Write	t_{WHQX}	120		ns
16	Address float after Read	t_{RLAZ}		0	ns
17	$\phi\overline{2}$ after $\overline{RD}$ or $\overline{WR}$	t_{P1},t_{P3}	85		ns
18	R/$\overline{W}$ setup before $\phi 2$	t_{P5}	65		ns
19	$\overline{WR}$ to R/$\overline{W}$	t_{P6}		20	ns
20	$\phi\overline{2}$ after $\overline{RD}$, $\overline{WR}$	t_{P2},t_{P4}		20	ns

Table 1. Bus Converter Timing (Propagation times are calculated assuming a **6 MHz** clock.)
These values have been extracted from data supplied by INTEL and Mitel does not guarantee the accuracy of this data.

Address (Hex)	R/	Description
20XX-21XX	0	Write to Transmit Data Register
20XX-21XX	1	Read from Receive Data Register
22XX-23XX	0	Write to Control Register A/B
22XX-23XX	1	Read Status Register

Table 2. MT8880 Address Map

from the call progress circuitry is a rectangular waveform having the same frequency as the call progress input signal. The resultant output from the call progress circuit can be monitored by a general purpose I/O pin on a microcomputer. A software routine examines the frequency and the interruption rate of the rectangular wave such that the nature of the call progress tone is determined.

In a system where no I/O ports are available, as is the case in the microprocessor arrangements shown in Figures 6,7 and 8, a very simple solution exists. The call progress output can be used to drive the steering circuitry (tone verification circuitry) normally used for DTMF which will update the Status Register already existing on chip. In a situation where call progress tones are being monitored, the Status Register is polled by the microprocessor. Bit three will indicate the interruption rate or cadence of the call progress signal. The circuit shown in Figure 9 illustrates the details concerning the interface between the $\overline{IRQ}$/CP output and the guard time steering input. Note that when call progress mode is selected, the $\overline{IRQ}$/CP output drives low and the 3k pullup resistor (normally used for interrupt) will pull high when there is a zero crossing induced by the call progress signal. Call progress signals are applied at the gain setting amplifier input and are affected by the gain setting resistors. A unity gain (which is normally used for DTMF applications) has been found to be adequate for call progress applications. Figure 8 shows a circuit which can be used to allow the MT8880 to monitor and identify call progress tones. The timing diagram in Figure 10 shows the waveforms associated with the call progress detection circuit. When Q1 turns ON (no Call Progress tone), ESt is forced high and will stay in the high state unless the tone present guard time has elapsed. The threshold voltage on U1 is set by the MT8880 V_{Ref} output. The tone present guard time is determined by the time constant formed by R3 and C2 plus the time constant determined by R5 and C3.

NAME	FREQUENCIES (Hz)	INTERRUPTION RATE	LEVEL	DESCRIPTION
DIAL TONE	350+440	STEADY	-13 dBm/frequency	Indicates that the receiving end is ready to receive dial pulse or DTMF signals.
AUDIBLE RINGBACK	440+480	2 sec. ON 4 sec. OFF	-19 dBm/frequency	Indicates that called line has been reached and that ringing has started.
LINE BUSY	480+620	0.5 sec. ON 0.5 sec. OFF	-24 dBm/frequency	Called customer's line has been reached but line is currently in use.
REORDER	480+ 620	0.25 sec. ON 0.25 sec. OFF	-24 dBm/frequency	Indicates that the local or toll switching transmission paths to the C.O. or equipment serving the customer are busy. May also indicate unassigned code.
PARTIAL DIAL TONE	480	STEADY	-17 dBm	Notifies calling party that dialing has not commenced in the preallotted time or that not enough digits have been dialed.
AUTOMATIC CREDIT CARD DIALING PROMPT TONE	941+1477 followed by 440+350	940 ms exponentially decayed from -10 dBm/freq. at a time constant=200ms	-10 dBm/frequency	Informs the customer that credit card information must be keyed in.

Table 3. Various Call Progress Tones

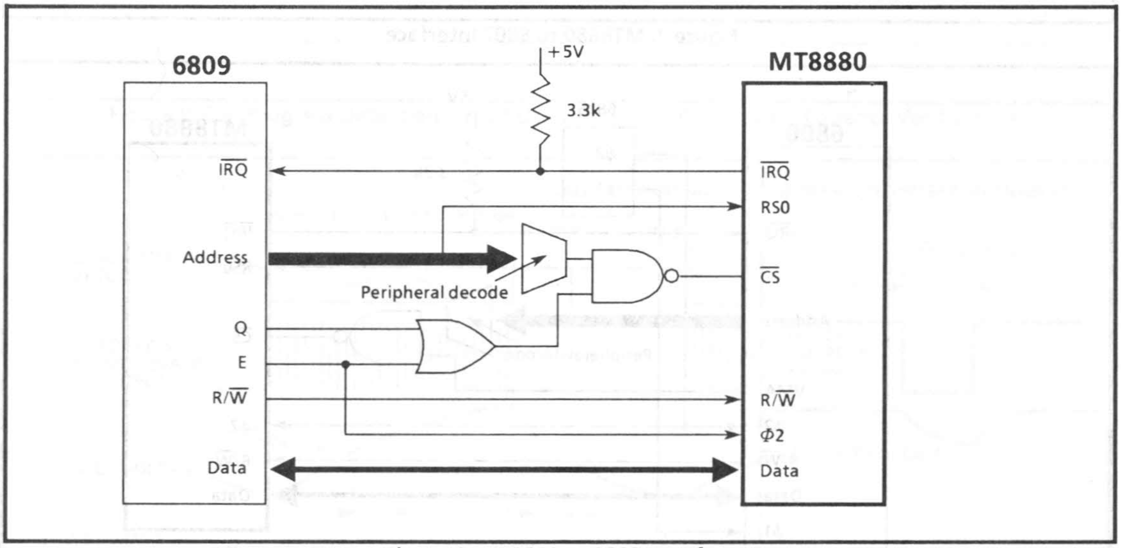


Figure 6. MT8880 to 6809 Interface

R3 and C2 determine the value for t_{GTA} in DTMF mode. The circuit shown in Figure 9 is transparent in DTMF operation. Timing is not adversely affected as a result of using the circuit since Q1 is high impedance when $\overline{IRQ}$/CP is high. Interrupts must be acknowledged within 100 ms (using the components shown) otherwise the St/GT pin will be forced high. The interrupt acknowledge time can be adjusted with C3 and R6 in Figure 9. A diode (D2) can be connected as shown in the diagram such that interrupts from other devices are ignored.

3.2 Call Progress Detection Program

The program shown in Appendix 1 was used in conjunction with the circuit shown in Figure 9 to provide a means of detecting the following call progress signals;

1) North American Dial Tone 350/440Hz, -13dBm.
2) European dial tone 425 Hz, -6 dBm.
3) Far East dial tone 400 Hz, -15 dBm.
4) Busy tone 480/620 Hz, -24 dBm, 0.5 sec ON 0.5 sec OFF.
5) Ring back tone 440/480 Hz, -24 dBm 2 sec ON 4 sec OFF.
6) Reorder tone 480/620 Hz -24 dBm, 0.2 sec ON 0.5 sec OFF.

Also, the detection scheme correctly ignored the 850 Hz European dial tone second harmonic at -44 dBm. The detection program makes use of two

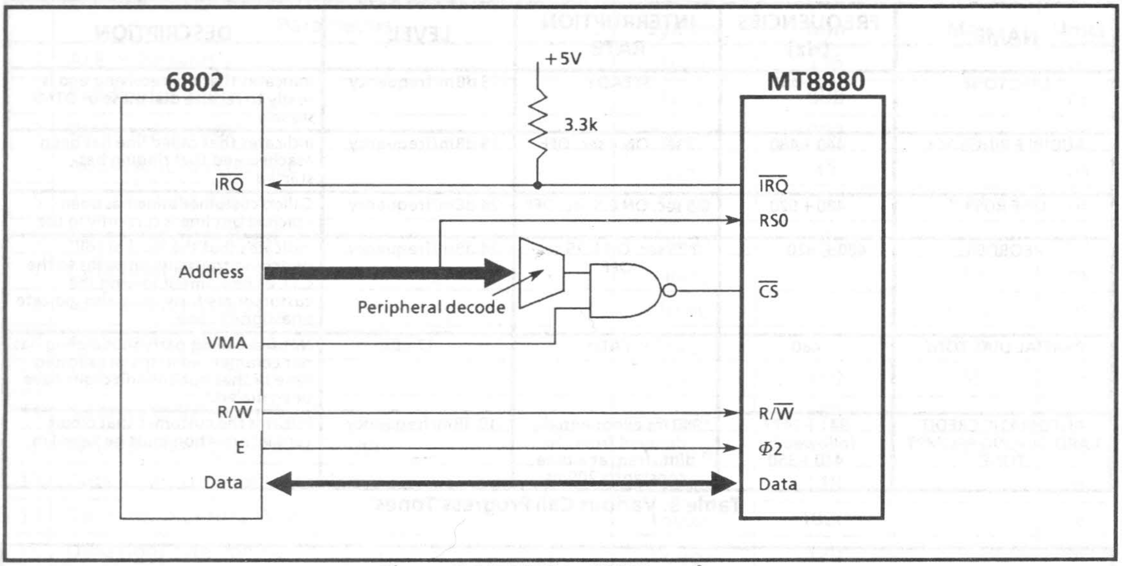


Figure 7. MT8880 to 6802 Interface

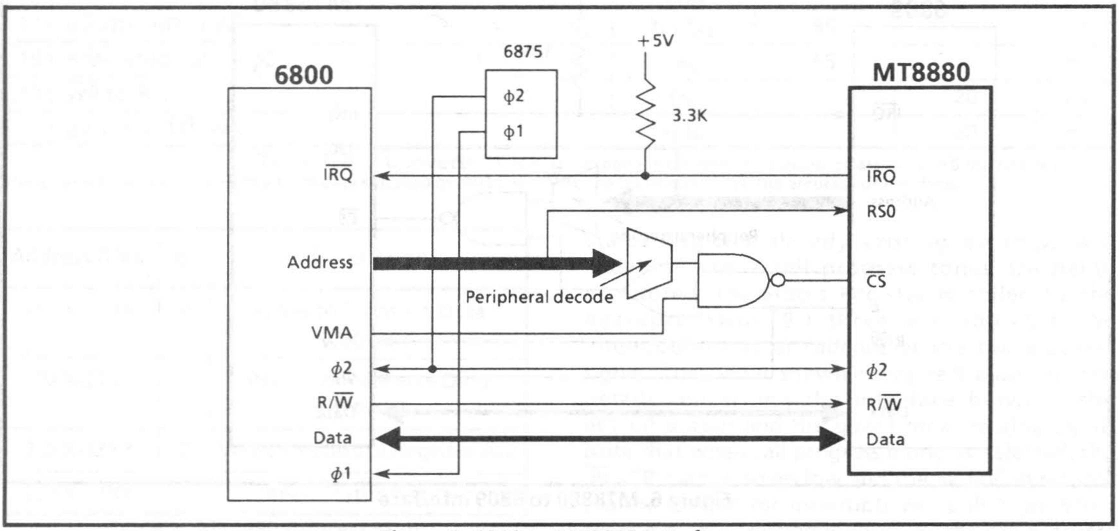


Figure 8. 6800 to MT8880 Interface

software counters in real time and as such the values shown in the program for counter verification limits must be tailored for every system due to the different clock rates in various microprocessor systems. Counter one monitors the time that the tone was interrupted (tone absent) and counter two monitors the time the tone was present. The two resulting counts are compared against the upper and lower limits initially specified in the program. These limits were found experimentally by checking the average count and then assigning suitable tolerances. An error counter allows one error from each counter and an error from the tone identification register. Reference to the flowchart in Figure 11 will clarify details.

3.3 Voice Detection Using the MT8880

Voice signals can, in fact, be detected with the MT8880. The fact that voice signals are concentrated in the 500 Hz region (on the average), allows these signals to be detected using the Call Progress mode. A very useful application for this function is in telemarketing systems that must detect when the called party has answered. The fact that most people usually respond with the word "hello" or some other short response can be used as a criteria to indicate that the called party has gone off hook and is waiting for a response. The speech detection is accomplished in exactly the same way as other call progress tones with the only difference

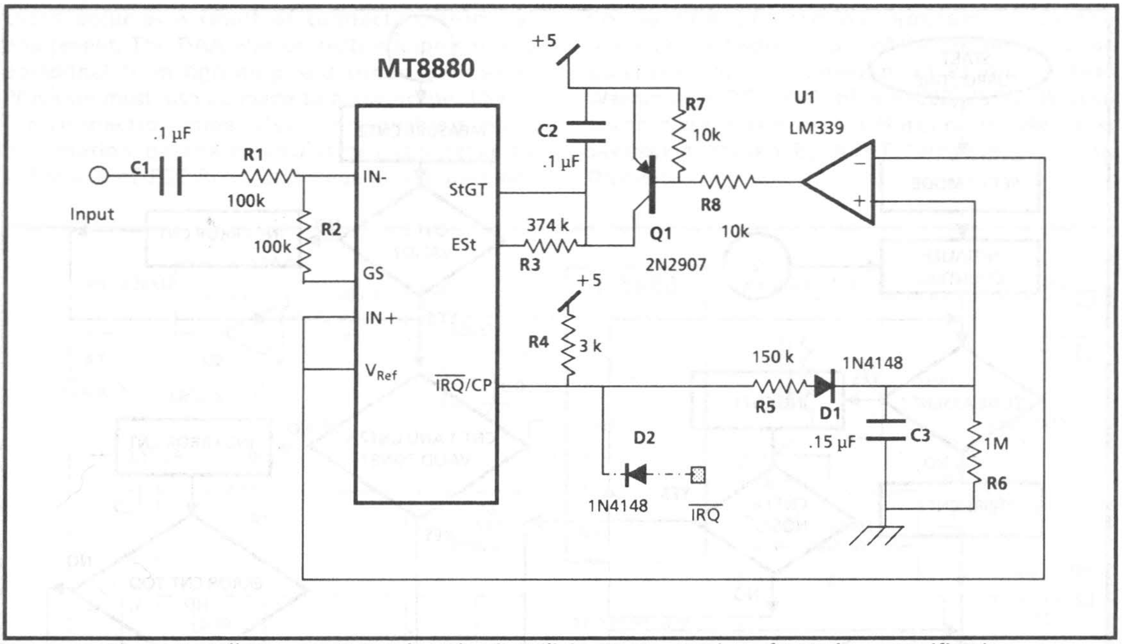


Figure 9. Call Progress Detection Circuit Utilizing Status Register for Cadence Verification

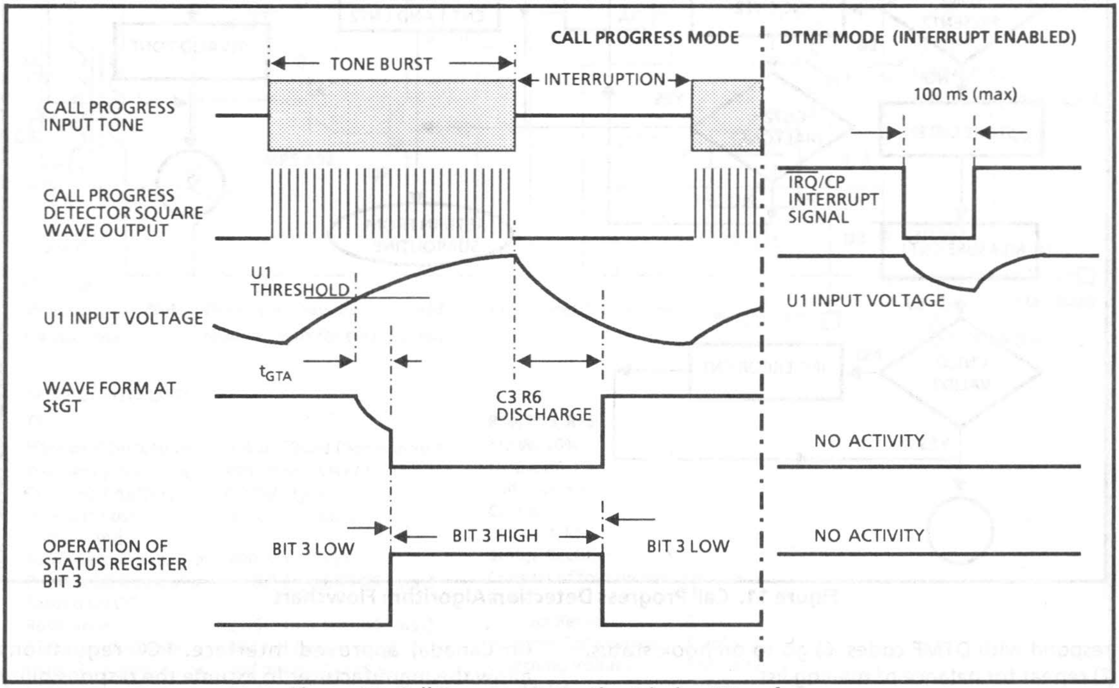


Figure 10. Call Progress Detection Timing Waveforms

being the accept/reject limits in the detection algorithm. The detection algorithm shown in Appendix 1 incorporates the voice detection function and can correctly detect "hello" with a 90% success rate. A typical scenerio using this technique would involve; 1) check for dial tone, 2) auto-dial DTMF signals 3) monitor call progress tone 4) if a called party responds with "hello", send a prerecorded sales message 5) have the customer

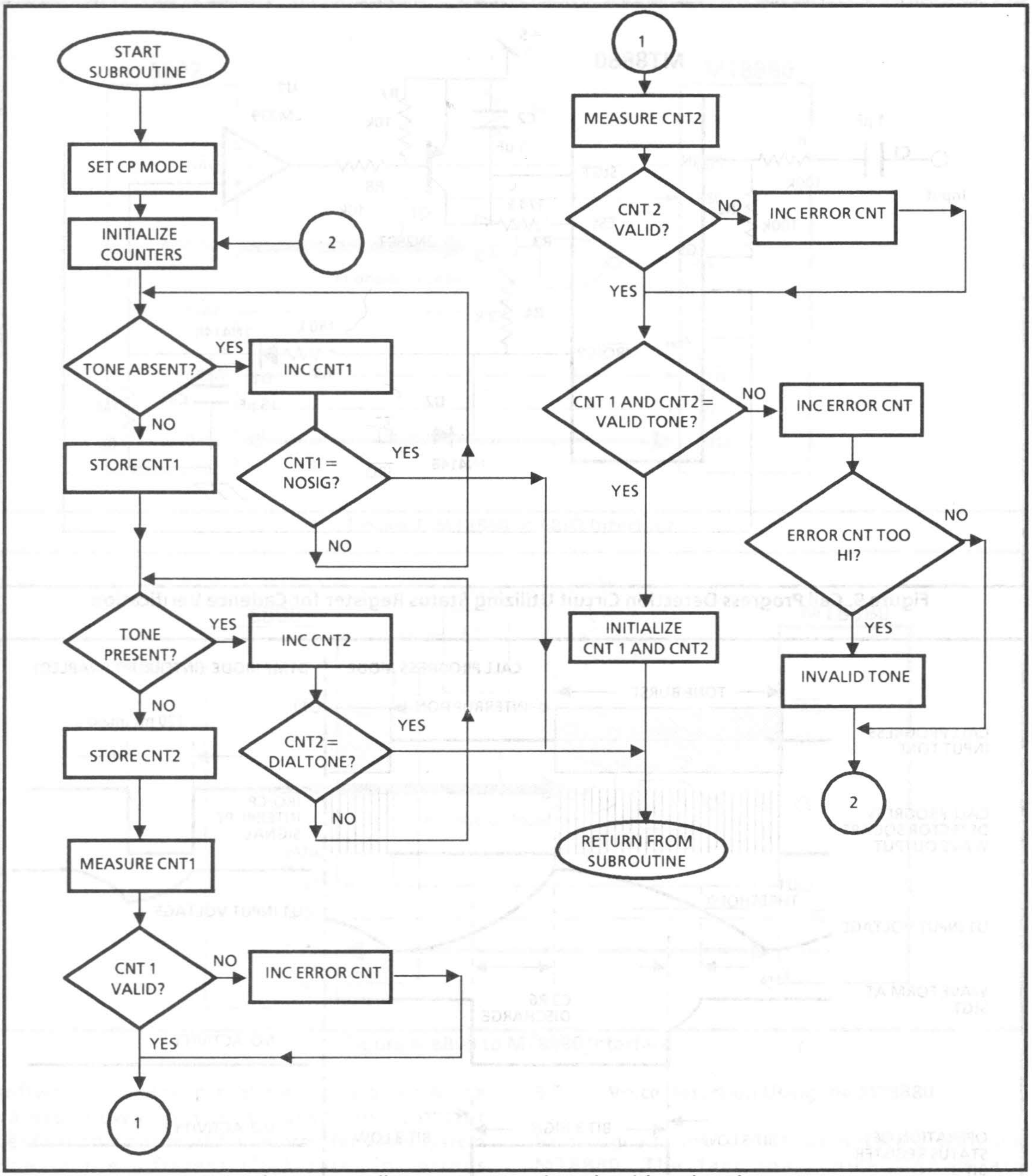


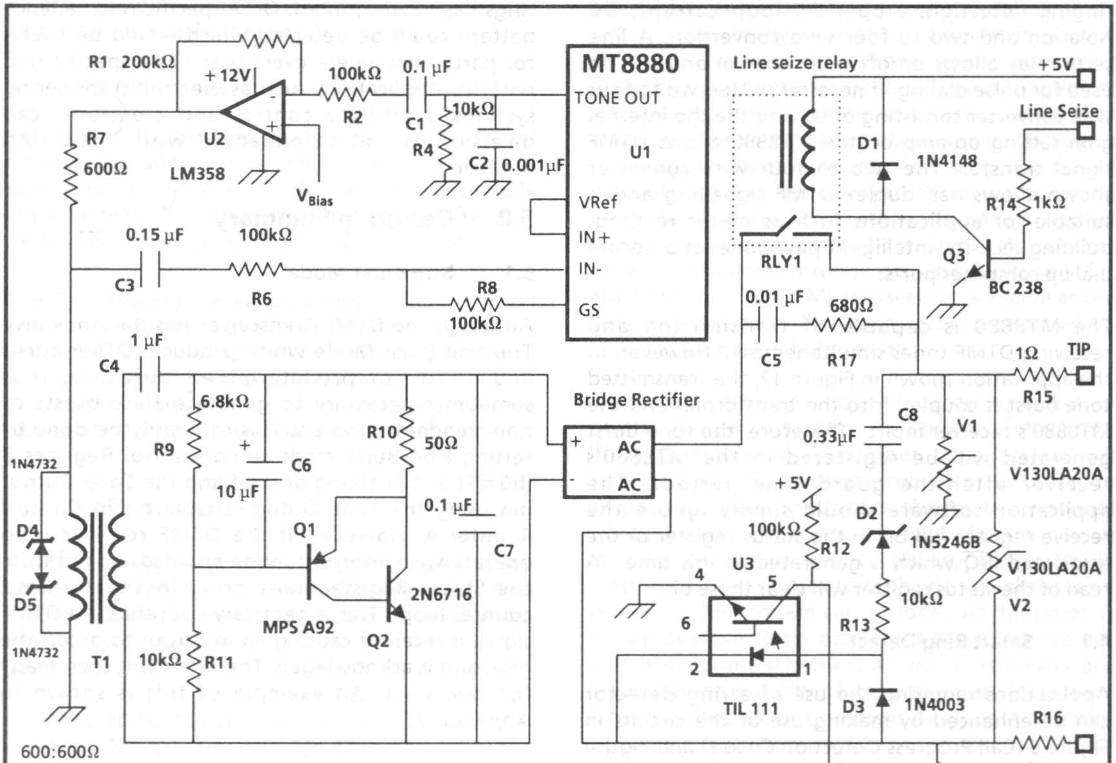
Figure 11. Call Progress Detection Algorithm Flowchart

respond with DTMF codes 6) go to on hook status. 7) repeat for balance of mailing list.

4.0 Simple Telephone Line Interface

Many applications employing the MT8880 require an interface to the telephone line to provide access to the outside world. Any system which connects to the telephone network must employ an FCC or DOC (in Canada) approved interface. FCC regulations allow the manufacturer to assume the responsibility of providing a protection and interface circuit commonly referred to as a data access arrangement (DAA). Historically, the manufacturer was not given this freedom and had to purchase a DAA from the telephone company. FCC Rules and Regulations part 68 provides a set of standards designed to protect the network from possible damage that

could occur as a result of connecting terminal equipment. The DAA also protects equipment and personnel from lightning and other transients. Provision must also be made to allow proper billing for connection time. Designers wishing more information on these regulations can refer to Volume X of FCC Rules and Regulations part 68: Connection of terminal equipment to the telephone network. A copy of the document can be obtained from the Government Printing Office, Washington, DC 20402: phone (202)-783-3238. Also another useful reference is Notes on the Network, Section 4, issued by AT&T Network Planning Division.



Note: *This circuit may require modifications to meet FCC Part 68 requirements for certification.*

COMPONENTS LIST:

T1

Harmonic Distortion:	1% at 300Hz (0dBm input)
Frequency Response:	300 Hz to 5 kHz (2dB)
Coupling Coefficient:	0.9993 (typ)
Insertion Loss:	2.0 dB (at 1kHz)
Primary and Secondary Impedance:	600Ω (at 1kHz)
Primary DC Resistance:	38.8Ω (min), 43.0Ω (max)
Secondary DC Resistance:	31.6Ω (min), 33.5Ω (max)
Primary Inductance:	462 mH (at Q = 48.6)
Secondary Inductance:	465 mH (at Q = 45.9)
Longitudinal Balance:	53 dB

U1
MITEL MT8880 DTMF Transceiver

R1, R2, R6, R8
1/4 W, 1%

R4, R7, R9, R11, R12, R13, R14, R17
1/4 W, 10%

R10, R15, R16
1/2 W, 10%

C1-C4, C6, C7
100 Volt, 5%

C5, C8
200 Volt, 5%

Bridge Rectifier
Consists of four diodes: 1N4003

RLY1

Contact Resistance:	0.5Ω
Nominal Coil Voltage:	5 Volts
Switching Voltage:	250 Volts

V1, V2, V3

Continuous Voltage:	130 Volt (RMS)
Energy:	70 Joules (10/1000 µs)
Varistor Voltage:	200 Volts (1 ma DC)
Clamp Voltage:	340 Volts (100 AMPS, 8/20µs)
Capacitance:	1900 pF

Figure 12. Telephone Line Interface

Although a DAA can be purchased separately, the cost of such a device is usually quite high and is often single sourced. The circuit shown in Figure 12 is a DAA which is optimized for the MT8880 DTMF transceiver. Although the circuit shown has not gone through the FCC approval cycle, it should not require to many alterations to gain the necessary approval. The circuit provides transient protection, ringing detection, proper DC loop current, DC isolation and two to four wire conversion. A line seize relay allows on/off hook control and can be used for pulse dialing, if necessary. The two to four wire converter consisting of U2 and the the internal gain setting op-amp on the MT8880 allows DTMF signal transfer. The two to four wire converter shown allows half duplex DTMF signalling and is suitable for applications such as meter reading, building security, intelligent payphones and secure dial up computer ports.

The MT8880 is capable of transmitting and receiving DTMF tones simultaneously. However, in the application shown in Figure 12, the transmitted tone burst is coupled into the transformer and the MT8880's receiver input. Therefore, the tone burst generated will be registered in the MT8880's receiver after the guard time period. The application software should simply ignore the receive register full bit in the status register or the associated $\overline{IRQ}$ which is generated at this time. A read of the status register will clear these bits.

4.1 Smart Ring Detect

Applications requiring the use of a ring detector can be enhanced by making use of the circuits in Figure 9 (Call Progress Detection Circuit) and Figure 12. The circuit in Figure 9 could be modified to allow the ring detector output (U3 in Figure 12) to trigger the Steering/Guard Time circuit normally used for the DTMF receiver. This would provide a means of detecting the presence of ringing voltage with the MT8880 (in Call Progress mode) by monitoring the state of bit 3 in the Status Register. A counter in the applications software could monitor the number of ring bursts and cause an off hook condition when a predetermined number of rings has been counted. Or, a specific ring cadence pattern could be detected which would be useful for party lines where every user has a specific ring pattern. Applications such as electronic answering systems, appliance control and electronic call diversion can all be enhanced with smart ring detection.

5.0 Design-In Summary

5.1 Non Burst Mode

Although the DTMF Transceiver has an innovative Transmit Burst Mode which produces DTMF bursts and pauses of predetermined duration, it is sometimes necessary to generate tone bursts of non-standard duration. This can easily be done by setting Non Burst mode using Control Register B (b0 = 1) and enabling or disabling the Tone Output pin using the Tone Output Enable bit in Control Register A. However, if the DTMF receiver is to operate with Interrupt mode enabled, a read from the Status Register must occur in the transmit counter loop. This is necessary such that if a DTMF signal is received causing an interrupt to occur, the interrupt is acknowleged. The receiver is then ready for new data. An example of this is shown in Appendix 2.

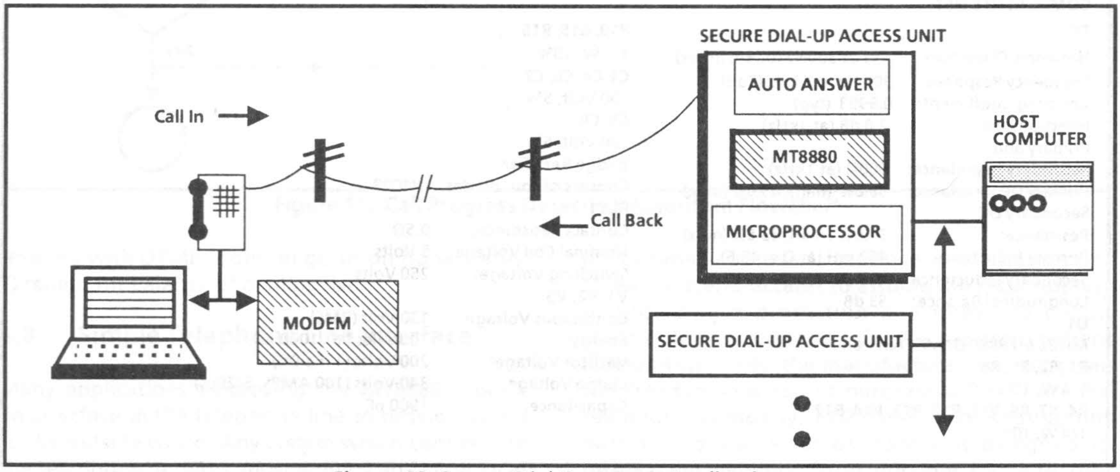


Figure 13. Secure Dial Up Access Application

5.2 Clock Oscillator

The MT8880 employs an on chip oscillator circuit that is completed with the addition of a 3.5795 MHz crystal. Multiple devices can be driven with a single clock source by driving OSC 1 on all devices. The driver should be capacitively coupled through a 0.01µf capacitor. Alternatively, the devices can be daisy chained (with limitations) such that the first device in the chain is the master oscillator.

5.3 Power Supply

Steps should be taken through the use of decoupling capacitors or other means to reduce power supply noise at the device. This is especially important in Call Progress mode since noise may cause random toggling on the $\overline{IRQ}$/CP output.

The Call Progress detect threshold is set to a level which is determined by the hysteresis on the Schmitt trigger used in the DTMF low group bandsplit filter. This level is quite low and is not adjustable. However, some adjustment can be obtained by altering the gain of the on chip op-amp.

5.4 Software Reset

A software reset is necessary on power up since the device may come up in an unknown state. The sequence is quite simple and should be used at the beginning of all programs.
Reset Sequence:

Write 00(hex) to CONTROL REGISTER
Write 00(hex) to CONTROL REGISTER
Write 08(hex) to CONTROL REGISTER
Write 00(hex) to CONTROL REGISTER

5.5 Use of Phase 2 (ϕ2) Input

The bus architecture is optimized for the MOTOROLA 6802 Microprocessor and as such requires a Phase 2 signal. This signal is not only necessary for data transfers but must also be present to update the Status Register. If data is not being transferred, the Phase 2 clock period can be increased to as long as 1 ms. A period longer than 1 ms may result in lost data.

5.6 CP Mode to DTMF Mode Delay

The transition from Call Progress mode to DTMF mode requires a finite time determined partially by the filter circuitry. Applications that require DTMF signals to be received directly after exiting Call Progress mode, which could be the case for smart ring detection, require at least 10 ms when switching to DTMF mode to insure that no DTMF data is lost.

6.0 APPLICATIONS

6.1 Secure Dial-Up Port for Modems

There has been an increasing interest in providing additional protection for computer systems. There are certainly many aspects to consider in a total security system ranging from secure operating system techniques to secure data base management systems. A hardware oriented secure access system and the systems mentioned above can be combined to achieve a highly secure network. Hardware oriented secure access systems are becoming popular as a result of the increased use of microprocessor based computers to access networked systems through dial up telephone links. The Mitel MT8880 DTMF transceiver can serve as the heart of a call-back-telephone-access product which provides a high level of security.

A popular method for limiting access to a dial up port in the past has been to simply refrain from listing the telephone number. This action will certainly limit abuse of the computer to a certain degree but may introduce problems to personnel which should have access. However, for the person looking for a computer to abuse, it is a simple matter to dial sequential phone numbers and search for the modem carrier tone. At this point it is then possible to try passwords or attempt to get past encryption schemes. As more attempts are made, the probability of gaining access increases. A fairly recent scheme employs a call-back protocol whereby a unit connected between the modem (at the host end) and the telephone line automatically answers an incoming call without an acknowledgement tone. Alternatively, when the call is answered a false busy signal can be issued such that unauthorized persons will be led to believe that the line is in a busy condition. Whatever scheme is used, once the host has answered the call an access code is entered using DTMF signalling. Once a code has been entered, the secure access unit goes on hook. After matching the access code with a preprogrammed telephone number the call is returned at which time normal modem handshaking activity occurs followed by data transmission. A slightly different scheme which would allow the user to change locations at will involves the use of an encoded telephone number which is entered after the access code. The secure access unit decodes the telephone number and does a call back to that location. Attempts to gain access by unauthorized personnel could trigger an alarm condition such that the system operator would be notified and appropriate

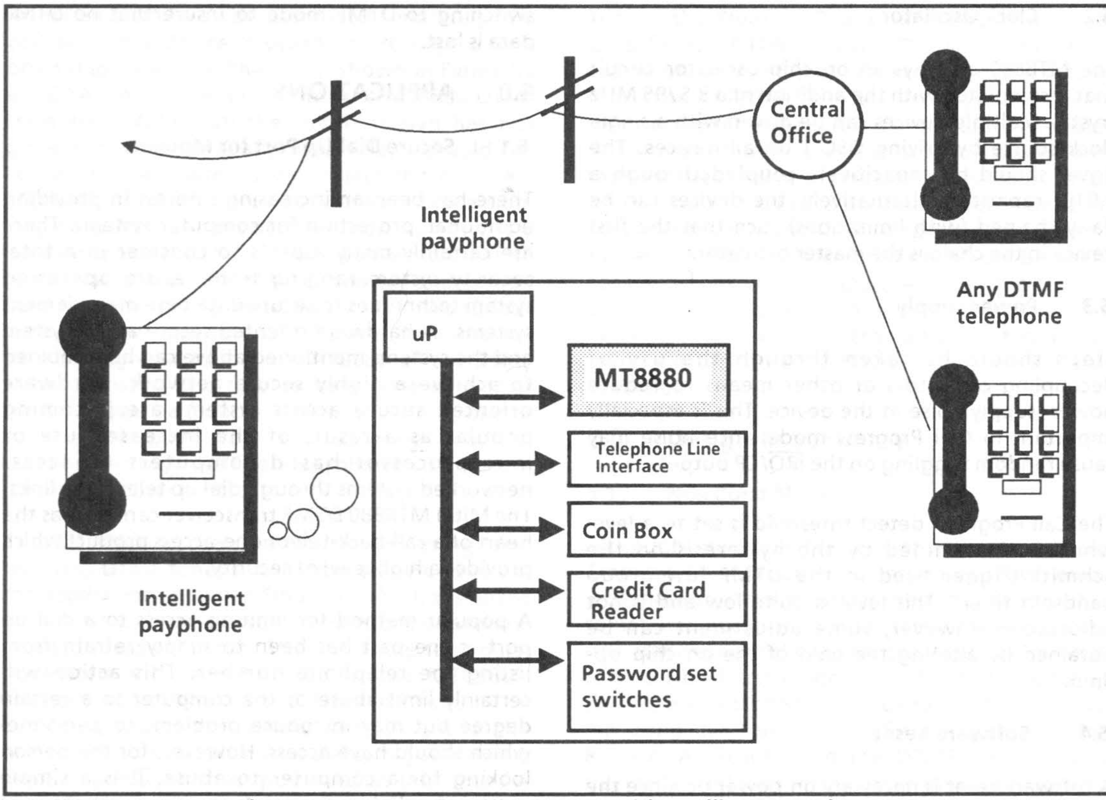


Figure 14. Program Your Own Rates With Intelligent Payphone

action taken. A data switch serving a large network could be fitted with a secure access unit at each dial up port providing a high level of security for sensitive data. Also, users of smaller networks such as those found in real estate or sales applications could benefit from added security. Figure 13 shows a typical arrangement.

6.2 Intelligent Payphone

Intelligent payphones can be installed in such places as variety or convenience stores, bowling alleys and other suitable locations and used as a source of income for the owner. Persons wanting to use the phone must deposit the fee as programmed by an authorized user. The MT8880 can play a key role in such an intelligent pay telephone system and is illustrated in Figure 14.

Any person having the phone number and password of a specific intelligent payphone can do such things as program the calling rates, check the amount of coin in the box or even check to see if the phone has been vandalized. An FCC approved data access arrangement must be used to connect the system to telephone lines with an automatic ring detect circuit answering incoming calls. Upon receiving an incoming call, the software could be set up such that the payphone issues a false ringback tone or busy tone to discourage unauthorized users. Personnel with the password, however, could simply enter DTMF codes over the false call progress tones to gain access. Once the password has been correctly entered (from any DTMF phone) commands can then be entered.

APPENDIX 1
Call Progress and Voice Detection Algorithm

```
1                *
2                * THIS PROGRAM PROVIDES AN ALGORITHM TO CHECK THE
3                * CADENCE OF CALL PROGRESS SIGNALS. THE CALL PROGRESS DETECT CIRCUIT
4                * MUST BE USED. THE CIRCUIT UTILIZES A CHARGE PUMP WHICH FEEDS INTO
5                * THE ANALOG GUARD TIME CIRCUIT NORMALLY USED FOR DTMF. WHEN IN
6                * DTMF MODE, TRANSISTOR Q1 IS IN A HIGH IMPEDANCE STATE
7                * THUS NOT AFFECTING THE NORMAL OPERATION OF THE GUARD TIME CIRCUIT.
8                * IF OPERATING IN INTERRUPT MODE IRQ/CP IS NORMALLY HIGH, HOWEVER
9                * INTERRUPTS MUST BE SERVICED WITHIN 200MS OR THE DTMF TIMING WILL BE
10               * TEMPORARILY CORRUPTED. THIS INTERRUPT SERVICE TIME CAN BE ADJUSTED
11               * WITH C3 AND R6.
12               * IN PRACTICE THE STATUS REGISTER (BIT 3) IS POLLED LOOKING FOR THE
13               * CONDITION OF BIT 3. THIS PROGRAM HAS TWO COUNTERS. COUNTER 1 DETERMINES
14               * HOW LONG THERE IS AN ABSENCE OF ENERGY IN THE PASSBAND AND COUNTER 2
15               * DETERMINES HOW LONG THERE IS A PRESENCE OF ENERGY IN THE PASSBAND.
16               * AN ERROR COUNTER ALLOWS ERRORS FROM THE SIGNAL ABSENT AND SIGNAL PRESENT
17               * COUNTERS IN ADDITION TO THE COUNT MATCH REGISTER.
18               * THE RESULT OF THE DETECT ALGORITHM IS PRINTED ON THE CRT
19               * ALSO, A FORM SPEECH DETECTION ALGORITHM INDICATES WHEN THE WORD 'HELLO'
20               * HAS BEEN RECEIVED AT THE INPUT OF THE MT8880.
21               *
22    4400       START EQU $4400
23    2000       TXRX EQU $2000
24    2001       CRSR EQU $2001
25    8662       CRLF EQU $8662
26    867B       HEX4 EQU $867B
27    8655       HEAD EQU $8655
28    8686       HEX2 EQU $8686
29    866E       SPACE2 EQU $866E
30               *              M.J.R.  MAR 1986
31               * CPVREF.LST
32    4400       ORG START
33               *
34               * PROGRESS TONE IDENTIFIER DATA
35               *
36    4400 A     86   00   LDAA #$00
37    4402 A     B7   479D STAA REORDR ;TONE 1 REORDER TONE
38    4405 A     86   01   LDAA #$01
39    4407 A     B7   479C STAA RNGBK ;TONE 2 RINGBACK TONE
40    440A A     86   02   LDAA #$02
41    440C A     B7   479B STAA BUSY ;TONE 3 BUSY TONE
42    440F A     86   03   LDAA #$03
43    4411 A     B7   479E STAA DIALTN ;TONE 4 DIAL TONE
44    4414 A     86   04   LDAA #$04
45    4416 A     B7   479F STAA NOTONE ;TONE 5 NO SIGNAL
46    4419 A     86   05   LDAA #$05
47    441B A     B7   47A0 STAA HELLO ;TONE 6 HELLO
48               *
49               * ERROR COUNT
50               *
51    441E A     C6   04   LDAB #$04
52    4420 A     B7   47A3 STAA ERRCNT
53               *
54               * TONE IDENTIFIERS
```

```
55            *
56  4423 A  CE  0000 LDX #$0000
57  4426 A  FF  47A8 STX REORDX

MODULE;    MICROBENCH 6800 CROSS ASSEMBLER (V2)-257  18-MAR-86 16:14:56 PAGE 2

 1  4429 A  CE  0101 LDX #$0101
 2  442C A  FF  47A6 STX RNGBKX
 3  442F A  CE  0002 LDX #$0002
 4  4432 A  FF  47A4 STX BUSYX
 5  4435 A  CE  0303 LDX #$0303
 6  4438 A  FF  47AA STX DIALX
 7  443B A  CE  0404 LDX #$0404
 8  443E A  FF  47AC STX NOTONX
 9  4441 A  CE  0505 LDX #$0505
10  4444 A  FF  47AE STX HELLOX
11            *      TONE 1 PRESENT LIMITS
12            *
13  4447 A  CE  0400 LDX #$0900 ;LOWER LIMIT
14  444A A  FF  4848 STX TLO1LL
15  444D A  CE  04FF LDX #$0AFF ;UPPER LIMIT
16  4450 A  FF  484A STX TLO1UL
17            *
18            *      TONE 1 ABSENT LIMITS
19            *
20  4453 A  CE  0A00 LDX #$0500 ;LOWER LIMIT
21  4456 A  FF  484C STX THI1LL
22  4459 A  CE  0C00 LDX #$0600 ;UPPER LIMIT
23  445C A  FF  484E STX THI1UL
24            *
25            *      TONE 2 PRESENT LIMITS
26            *
27  445F A  CE  6D00 LDX #$7200 ;LOWER LIMIT
28  4462 A  FF  4850 STX TLO2LL
29  4465 A  CE  6EFF LDX #$74FF ;UPPER LIMIT
30  4468 A  FF  4852 STX TLO2UL
31            *
32            *      TONE 2 ABSENT LIMITS
33            *
34  446B A  CE  4050 LDX #$3B00 ;LOWER LIMIT
35  446E A  FF  4854 STX THI2LL
36  4471 A  CE  4255 LDX #$3DFF ;UPPER LIMIT
37  4474 A  FF  4856 STX THI2UL
38            *      TONE 3 PRESENT LIMITS
39            *
40  4477 A  CE  0400 LDX #$0900 ;LOWER LIMIT
41  447A A  FF  4858 STX TLO3LL
42  447D A  CE  04FF LDX #$0AFF ;UPPER LIMIT
43  4480 A  FF  485A STX TLO3UL
44            *
45            *      TONE 3 ABSENT LIMITS
46            *
47  4483 A  CE  13A0 LDX #$0E00;LOWER LIMIT
48  4486 A  FF  485C        STX THI3LL
49  4489 A  CE  1460 LDX #$0F20 ;UPPER LIMIT
50  448C A  FF  485E STX THI3UL
51            *
52            *      TONE 4 PRESENT LIMITS
53            *
```

```
54    448F A   CE   5000 LDX #$5000 ;LOWER LIMIT
55    4492 A   FF   4860 STX THI4LL
56    4495 A   CE   5010 LDX #$5010 ;UPPER LIMIT
57    4498 A   FF   4862 STX THI4UL

MODULE;    MICROBENCH 6800 CROSS ASSEMBLER (V2)-257 18-MAR-86 16:14:56 PAGE 3
1                    *
2                    *        NOTONE 5  SIGNAL ABSENT LIMITS

3                    *
4     449B A   CE   9000 LDX #$9000
5     449E A   FF   4864 STX TLO5LL
6     44A1 A   CE   9010 LDX #$9010
7     44A4 A   FF   4866 STX TLO5UL
8                    *
9                    *
10                   *        HELLO 6  SIGNAL PRESENT LIMIT
11                   *
12    44A7 A   CE   05BA LDX #$05BA ;TONE 6 LOWER LIMIT
13    44AA A   FF   486C STX THI6LL
14    44AD A   CE   0CFF LDX #$08FF ;TONE 6 UPPER LIMIT
15    44B0 A   FF   486E STX THI6UL
16                   *
17                   *
18                   *        HELLO 6 SIGNAL ABSENT LIMIT
19                   *
20    44B3 A   CE   1000 LDX #$1000 ; TONE 6 LOWER LIMIT
21    44B6 A   FF   4868 STX TLO6LL
22    44B9 A   CE   8000 LDX #$8000 ; TONE 6 UPPER LIMIT
23    44BC A   FF   486A STX TLO6UL
24                   *
25                   * RESET
26                   *
27    44BF A   86   00   LDAA #$00
28    44C1 A   B7   2001 STAA CRSR
29    44C4 A   B7   2001 STAA CRSR
30    44C7 A   86   08   LDAA #$08
31    44C9 A   B7   2001 STAA CRSR
32    44CC A   86   00   LDAA #$00
33    44CE A   B7   2001 STAA CRSR
34                   *
35                   * CALL PROGRESS MODE WITH IRQ ENABLED
36                   *
37    44D1 A   86   06   LDAA #$06
38    44D3 A   B7   2001 STAA CRSR
39                   *
40                   * MAIN PROGRAM
41                   *
42    44D6 A   BD   44FA JSR RESET
43    44D9 A   BD   4516 JSR CHECB3
44    44DC A   BD   4536 JSR PRIME
45    44DF A   BD   452C MORINC JSR MORB3
46    44E2 A   BD   4516 JSR CHECB3
47    44E5 A   BD   45B3 JSR MEASLO
48    44E8 A   BD   4548 JSR MEASHI
49    44EB A   BD   4621 JSR MATCH
50    44EE A   BD   4689 JSR CHERR
51    44F1 A   BD   469F JSR PRINT
52    44F4 A   BD   4536 JSR PRIME
```

```
53   44F7 A  7E  44DF JMP MORINC
54               *
55   44FA A  CE  0000RESET LDX #$0000
56   44FD A  FF  4844 STX CNT1
57   4500 A  FF  4846 STX CNT2

MODULE;     MICROBENCH 6800 CROSS ASSEMBLER (V2)-257  18-MAR-86 16:14:56 PAGE 4

1                *
2                * SET ERROR COUNTER
3                *
4    4503 A  F6  47A3 LDAB ERRCNT
5    4506 A  F7  47A1 STAB MATERR
6    4509 A  39       RTS
7                *
8                * START OF DETECT ALGORITHM
9                * COUNTER 1 CHECKS TO SEE HOW LONG
10               * BIT 3 IS HI (ABSENCE OF SIGNAL)
11               *
12   450A A  FE  4844INCCNT LDX CNT1
13   450D A  08   INX
14   450E A  FF  4844 STX CNT1
15   4511 A  BC  4862 CPX THI4UL
16   4514 A  22  32   BHI MEASHI
17               *
18   4516 A  F6  2001CHECB3 LDAB CRSR
19   4519 A  C4  08   ANDB #$08
20   451B A  C1  08   CMPB #$08
21   451D A  27  EB   BEQ INCCNT
22   451F A  39       RTS
23               *
24               *
25               *
26               * COUNTER 2 CHECKS TO SEE HOW LONG ENERGY IS PRESENT
27               *
28   4520 A  FE  4846MORCNT LDX CNT2
29   4523 A  08   INX
30   4524 A  FF  4846 STX CNT2
31   4527 A  BC  4866 CPX TLO5UL
32   452A A  22  1A   BHI PATCH1
33               *
34   452C A  B6  2001MORB3 LDAA CRSR
35   452F A  84  08   ANDA #$08
36   4531 A  81  08   CMPA #$08
37   4533 A  26  EB   BNE MORCNT
38   4535 A  39       RTS
39               *
40   4536 A  CE  0000PRIME LDX #$0000
41   4539 A  FF  4844 STX CNT1
42   453C A  FF  4846 STX CNT2
43   453F A  CE  FFFF LDX #$FFFF
44   4542 A  FF  4842 STX MATCHA
45   4545 A  39       RTS
46               *
47               *
48   4546 A  20  6B   PATCH1 BRA MEASLO
49               *
50               * COMPARE THE LOWER LIMIT AND UPPER LIMIT TO CNT1 WHICH
51               * CONTAINS THE TIME THE PROGRESS TONE WAS PRESENT
```

```
52                 *
53   4548 A  FE    4844MEASHI LDX CNT1
54                 *
55   454B A  BD    867B JSR HEX4
56                 *
57   454E A  FE    4844 LDX CNT1
MODULE;    MICROBENCH 6800 CROSS ASSEMBLER (V2)-257  18-MAR-86 16:14:56 PAGE 5

1    4551 A  BC    484C CPX THI1LL
2    4554 A  22    17    BHI CHH1UL
3    4556 A  BC    4854TH2LL CPX THI2LL
4    4559 A  22    1A    BHI CHH2UL
5    455B A  BC    485C TH3LL CPX THI3LL
6    455E A  22    1D    BHI CHH3UL
7    4560 A  BC    4860TH4LL CPX THI4LL ;ONLY CHECK THE LOWER LIMIT TONE PRESENT FOR DIALTONE
8    4563 A  22    3D    BHI T4HIID
9    4565 A  BC    486C TH6LL CPX THI6LL
10   4568 A  22    1B    BHI CHH6UL
11   456A A  7E    4676 JMP NONID
12                 *
13   456D A  BC    484ECHH1UL CPX THI1UL
14   4570 A  23    1B    BLS T1HIID
15   4572 A  7E    4556 JMP TH2LL
16   4575 A  BC    4856CHH2UL CPX THI2UL
17   4578 A  23    1A    BLS T2HIID
18457A A   7E    455B JMP TH3LL
19   457D A  BC    485ECHH3UL CPX THI3UL
20   4580 A  23    19    BLS T3HIID
21   4582 A  7E    4560 JMP TH4LL
22   4585 A  BC    486ECHH6UL CPX THI6UL
23   4588 A  23    22    BLS T6HIID
24   458A A  7E    4676 JMP NONID
25                 *
26                 * IDENTIFY THE MEASURED VALUE
27                 *
28   458D A  B6    479D T1HIID LDAA REORDR
29   4590 A  B7    4843 STAA MATCHB
30   4593 A  39          RTS
31                 *
32   4594 A  B6    479C T2HIID LDAA RNGBK
33   4597 A  B7    4843 STAA MATCHB
34   459A A  39          RTS
35                 *
36   459B A  B6    479B T3HIID LDAA BUSY
37   459E A  B7    4843STAA MATCHB
38   45A1 A  39          RTS
39                 *
40   45A2 A  B6    479ET4HIID LDAA DIALTN
41   45A5 A  B7    4842 STAA MATCHA
42   45A8 A  B7    4843 STAA MATCHB ;STORE IN MATCHA AND MATCHB SINCE ONLY CHECKING PRESENT TIME
43   45AB A  39          RTS
44                 *
45   45AC A  B6    47A0 T6HIID LDAA HELLO
46   45AF A  B7    4843 STAA MATCHB
47   45B2 A  39          RTS
48                 *
49                 * COMPARE THE LOWER LIMIT AND UPPER LIMIT TO CNT2
50                 * WHICH CONTAINS THE TIME THE PROGRESS TONE WAS ABSENT
```

```
51                  *
52   45B3 A   FE    4846MEASLO LDX CNT2
53                  *
54   45B6 A   BD    867B JSR HEX4
55   45B9 A   BD    866E JSR SPACE2
56                  *
57   45BC A   FE    4846 LDX CNT2
```

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```
1    45BF A   BC    4848 CPX TLO1LL
2    45C2 A   22    17    BHI CHL1UL
3    45C4 A   BC    4850TL2LL CPX TLO2LL
4    45C7 A   22    1A    BHI CHL2UL
5    45C9 A   BC    4858TL3LL CPX TLO3LL
6    45CC A   22    1D    BHI CHL3UL
7    45CE A   BC    4864TL5LL CPX TLO5LL
8    45D1 A   22    3D    BHI T5LOID
9    45D3 A   BC    4868TL6LL CPX TLO6LL
10   45D6 A   22    1B    BHI CHL6UL
11   45D8 A   7E    4676 JMP NONID
12                  *
13   45DB A   BC    484A CHL1UL CPX TLO1UL
14   45DE A   23    1B    BLS T1LOID
15   45E0 A   7E    45C4 JMP TL2LL
16   45E3 A   BC    4852CHL2UL CPX TLO2UL
17   45E6 A   23    1A   BLS T2LOID
18   45E8 A   7E    45C9 JMP TL3LL
19   45EB A   BC    485A CHL3UL CPX TLO3UL
20   45EE A   23    19    BLS T3LOID
21   45F0 A   7E    45CE JMP TL5LL
22   45F3 A   BC    486A CHL6UL CPX TLO6UL
23   45F6 A   23    22    BLS T6LOID
24   45F8 A   7E    4676 JMP NONID
25                  *
26                  * IDENTIFY THE MEASURED VALUE
27                  *
28   45FB A   B6    479D T1LOID LDAA REORDR
29   45FE A   B7    4842 STAA MATCHA
30   4601 A   39          RTS
31                  *
32   4602 A   B6    479C T2LOID LDAA RNGBK
33   4605 A   B7    4842 STAA MATCHA
34   4608 A   39          RTS
35                  *
36   4609 A   B6    479B T3LOID LDAA BUSY
37   460C A   B7    4842 STAA MATCHA
38   460F A   39          RTS
39                  *
40   4610 A   B6    479FT5LOID LDAA NOTONE
41   4613 A   B7    4842STAA MATCHA
42   4616 A   B7    4843STAA MATCHB
43   4619 A   39          RTS
44                  *
45   461A A   B6    47A0 T6LOID LDAA HELLO
46   461D A   B7    4842 STAA MATCHA
47   4620 A   39          RTS
48                  *
49   4621 A   FE    4842MATCH LDX MATCHA
```

```
50   4624 A  BC  47A4 CPX BUSYX
51   4627 A  27  1C   BEQ BUSY1
52   4629 A  BC  47A6 CPX RNGBKX
53   462C A  27  20   BEQ RNGBK1
54   462E A  BC  47A8 CPX REORDX
55   4631 A  27  25   BEQ REORD1
56   4633 A  BC  47AA CPX DIALX
57   4636 A  27  2A   BEQ DIALT1
```

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```
1    4638 A  BC  47AC CPX NOTONX
2    463B A  27  2F   BEQ NOTON1
3    463D A  BC  47AE CPX HELLOX
4    4640 A  27  3D   BEQ HELLO1
5    4642 A  7E  4676 JMP NONID
6            *
7            *
8            *
9    4645 A  CE  46A9 BUSY1 LDX #MSG1
10   4648 A  C6  02   LDAB #$02
11   464A A  F7  47A1 STAB MATERR
12   464D A  39       RTS
13   464E A  CE  46CD RNGBK1 LDX #MSG2
14   4651 A  F6  47A3 LDAB ERRCNT
15   4654 A  F7  47A1 STAB MATERR
16   4657 A  39       RTS
17   4658 A  CE  46F5 REORD1 LDX #MSG3
18   465B A  F6  47A3 LDAB ERRCNT
19   465E A  F7  47A1 STAB MATERR
20   4661 A  39       RTS
21   4662 A  CE  471C DIALT1 LDX #MSG4
22   4665 A  F6  47A3 LDAB ERRCNT
23   4668 A  F7  47A1 STAB MATERR
24   466B A  39       RTS
25   466C A  CE  4740 NOTON1 LDX #MSG5
26   466F A  F6  47A3 LDAB ERRCNT
27   4672 A  F7  47A1 STAB MATERR
28   4675 A  39       RTS
29   4676 A  CE  474E NONID LDX #MSG6
30   4679 A  C6  00   LDAB #$00
31   467B A  F7  47A2 STAB ERFLAG
32   467E A  39       RTS
33   467F A  CE  4770 HELLO1 LDX #MSG7
34   4682 A  F6  47A3 LDAB ERRCNT
35   4685 A  F7  47A1 STAB MATERR
36   4688 A  39       RTS
37   4689 A  F6  47A1 CHERR LDAB MATERR
38   468C A  F1  47A2 CMPB ERFLAG
39   468F A  2F  04   BLE UNIDEN
40   4691 A  7A  47A1 DEC MATERR
41   4694 A  39       RTS
42   4695 A  CE  4776 UNIDEN LDX #INVLD
43   4698 A  F6  47A3 LDAB ERRCNT
44   469B A  F7  47A1 STAB MATERR
45   469E A  39       RTS
46           *
47   469F A  BD  8662 PRINT JSR CRLF
48   46A2 A  BD  8655 JSR HEAD
```

15

```
49   46A5 A  BD   866E JSR SPACE2
50   46A8 A  39        RTS
51           *
52           *
53           *
54           *
55           *
56   46A9 A  54   48   MSG1 FCC 'THE SIGNAL NOW PRESENT IS BUSY TONE'
57   46CC A  00        FCB 0
```

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```
1    46CD A  54   48   MSG2 FCC 'THE SIGNAL NOW PRESENT IS RINGBACK TONE'
2    46F4 A  00        FCB 0
3    46F5 A  54   48   MSG3 FCC 'THE SIGNAL NOW PRESENT IS REORDER TONE'
4    471B A  00        FCB 0
5    471C A  54   48   MSG4 FCC 'THE SIGNAL NOW PRESENT IS DIAL TONE'
6    473F A  00        FCB 0
7    4740 A  4E   4F   MSG5 FCC 'NO SIGNAL....
8    474D A  00        FCB 0
9    474E A  50   4C   MSG6 FCC 'PLEASE WAIT....PROCESSING TONE ID'
10   476F A  00        FCB 0
11   4770 A  48   45   MSG7 FCC 'HELLO'
12   4775 A  00        FCB 0
13   4776 A  54   48   INVLD FCC 'THE TONE NOW PRESENT IS UNIDENTIFIED'

14   479A A  00        FCB 0
15           *
16           *
17   479B A            BUSY RMB 1
18   479C A            RNGBK RMB 1
19   479D A            REORDR RMB 1
20   479E A            DIALTN RMB 1
21   479F A            NOTONE RMB 1
22   47A0 A            HELLO RMB 1
23           *
24   47A1 A            MATERR RMB 1
25   47A2 A            ERFLAG RMB 1
26   47A3 A            ERRCNT RMB 1
27           *
28   47A4 A            BUSYX RMB 2
29   47A6 A            RNGBKX RMB 2
30   47A8 A            REORDX RMB 2
31   47AA A            DIALX RMB 2
32   47AC A            NOTONX RMB 2
33   47AE A            HELLOX RMB 2
34           *
35   47B0 A            RAMSG RMB 146
36   4842 A            MATCHA RMB 1
37   4843 A            MATCHB RMB 1
38   4844 A            CNT1 RMB 2 ;TONE ABSENT COUNT
39   4846 A            CNT2 RMB 2 ;TONE PRESENT COUNT
40           *
41   4848 A            TLO1LL RMB 2 ;TONE 1 ABSENT LOWER LIMIT
42   484A A            TLO1UL RMB 2 ;TONE 1 ABSENT UPPER LIMIT
43   484C A            THI1LL RMB 2 ;TONE 1 PRESENT LOWER LIMIT
44   484E A            THI1UL RMB 2 ;TONE 1 PRESENT UPPER LIMIT
45           *
46   4850 A            TLO2LL RMB 2 ;TONE 2 ABSENT LOWER LIMIT
```

```
47      4852 A          TLO2UL RMB 2 ;TONE 2 ABSENT UPPER LIMIT
484854 A              THI2LL RMB 2 ;TONE 2 PRESENT LOWER LIMIT
49      4856 A          THI2UL RMB 2 ;TONE 2 PRESENT UPPER LIMIT
50              *
51      4858 A          TLO3LL RMB 2 ;TONE 3 ABSENT LOWER LIMIT
52      485A A          TLO3UL RMB 2 ;TONE 3 ABSENT UPPER LIMIT
53      485C A          THI3LL RMB 2 ;TONE 3 PRESENT LOWER LIMIT
54      485E A          THI3UL RMB 2 ;TONE 3 PRESENT UPPER LIMIT
55              *
56      4860 A          THI4LL RMB 2 ;TONE 4 PRESENT LOWER LIMIT
57      4862 A          THI4UL RMB 2 ;TONE 4 PRESENT UPPER LIMIT

MODULE;    MICROBENCH 6800 CROSS ASSEMBLER (V2)-257  18-MAR-86 16:14:56 PAGE 9

1               *
2       4864 A          TLO5LL RMB 2 ;TONE ABSENT LOWER LIMIT
3       4866 A          TLO5UL RMB 2 ;TONE ABSENT UPPER LIMIT
4               *
5       4868 A          TLO6LL RMB 2
6       486A A          TLO6UL RMB 2
7       486C A          THI6LL RMB 2
8       486E A          THI6UL RMB 2
9               *
10              END

MODULE;    MICROBENCH 6800 CROSS ASSEMBLER (V2)-257  18-MAR-86 16:14:56 PAGE 10
SYMBOL TABLE

BUSY  479B  BUSYX  47A4    BUSY1  4645
CHECB34516    CHERR  4689
CHH1UL 456D   CHH2UL 4575   CHH3UL 457D   CHH6UL 4585   CHL1UL 45DB
CHL2UL 45E3   CHL3UL 45EB   CHL6UL 45F3   CNT1  4844  CNT2  4846
CRLF  = 8662  CRSR  = 2001  DIALTN 479E   DIALT1 4662   DIALX  47AA
ERFLAG 47A2   ERRCNT 47A3   HEAD  = 8655  HELLO  47A0   HELLOX 47AE
HELLO1 467F   HEX2  = 8686  HEX4  = 867B  INCCNT 450A   INVLD  4776
MATCH  4621   MATCHA 4842   MATCHB 4843   MATERR 47A1   MEASHI 4548
MEASLO 45B3   MORB3  452C   MORCNT 4520   MORINC 44DF   MSG1   46A9
MSG2   46CD   MSG3   46F5  MSG4  471C    MSG5  4740  MSG6  474E
MSG7  4770  NONID  4676   NOTONE 479F   NOTONX 47AC   NOTON1 466C
PATCH1 4546   PRIME  4536  PRINT  469F  RAMSG  47B0    REORDR 479D
REORDX 47A8   REORD1 4658   RESET  44FA  RNGBK  479C    RNGBKX 47A6
RNGBK1 464E   SPACE2= 866E  START = 4400  THI1LL 484C  THI1UL 484E
THI2LL 4854  THI2UL 4856    THI3LL 485C  THI3UL 485E    THI4LL 4860
THI4UL 4862   THI6LL 486C  THI6UL 486E   TH2LL  4556  TH3LL  455B
TH4LL  4560  TH6LL  4565  TLO1LL 4848    TLO1UL 484A    TLO2LL 4850
TLO2UL 4852   TLO3LL 4858   TLO3UL 485A   TLO5LL 4864   TLO5UL 4866
TLO6LL 4868   TLO6UL 486A   TL2LL  45C4  TL3LL  45C9  TL5LL  45CE
TL6LL  45D3  TXRX  = 2000   T1HIID 458D   T1LOID 45FB    T2HIID 4594
T2LOID 4602   T3HIID 459B  T3LOID 4609   T4HIID 45A2    T5LOID 4610
T6HIID 45AC   T6LOID 461A    UNIDEN 4695    X   %

0000
. ASCT    487000

MODULE: MODULE
ERRORS DETECTED: 0

FREE CORE: 8569. WORDS
)USR_VSI_6800:MA6800 CPDEMOFIN,CPDEMOFIN/-SP=CPDEMOFIN/C
```

MODULE; MICROBENCH 6800 CROSS ASSEMBLER (V2)-257 18-MAR-86 16:14:56 PAGE S-1
CROSS REFERENCE TABLE

BUSY 1-41* 5-36 6-36 8-17#
BUSY1 6-51 7-9#
BUSYX 2-4* 6-50 8-28#
CHECB3 3-43 3-46 4-18#
CHERR 3-50 7-37#
CHH1UL 5-2 5-13#
CHH2UL 5-4 5-16#
CHH3UL 5-6 5-19#
CHH6UL 5-10 5-22#
CHL1UL 6-2 6-13#
CHL2UL 6-4 6-16#
CHL3UL 6-6 6-19#
CHL6UL 6-10 6-22#
CNT1 3-56* 4-12 4-14* 4-41* 4-53 4-57 8-38#
CNT2 3-57* 4-28 4-30* 4-42* 5-52 5-57 8-39#
CRLF 1-25# 7-47
CRSR 1-24# 3-28* 3-29* 3-31* 3-33* 3-38* 4-18 4-34
DIALT1 6-57 7-21#
DIALTN 1-43* 5-40 8-20#
DIALX 2-6* 6-56 8-31#
ERFLAG 7-31* 7-38 8-25#
ERRCNT 1-52* 4-4 7-14 7-18 7-22 7-26 7-34 7-43

8-26#
HEAD 1-27# 7-48
HELLO 1-47* 5-45 6-45 8-22#
HELLO1 7-4 7-33#
HELLOX 2-10* 7-3 8-33#
HEX2 1-28#
HEX4 1-26# 4-55 5-54
INCCNT 4-12# 4-21
INVLD 7-42 8-13#
MATCH 3-49 6-49#
MATCHA 4-44* 5-41* 6-29* 6-33* 6-37* 6-41* 6-46* 6-49

8-36#
MATCHB 5-29* 5-33* 5-37* 5-42* 5-46* 6-42* 8-37#
MATERR 4-5* 7-11* 7-15* 7-19* 7-23* 7-27* 7-35* 7-37

7-40* 7-44* 8-24#
MEASHI 3-48 4-16 4-53#
MEASLO 3-47 4-48 5-52#
MORB3 3-45 4-34#
MORCNT 4-28# 4-37
MORINC 3-45# 3-53
MSG1 7-9 7-56#
MSG2 7-13 8-1#
MSG3 7-17 8-3#
MSG4 7-21 8-5#
MSG5 7-25 8-7#
MSG6 7-29 8-9#
MSG7 7-33 8-11#
NONID 5-11 5-24 6-11 6-24 7-5 7-29#
NOTON1 7-2 7-25#

NOTONE 1-45* 6-40 8-21#
NOTONX 2-8* 7-1 8-32#
PATCH1 4-32 4-48#
PRIME 3-44 3-52 4-40#
PRINT 3-51 7-47#
RAMSG 8-35#
REORD1 6-55 7-17#

MODULE; MICROBENCH 6800 CROSS ASSEMBLER (V2)-257 18-MAR-86 16:14:56 PAGE S-2
CROSS REFERENCE TABLE

REORDR 1-37* 5-28 6-28 8-19#
REORDX 1-57* 6-54 8-30#
RESET 3-42 3-55#
RNGBK 1-39* 5-32 6-32 8-18#
RNGBK1 6-53 7-13#
RNGBKX 2-2* 6-52 8-29#
SPACE2 1-29# 5-55 7-49
START 1-22# 1-32
T1HIID 5-14 5-28#
T1LOID 6-14 6-28#
T2HIID 5-17 5-32#
T2LOID 6-17 6-32#
T3HIID 5-20 5-36#
T3LOID 6-20 6-36#
T4HIID 5-8 5-40#
T5LOID 6-8 6-40#
T6HIID 5-23 5-45#
T6LOID 6-23 6-45#
TH2LL 5-3# 5-15
TH3LL 5-5# 5-18
TH4LL 5-7# 5-21
TH6LL 5-9#
THI1LL 2-21* 5-1 8-43#
THI1UL 2-23* 5-13 8-44#
THI2LL 2-35* 5-3 8-48#
THI2UL 2-37* 5-16 8-49#
THI3LL 2-48* 5-5 8-53#
THI3UL 2-50* 5-19 8-54#
THI4LL 2-55* 5-7 8-56#
THI4UL 2-57* 4-15 8-57#
THI6LL 3-13* 5-9 9-7#
THI6UL 3-15* 5-22 9-8#
TL2LL 6-3# 6-15
TL3LL 6-5# 6-18
TL5LL 6-7# 6-21
TL6LL 6-9#
TLO1LL 2-14* 6-1 8-41#
TLO1UL 2-16* 6-13 8-42#
TLO2LL 2-28* 6-3 8-46#
TLO2UL 2-30* 6-16 8-47#
TLO3LL 2-41* 6-5 8-51#
TLO3UL 2-43* 6-19 8-52#
TLO5LL 3-5* 6-7 9-2#
TLO5UL 3-7* 4-31 9-3#
TLO6LL 3-21* 6-9 9-5#
TLO6UL 3-23* 6-22 9-6#
TXRX 1-23#
UNIDEN 7-39 7-42#

APPENDIX 2
Transmitter in Non Burst mode, Receiver in Interrupt mode

MODULE; MICROBENCH 6800 CROSS ASSEMBLER (V2)-257 2-APR-86 10:21:00 PAGE 1

```
 1* THIS PROGRAM DEMONSTRATES THAT THE MT8880 CAN SEND TONE BURSTS IN THE NON
 2* BURST MODE, OF DURATION DETERMINED BY A SOFTWARE COUNTER LOOP. THE RECEIVER
 3* IS SET TO OPERATE IN INTERRUPT MODE AND ON DETECTING A TONE PRODUCES AN
 4* INTERRUPT WHICH MUST BE ACKNOWLEDGED BY A READ FROM THE STATUS REGISTER.
 5*
 6*  EQUATES
 7*
 8      4500          START EQU $4500
 9      2000          TXRX EQU $2000
10      2001          CRSR EQU $2001
11      8723          READ EQU $8723
12      8655          HEAD EQU $8655
13      5100          RAMMSG EQU $5100
14      8662          CRLF EQU $8662
15      5000          DIGIT EQU $5000
16                    *
17      4500           ORG START
18                    *
19                    * * RESET
20                    *
21    4500 A   86  00    LDAA #$00
22    4502 A   B7  2001 STAA CRSR
23    4505 A   86  00    LDAA #$00
24    4507 A   B7  2001 STAA CRSR
25    450A A   86  08    LDAA #$08
26    450C A   B7  2001 STAA CRSR
27    450F A   86  00    LDAA #$00
28    4511 A   B7  2001 STAA CRSR
29                    *
30                    * ENABLE OUTPUT,IRQ,RSEL...NON BURST
31                    *
32    4514 A   86  0D    LDAA #$0D
33    4516 A   B7  2001 STAA CRSR
34    4519 A   86  01    LDAA #$01
35    451B A   B7  2001 STAA CRSR
36                    *
37                    * TYPE MESSAGE
38                    *
39    451E A   BD  8662 JSR CRLF
40    4521 A   BD  8662 JSR CRLF
41    4524 A   CE  5100 LDX #MSG1
42    4527 A   BD  8655 JSR HEAD
43    452A A   BD  8662 JSR CRLF
44                    *
45                    * READ FROM THE KEYBOARD
46                    *
47    452D A   BD  8723DATA JSR READ
48    4530 A   24  08    BCC UPDATE
49    4532 A   B7  5000 STAA DIGIT
50    4535 A   B7  2000 STAA TXRX
51    4538 A   20  06    BRA OK
```

```
52   453A A    B6  5000UPDATE LDAA DIGIT
53   453D A    B7  2000 STAA TXRX
54             *
55             * COUNTER
56             *
57   4540 A    FE  FFFF OK LDX $FFFF
MODULE;    MICROBENCH 6800 CROSS ASSEMBLER (V2)-257  2-APR-86 10:21:00 PAGE 2

1    4543 A    09   COUNTB DEX
2              *
3              * READ FROM THE STATUS REGISTER TO ACKNOWLEGDE IRQ
4              *
5    4544 A    F6  2001 LDAB CRSR
6    4547 A    9C  00    CPX $0000
7    4549 A    26  F8    BNE COUNTB
8              *
9              * TURN OFF OUTPUT BUT ENABLE IRQ
10             *
11   454B A    86  04   TONOFF LDAA #$04
12   454D A    B7  2001 STAA CRSR
13   4550 A    FE  FFFF LDX $FFFF
14   4553 A    09        COUNTP DEX
15             *
16             * READ FROM STATUS REGISTER TO ACKNOWLEGDE IRQ
17             *
18   4554 A    F6  2001 LDAB CRSR
19   4557 A    9C  00    CPX $0000
20   4559 A    26  F8    BNE COUNTP
21             *
22             * ENABLE OUTPUT, IRQ AGAIN
23             *
24   455B A    86  05    LDAA #$05
25   455D A    B7  2001 STAA CRSR
26   4560 A    7E  452D      JMP DATA
27             *
28    5100      ORG RAMMSG
29   5100 A    4E  4F   MSG1 FCC 'NON BURST MODE, RX IRQ .. ENTER DIGIT FOR TX'
30   512C A    00        FCB 0
31              END

MODULE;    MICROBENCH 6800 CROSS ASSEMBLER (V2)-257  2-APR-86 10:21:00 PAGE 3
SYMBOL TABLE

COUNTB 4543     COUNTP 4553     CRLF  = 8662     CRSR  =

2001    DATA   452D
DIGIT = 5000     HEAD  = 8655     MSG1   5100   OK

4540    RAMMSG = 5100
READ  = 8723     START = 4500     TONOFF 454B     TXRX  =

2000    UPDATE 453A
X    %0000
. ASCT  512D  00
```

15

```
MODULE: MODULE
ERRORS DETECTED: 0

FREE CORE: 8901. WORDS
)USR_VSI_6800:MA6800 TXNONBUR,TXNONBUR/-SP=TXNONBUR/C


MODULE;      MICROBENCH 6800 CROSS ASSEMBLER (V2)-257  2-APR-86 10:21:00 PAGE S-1
CROSS REFERENCE TABLE


COUNTB  2-1#   2-7
COUNTP  2-14#  2-20
CRLF   1-14#  1-39   1-40   1-43
CRSR   1-10#  1-22*  1-24*  1-26*  1-28*  1-33*  1-35*  2-5

 2-12*  2-18   2-25*
DATA   1-47#  2-26
DIGIT  1-15#  1-49*  1-52
HEAD   1-12#  1-42
MSG1   1-41   2-29#
OK     1-51   1-57#
RAMMSG  1-13#  2-28
READ   1-11#  1-47
START  1-8#   1-17
TONOFF  2-11#
TXRX   1-9#   1-50*  1-53*
UPDATE  1-48   1-52#

..INIT  0-0#
```

Application Note **MSAN-133**

Designing Large Switching Matrices Using Mitel Analog Switch Arrays

9161-001-050- NA ISSUE 1 January 1990

Introduction

Traditionally, the design of large analog switching matrices has been based upon the use of electromechanical switches. As such, many moving parts were used in the construction of these switch matrices. With advances in electronics, electromechanical switches can now be replaced by equivalent semiconductor switches which offer more economical solutions as well as improved reliability. The Mitel family of analog crosspoint switch devices can be configured easily into various sizes of switch matrices due to the wide variety of switch array configurations and their excellent electrical performance.

The purpose of this application note is to show how a 3-stage non-blocking switch matrix can be implemented using the minimum number of Mitel switch arrays. The theory of optimizing the 3-stage switch matrix will be discussed briefly and examples will be presented. The MT8816 8×16 crosspoint switch is used as the primary example because its large size will reduce the total number of devices for a particular switch matrix design. However, the exercise can be repeated easily with other Mitel switch arrays.

The most common method employed in analog switch matrix design is space division switching whereby signals are physically switched from one signal line to another. Unlike time division switching used in digital matrices, there is little delay added to the signal due to the switching mechanism. The actual delay is determined by the propagation time through the semiconductor switch and the local circuit. This, coupled with low values of on-resistance, allows matrices of different configurations to be built with little signal degradation.

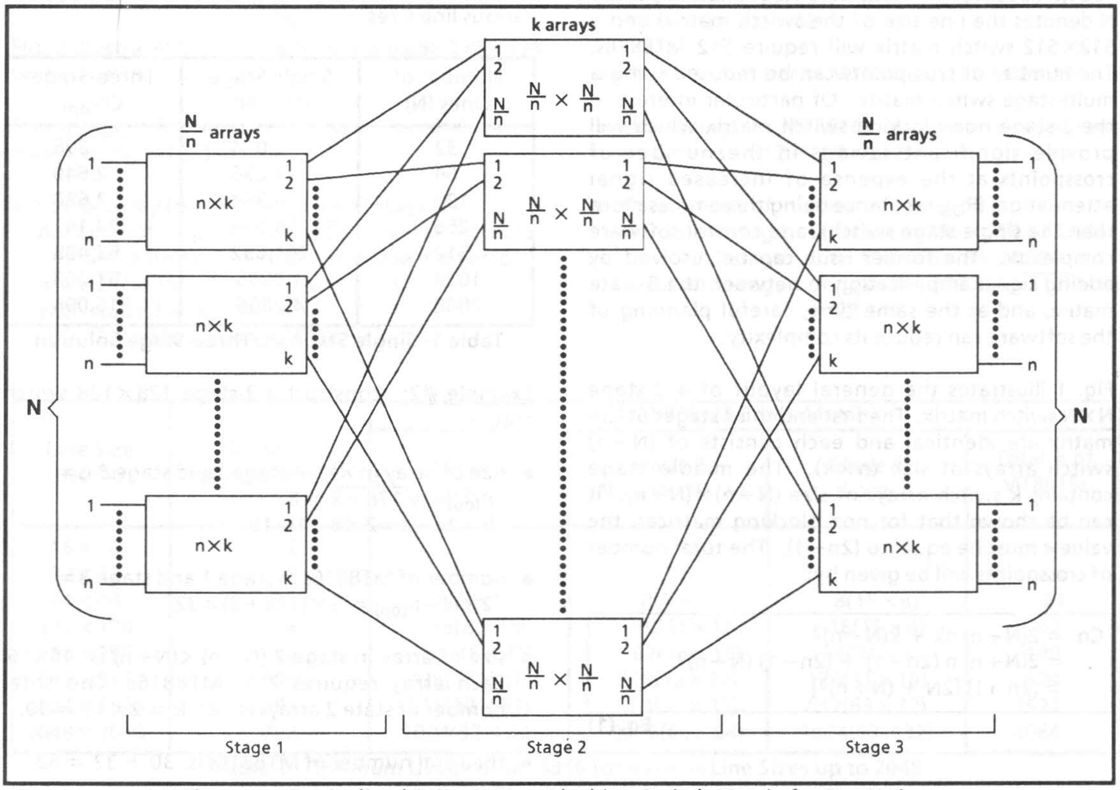

Figure 1 - Generalized 3-Stage Non-Blocking Switch Matrix for N × N Lines

Single State Solution

The simplest switching structure is a single stage non-blocking matrix consisting of an $M \times N$ rectangular array of crosspoints. This switch matrix can always make a connection from one of its M inputs/outputs to one of its N inputs/outputs regardless of any connections already established, e.g., MT8816 can connect any one of 8 Xi inputs/outputs to any one of 16 Yi inputs/outputs. Altogether there are 128 (8×16) crosspoint switches within the matrix. Normally for designing a system with a small matrix size, the number of analog switch arrays can be determined directly by their sizes.

Example # 1: Construct a 32×32 switch matrix using MT8816. The number of MT8816s in the vertical (Y) direction is given by $32 \div 16 = 2$. The number of MT8816s in the horizontal (X) direction is given by $32 \div 8 = 4$. Therefore, 8 (4×2) MT8816s will be required.

Multi-stage Solution

However, when the number of lines gets very large, the number of switch arrays can increase substantially. A 128×128 switch matrix will require 128 MT8816s for a $N \times N$ single stage matrix (where N denotes the line size of the switch matrix) and a 512×512 switch matrix will require 512 MT8816s. The number of crosspoints can be reduced using a multi-stage switch matrix. Of particular interest is the 3-stage non-blocking switch matrix which will provide significant savings in the number of crosspoints at the expense of increased signal attenuation (R_{ON} resistance being three times more than the single stage switch), and control software complexity. The former issue can be resolved by adding signal amplification in between the 3-state matrix, and at the same time, careful planning of the software can reduce its complexity.

Fig. 1 illustrates the general layout of a 3-stage $N \times N$ switch matrix. The first and third stages of the matrix are identical and each consists of $(N \div n)$ switch arrays of size $(n \times k)$. The middle stage contains k switch arrays of size $(N \div n) \times (N \div n)$. It can be shown that for non-blocking matrices, the value k must be equal to $(2n - 1)$. The total number of crosspoints will be given by:

$$\begin{aligned} Cn &= 2(N \div n)\, nk + k(N \div n)^2 \\ &= 2(N \div n)\, n\,(2n-1) + (2n-1)\,(N \div n)^2 \\ &= (2n-1)\,[2N + (N \div n)^2] \end{aligned}$$

...Eq. (1)

To obtain the optimal value of n, differentiate Cn w.r.t. n and set the equation to 0:

$$\frac{dCn}{dn} = 2(2N + (N \div n)^2) - 2(2n-1)(N \div n)^3 = 0$$
$$2n^3 - nN + N = 0$$

...Eq. (2)

As N gets very large, Eq. (2) can be approximated by:

$$2n^3 - nN = 0$$
$$n_{(op)} = \sqrt{\left(\frac{N}{2}\right)}$$

...Eq. (3)

where $n_{(op)}$ denotes the optimum value of n.

The optimum value of Cn, $Cn_{(op)}$ can be found by substituting Eq. (3) into Eq. (1):

$$Cn_{(op)} = 4N\,[\sqrt{2N} - 1]$$

...Eq. (4)

where $Cn_{(op)}$ denotes the minimum number of crosspoints.

Table 1 compares the number of crosspoints in a single-stage matrix versus a three-stage matrix for various line sizes.

Number of Lines (N)	Single Stage ($N \times N$)	Three-Stage $Cn_{(op)}$
32	1,024	896
64	4,096	2,640
128	16,384	7,680
256	65,536	22,147
512	261,632	63,488
1024	1.0E06	181,268
2048	4.2E06	516,096

Table 1- Single Stage vs. Three-Stage Solution

Example #2: Construct a 3-stage 128×128 switch matrix.

- size of array ($n \times k$) in stage 1and stage 3 is=
  $n_{(op)} = \sqrt{128 \div 2} = 8$
  $k = 2n - 1 = 2 \times 8 - 1 = 15$
- number of MT8816s in stage 1 and stage 3=
  $2 \times N \div n_{(op)} = 2 \times (128 \div 8) = 32$
- size of array in stage 2 $(N \div n) \times (N \div n)$ is: 16×16. Each array requires $2 \times$ MT8816s. The total number of state 2 arrays is: $2 \times k = 2 \times 15 = 30$.
- the total number of MT8816s is: $30 + 32 = 62$.

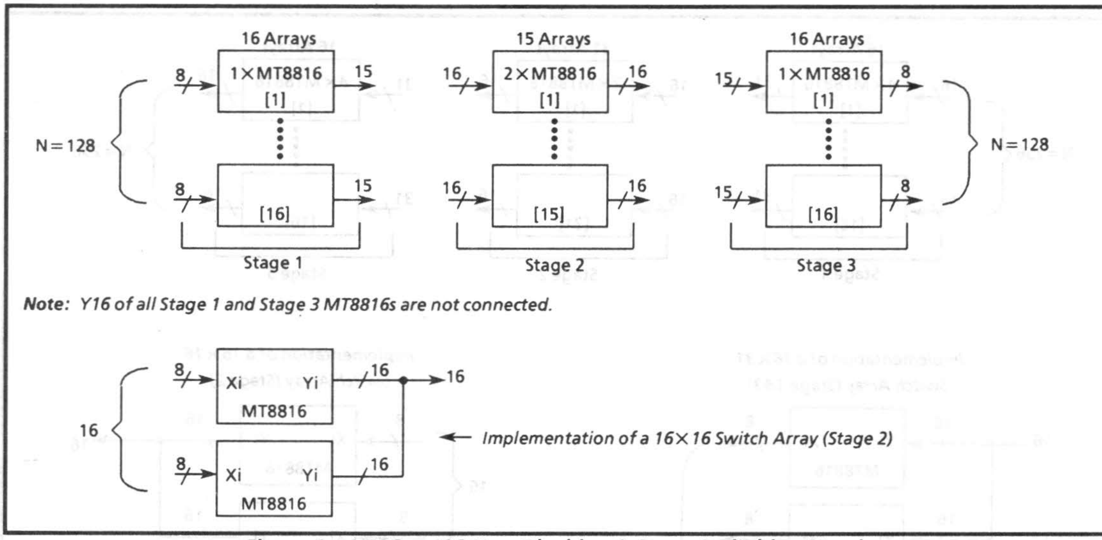

Figure 2 - A 128 × 128 Non-Blocking 3-Stage Switching Matrix

- The savings in MT8816s over the single stage solution is: $128 - 62 = 66$

- comparison of number of crosspoints:
  single stage: $Cn(N \times N) = 128 \times 128 = 16{,}384$
  3-stage: $Cn = 66 \times 16 \times 8 = 8{,}448$
  optimal 3-stage: $Cn_{(op)} = 4 \times 128 \times [\sqrt{(256)} - 1)] = 7{,}680$

Fig. 2 illustrates the structure of a 3-stage 128×128 switch matrix.

Example #3: Construct a 3-stage 256×256 switch matrix using MT8816s.

- size of array (n×k) in stage 1and stage 3 is: notice that $n_{(op)} = \sqrt{128 \div 2}$ is not an integral number, a better line size in this case is given by: $n = \sqrt{256} = 16$, $k = 2n - 1 = 2 \times 16 - 1 = 31$.
  Each stage 1 array requires:
  $(32 \div 16) \times (16 \div 8) = 4 \times$ MT8816s
  number of MT8816s in stage 1 and stage 3:
  $2 \times (N \div n) \times 4 = 2 \times (256 \div 16) \times 4 = 128$

- Size of array in the second stage is: $(N \div n) \times (N \div n) = 16 \times 16$. Each stage 2 array requires $(16 \div 16) \times (16 \div 8) = 2 \times$ MT8816s.
  The total number of MT8816s for stage 2 is:
  $2 \times k = 2 \times 31 = 62$

- the total number of MT8816s $= 128 + 62 = 190$.

- the savings in MT8816s over the single stage solution is: $512 - 190 = 332$.

- Comparison of number of crosspoints:
  single stage: $Cn(N \times N) = 256 \times 256 = 65{,}536$
  3-stage: $Cn = 190 \times 16 \times 8 = 24{,}320$
  optimal 3-stage: $Cn_{(op)} = 4 \times 256 \times [\sqrt{(512)} - 1)] = 22{,}147$

Line Size (N×N)	MT8816 (Single Stage)	MT8816s (3-Stage Matrix)			
		Stage 1 n×k	Stage 2 (N÷n)×(N÷n)	Stage 3 k×n	Total # of MT8816s
16×16	2	---	---	---	---
32×32	8	---	---	---	---
64×64	32	8(8×15)	8(8×8)	8(15×8)	24
128×128	128	16(8×15)	30(16×16)	16(15×8)	62
256×256	512	64(16×31)	62(16×16)	64(31×16)	190
512×512	2048	128(16×31)	248(32×32)	128(31×16)	504
1024×1024	8192	512(32×63)	504(32×32)	512(63×32)	1524
2048×2048	32768	1024(32×63)	2016(64×64)	1024(63×32)	4064

Table 2 - Optimum Usage of MT8816 for Various Line Sizes up to 2048

Note: the individual array sizes are shown inside the brackets for a number of 3-stage matrices.

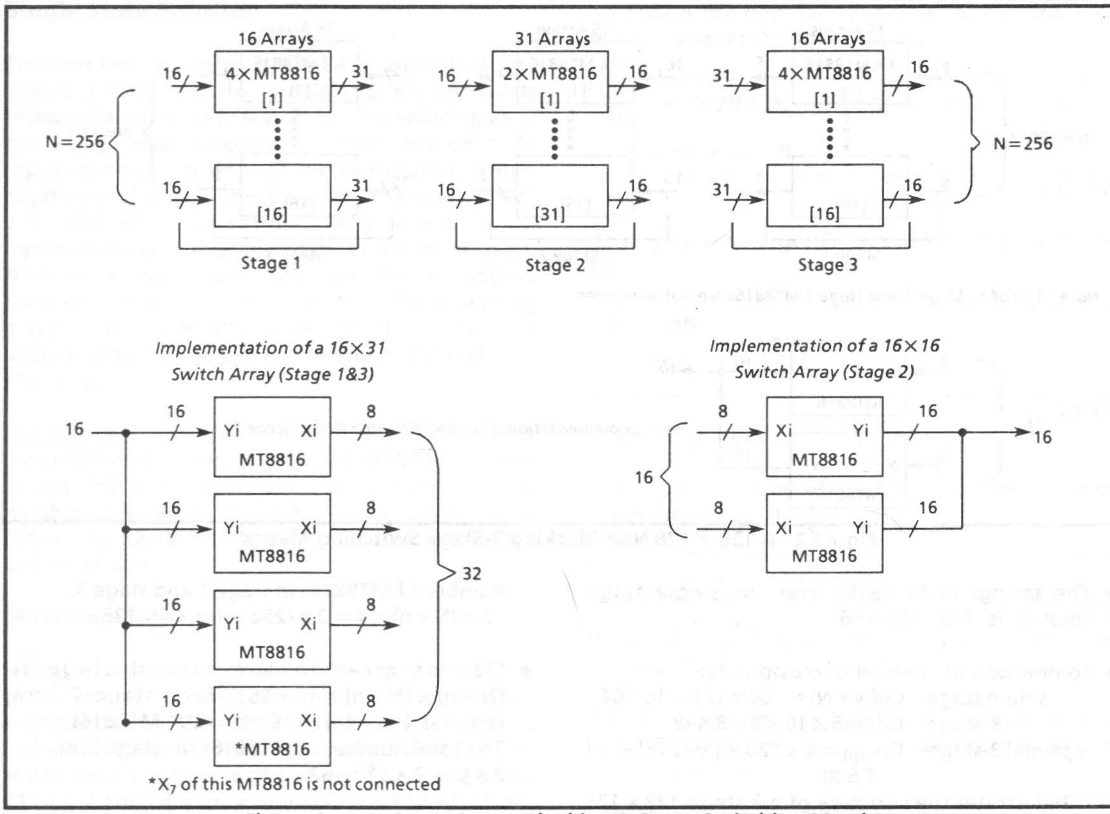

Figure 3 - A 256 × 256 Non-Blocking 3-Stage Switching Matrix

Fig. 3 illustrates the structure of a 3-stage 256×256 switch array.

Table 2 summarizes the optimum usage of MT8816s for various line sizes up to 2,048.

Conclusion

As observed, even with the use of the 3-stage matrix, the number of switch arrays can be very large and makes the design uneconomical. The solution is to either to adopt higher stage switch matrix design (of more than three stages) or to introduce partial blocking without increasing the number of switch arrays.

References

Charles Clos, *"A Study of Non-Blocking Switching Networks"*, Bell System Technical Journal, March 1953, pp. 406-424.

John Bellamy, Digital Telephony, pp. 220-242, pub. by John Wiley & Sons, 1982, ISBN 0-471-08089-6.

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